XC2000 and XE166 Family Derivatives / Base Line

Electromagnetic Emission Summary

AP16167

Test Report
V1.0 2009-04
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## Revision History: V1.0, 2009-04

Previous Version: none

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1 Introduction

This summary describes the electromagnetic emission behaviour of the following microcontroller products:

**PG-LQFP-64 package:**
- XC223xM derivatives
- XC233xA derivatives
- XC2735X derivatives
- XE162xM derivatives

**PG-LQFP-100 package:**
- XC226xM derivatives
- XC236xA derivatives
- XC2765X derivatives
- XE164xM derivatives

**PG-LQFP-144 package:**
- XC228xM derivatives
- XC238xA derivatives
- XC2785X derivatives
- XE167xM derivatives

Slight differences in the electromagnetic emission performance exist between the package versions (PG-LQFP-64, 100, 144). The derivatives which come in the same package show similar emission due to the fact that they contain similar microcontroller designs.

Detailed reports on electromagnetic emission – dedicated to every package version – are available on request as listed in chapter 7. The detailed reports contain much more information about the test board, the software settings wrt. module operation, additional probed pins, and comparison with other Infineon 16-bit microcontrollers.

The following derivatives have been measured as representatives of the different packages to obtain the electromagnetic emission results found in this summary:

**PG-LQFP-64 package:** XC2735X

**PG-LQFP-100 package:** XC2361A

**PG-LQFP-144 package:** XC2286M

All EMI test results presented in this report are obtained from hardware and software test setups compliant to the “Generic IC EMC Test Specification” (“BISS paper”), open copyright 2004 by Robert Bosch GmbH, Infineon Technologies AG, Continental AG (former Siemens-VDO).

All significant emission peaks around 950 MHz are mainly caused by transmitters in the GSM band, and not caused by microcontroller emission.
### 2 Emission Measurement Methods

The setup used for electromagnetic emission measurement complies fully with the BISS test specification which can be provided on request. One test board was designed for every PG-LQFP package with similar layout. The test board is used for conducted and radiated emission measurements.

Conducted emission is measured using the standardized 150 $\Omega$ network, see figure 1. This network is used for both port and power supply emission measurements. Only crosstalk noise is measured; i.e. the port pins under test are never actively switching. Frequency range is 150 kHz to 1 GHz.

Fig. 1 shows the schematic 150 $\Omega$ network connection to the microcontroller (IC under test) and the general layout of each 150 $\Omega$ probing net.

![Figure 1 150 $\Omega$ probing networks for conducted emission measurement](image1)

150Ω networks are provided for conducted emission measurements according the international standard IEC 61967 part 4 and the BISS test specification for a set of signals and power supply nets. All digital power supply nets plus a subset of I/O pins (typically located in the center of all 4 package edges) are measured, see figure 2.

![Figure 2 Probed supply and signal nets for conducted emission measurement](image2)
Radiated emission is measured using the standard mini TEM cell according IEC 61967 part 2 and BISS emission test specification. The frequency range is from 150 kHz to 1 GHz.

**Figure 3** Measurement setup for radiated emission

Measurement instrumentation and conditions:
- **Spectrum analyzer:** Rohde & Schwarz FSP7
- **Detector type:** Peak detector
- **Measurement time:** For all measurements, the emission measurement time (10ms) at one frequency is longer than the test software loop duration.
- **Pre-Amplifier:** internal
- **Data generation software:** Rohde & Schwarz EMIPAK 9950
- **Environment:** temperature 23°C ± 5°C
- **Supply:** nominal voltage ± 5%

For all measurements the noise floor is at least 6dB below the limit.

<table>
<thead>
<tr>
<th>Frequency range</th>
<th>Spectrum Analyzer</th>
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<tbody>
<tr>
<td><strong>150 Ω TEM</strong></td>
<td></td>
</tr>
<tr>
<td>150 kHz to 30 MHz</td>
<td><strong>RBW</strong> 10kHz</td>
</tr>
<tr>
<td>30 MHz to 200 MHz</td>
<td><strong>Sweep time</strong> ( t_s = \frac{NP \cdot LT \cdot FR}{RBW} )</td>
</tr>
<tr>
<td>200 MHz to 1000 MHz</td>
<td></td>
</tr>
</tbody>
</table>

*) \( NP \) = number of points; \( LT \) = loop time; \( FR \) = frequency range
3 Emission Limit Curves

For reference purpose, all measured emission spectra are enhanced by the “external digital bus systems” limit curves taken from the BISS specification. Figure 4 introduces these 3 limit curves:

- Conducted emission 150 Ω, limit for supply pin emission (Supply Conducted),
- Conducted emission 150 Ω, limit for port pin emission (I/O Conducted),
- Radiated emission, limit for Mini TEM cell emission (Radiated).

![Figure 4 BISS limit curves in logarithmic scale](image)

If the measured emission stays below the respective limit, the measured supply or signal net is treated as “clean”. If the measured emission violates the respective limit for one or more frequencies, some more care must be taken for an EMC-friendly PCB layout. Infineon strongly recommends to use all microcontroller hardware settings provided for reduction of electromagnetic emission (as long as your required system performance permits):

- Reduce system clock frequency
- Disable unused clocks (e.g. CLKOUT [automatically disabled after reset])
- Reduce output pad driver strength (up to 6 settings available for all port pins) [1]
- Consider Infineon’s general and product-specific PCB design guidelines which propose optimized power supply layout and decoupling concept [2] [3]
4 Microcontroller Operation during Test

To get a realistic impression of the microcontroller's emission potential, so called "application-typical" settings have been applied during the tests. This means:

- CPU and all functional modules are active
- CLKOUT is disabled
- High-speed interfaces are active (e.g. SPI @ 5 MBit/s, ASC / LIN / CAN @ 500 kBit/s)
- Other I/Os operate at lower data rates
- All output pad driver strengths are selected according their data rates, driving 22pF load. Since most pins cannot be configured individually, some more pins of the same ports are also forced to stronger state even if this would be desired only for one or two port pins. This is the ratio in percent of driver settings (All GPIOs without ADC channels) used for the emission tests:

<table>
<thead>
<tr>
<th>Driver strength</th>
<th>PG-LQFP-64</th>
<th>PG-LQFP-100</th>
<th>PG-LQFP-144</th>
</tr>
</thead>
<tbody>
<tr>
<td>Weak</td>
<td>57 %</td>
<td>50 %</td>
<td>32 %</td>
</tr>
<tr>
<td>Medium</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Strong-soft</td>
<td>0</td>
<td>14 %</td>
<td>9 %</td>
</tr>
<tr>
<td>Strong-medium</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Strong-sharp</td>
<td>40 %</td>
<td>34 %</td>
<td>58 %</td>
</tr>
<tr>
<td>Extra-strong</td>
<td>3 %</td>
<td>2 %</td>
<td>1 %</td>
</tr>
</tbody>
</table>

- External memory bus (if available) is not used
- Execution from on-chip flash memory

In addition, a worst-case operation scenario is measured for reference purpose:

- CLKOUT is activated for worst-case operation.
- The external memory bus is never enabled since it is not recommended to be used because of significant occupation of ports and execution slow-down by wait-states.

The power supply system is in all cases configured as follows:

- VDDP and VDDP1 supplies are 5.0 V
- VDDI and VDDIM are supplied by internal voltage regulator

The crystal frequency is 8 MHz in all cases.
5 Application-Typical Emission Tests

General remarks:

The microcontroller is running in “application-typical” mode. The general hardware settings are described in chapter 4.

The I/O supply voltage VDDP is set to 5.0 V.

Any emission peaks rising from lower noise floor in the 900 MHz range result from GSM transmitters and are not related to microcontroller operation.

Summary of emission behaviour in application-typical operating mode:

1) VDDI reflects the emission resulting from the core clock tree, i.e. the harmonics are multiples of the system clock frequency. However, since all measured microcontroller derivatives use an internal voltage regulator, the VDDI net has no connection to an external voltage regulator. The only component connected to VDDI is the decoupling capacitor. Thus no effective antenna structure to radiate emission from VDDI should be provided on the PCB, and the VDDI emission should not be system-relevant.

2) Both power supplies VDDI and VDDP show highest emission on the smallest device (PG-LQFP-64). Reason is that this package provides no e-pad for central VSS solder connection. From this result, it is advisable to solder the VSS e-pad when using PG-LQFP-100 and PG-LQFP-144 devices to reduce emission.

3) Core noise coupling from VDDI to VDDP is efficiently suppressed in PG-LQFP-100 and PG-LQFP-144 devices, but some coupling happens on the PG-LQFP-64 package which is again due to the missing VSS e-pad, which connects all VSS pins (from core and I/O domain) with very low impedance and thus offers a better common reference point for the VDDI and VDDP noise.

4) I/O emission is – in contrast to supply emission – visible up to 1 GHz. Reason is that there is no available on-chip space to design decoupling capacitors for the VDDP system. Also I/O pins cannot be decoupled on chip nor on PCB. This is the reason why the BISS limit curve for I/O emission is defined 10 dB above the supply limit curve. Please note that all I/O pins where emission is measured are inactive (i.e. not switching) pads which are set to state “output low”. From the emission shape, special care on PCB layout might be necessary to prevent I/O noise from being coupled to any antenna structures on the PCB. Advisable PCB layout rules are:
   a. Keep signal traces short
   b. Route signal traces as micro-strip or stripline (ground shielding)
   c. Avoid signal trace vias through power or ground planes
   d. Use lowest permissible data rates
   e. Use weakest permissible pad driver settings

For further recommendations please refer to Infineon’s application notes listed in chapter 7.

5) Summarized, the emissions of all package versions stay below the BISS limits and thus should not cause any severe problems for low-emission PCB design. More care on power routing and noise decoupling should be taken for PG-LQFP-64 derivatives.

6) Radiated emission stays far below BISS limits – there is no indication of any significant direct radiation from chip or package, independent from the package size.

7) The part of conducted and radiated emission which is caused by switching I/O noise will decrease when the VDDP voltage is lowered from 5.0 V to 3.3 V. In this case emission peaks may be reduced by ca. 6 dB.
Application-typical conducted emission on core supply net VDDI; system clock is 20 MHz.

Figure 5  PG-LQFP-64; Application; VDDI conducted; 20 MHz

Figure 6  PG-LQFP-100; Application; VDDI conducted; 20 MHz

Figure 7  PG-LQFP-144; Application; VDDI conducted; 20 MHz
Application-typical conducted emission on core supply net VDDI; system clock is 80 MHz.

Figure 8   PG-LQFP-64; Application; VDDI conducted; 80 MHz

Figure 9   PG-LQFP-100; Application; VDDI conducted; 80 MHz

Figure 10  PG-LQFP-144; Application; VDDI conducted; 80 MHz
Application-typical conducted emission on I/O supply net VDDP; system clock is 20 MHz.

Figure 11  PG-LQFP-64; Application; VDDP conducted; 20 MHz

Figure 12  PG-LQFP-100; Application; VDDP conducted; 20 MHz

Figure 13  PG-LQFP-144; Application; VDDP conducted; 20 MHz
Application-typical conducted emission on I/O supply net VDDP; system clock is 80 MHz.

Figure 14  PG-LQFP-64; Application; VDDP conducted; 80 MHz

Figure 15  PG-LQFP-100; Application; VDDP conducted; 80 MHz

Figure 16  PG-LQFP-144; Application; VDDP conducted; 80 MHz
Application-typical conducted emission on I/O net at upper package edge; system clock is 20 MHz.

Figure 17  PG-LQFP-64; Application; P10.14 conducted; 20 MHz

Figure 18  PG-LQFP-100; Application; P1.4 conducted; 20 MHz

Figure 19  PG-LQFP-144; Application; P9.5 conducted; 20 MHz
Application-typical conducted emission on I/O net at upper package edge; system clock is 80 MHz.

Figure 20  PG-LQFP-64; Application; P10.14 conducted; 80 MHz

Figure 21  PG-LQFP-100; Application; P1.4 conducted; 80 MHz

Figure 22  PG-LQFP-144; Application; P9.5 conducted; 80 MHz
Application-typical conducted emission on I/O net at left package edge; system clock is 20 MHz.

Figure 23  PG-LQFP-64; Application; P6.1 conducted; 20 MHz

Figure 24  PG-LQFP-100; Application; VAREF conducted; 20 MHz

Figure 25  PG-LQFP-144; Application; VAREF conducted; 20 MHz
Application-typical conducted emission on I/O net at left package edge; system clock is 80 MHz.

**Figure 26**  PG-LQFP-64; Application; P6.1 conducted; 80 MHz

**Figure 27**  PG-LQFP-100; Application; VAREF conducted; 80 MHz

**Figure 28**  PG-LQFP-144; Application; VAREF conducted; 80 MHz
Application-typical radiated emission; system clock is 20 MHz.

Figure 29  PG-LQFP-64; Application; radiated; 20 MHz

Figure 30  PG-LQFP-100; Application; radiated; 20 MHz

Figure 31  PG-LQFP-144; Application; radiated; 20 MHz
Application-typical radiated emission; system clock is 80 MHz.

Figure 32  PG-LQFP-64; Application; radiated; 80 MHz

Figure 33  PG-LQFP-100; Application; radiated; 80 MHz

Figure 34  PG-LQFP-144; Application; radiated; 80 MHz
6  Worst-Case Emission Tests

The microcontroller is running in “worst-case” mode. This means that in addition to the “application-specific” settings, CLKOUT function is activated on port pin P2.8. The toggle rate on CLKOUT is equal to the system clock (20MHz or 80MHz). The CLKOUT pin is set to the strongest driver setting “extra-strong”.

If CLKOUT is used to drive slower clocks, its P2.8 driver should be configured to weaker settings which significantly reduce the electromagnetic emission; figures 35 and 36 show the emission reduction potential by pad driver scaling for the two cases VDDP=5.0V and VDDP=3.3V.

![Graph showing emission reduction by pad driver settings for VDDP = 5.0V](image)

**Figure 35**  Emission reduction by pad driver settings for VDDP = 5.0V

![Graph showing emission reduction by pad driver settings for VDDP = 3.3V](image)

**Figure 36**  Emission reduction by pad driver settings for VDDP = 3.3V
The weakest possible driver setting for a port pin depends on:

- VDDP voltage
- External capacitive load
- Data rate
- Edge-to-period ratio of the data signal
- Ambient temperature

Figure 37 explains how to use the decision graphs provided in the “Scalable Pads Application Note” [1]. The title of each diagram indicates the conditions (edge/voltage/temperature) for the shown values:

**Edge** is either “T/4” (meaning the rise time and the fall time take each 1/4 of the data rate period) or “T/6” (meaning the rise time and the fall time take each 1/6 of the data rate period).

**Voltage** indicates the I/O pad supply voltage VDDP and is either 3.3 V or 5.0 V.

**Temperature** indicates the ambient temperature and ranges from -40°C up to +125°C.

The maximal clock/data rate to meet good signal integrity is given in [MHz] for capacitive loads of 10, 15, 22, 33, 47 pF and driver selections of weak, medium, strong soft/medium/sharp/extra-strong. In Fig. 35, the resulting maximum data rates for the strong-medium driver are marked with red circles:

If the strong-medium driver is loaded with 10 pF (which means actually 13 pF including the oscilloscope probe load), it is able to drive a clean 37 MHz signal (under the above mentioned edge/voltage/temperature conditions).

An 18 pF load (15+3pF) can be driven at 31 MHz; a 25 pF load (22+3 pF) can be driven at 30 MHz; a 36 pF load (33+3pF) can be driven at 28 MHz; a 50 pF load (47+3 pF) can be driven at 26 MHz.

![Figure 37](image-url)
Figures 38 to 41 show decision graphs for some variations of these parameters. It is assumed that rising edge and falling edge occupy \(\frac{1}{4}\) of the signal period. For a full description and suggestions please refer to [1].

**Figure 38** Pad driver selection for VDDP = 5.0 V at -40°C

**Figure 39** Pad driver selection for VDDP = 5.0 V at +125°C
Figure 40  Pad driver selection for VDDP = 3.3 V at -40°C

Figure 41  Pad driver selection for VDDP = 3.3 V at +125°C
General remarks:

The microcontroller is running in “worst-case” mode. The general hardware settings are described in chapter 4.

The I/O supply voltage VDDP is set to 5.0V.

Any emission peaks in the 900 MHz range rising from lower noise floor result from GSM transmitters and are not related to microcontroller operation.

Summary of emission behaviour in worst-case operating mode:

1) I/O noise is efficiently coupled to VDDI, especially in the smallest PG-LQFP-64 package. VDDI emission from CLKOUT is less in PG-LQFP-100 and PG-LQFP-144, where QFP144 shows the lowest CLKOUT coupling.

2) I/O noise is massively seen as VDDP emission. Here, the smallest package QFP64 shows the best damping towards high frequency > 600 MHz. VDDP emission from CLKOUT is less and comparable in PG-LQFP-100 and PG-LQFP-144 with significant high-frequency peaks above 600 MHz.

3) I/O pin emission is highest between 500 and 700 MHz. Reason is that crosstalk from VDDP to the port pins becomes more efficient at higher frequency. Above 700 MHz, the natural damping occurs. Please note that all I/O pins where emission is measured are inactive (i.e. not switching) pads which are set to state “output low”. From the emission shape, special care on PCB layout might be necessary to prevent I/O noise from being coupled to any antenna structures on the PCB. Advisable PCB layout rules are:

   b. Keep signal traces short
   c. Route signal traces as micro-strip or stripline (ground shielding)
   d. Avoid signal trace vias through power or ground planes
   e. Use lowest permissible data rates
   f. Use weakest permissible pad driver settings

For further recommendations please refer to Infineon's application notes listed in chapter 7.

4) Summarized, the activation of any high-speed clock or data driver with strongest settings rise real layout challenges for low-emission PCB layout. Thus high-speed signals should be avoided. If this is not possible, they should be limited by clock rate and driver strength. Hints for the expected emission reduction have been provided above. In case of strong high-speed signals, the smallest package PG-LQFP-64 shows lowest emission on I/O signals; minor differences are visible between PG-LQFP-100 and PG-LQFP-144. The bigger packages show significant high-frequency emission on I/O nets.

5) Radiated emission exceeds the BISS limits. The level can be significantly decreased when operating I/Os at lower speed and select weaker driver strengths, as discussed above. All packages show similar emission, where the PG-LQFP-64 stays ca. 6dB below the bigger ones.
Worst-case conducted emission on core supply net VDDI; system clock is 20 MHz.

Figure 42  PG-LQFP-64; Worst-case; VDDI conducted; 20 MHz

Figure 43  PG-LQFP-100; Worst-case; VDDI conducted; 20 MHz

Figure 44  PG-LQFP-144; Worst-case; VDDI conducted; 20 MHz
Worst-case conducted emission on core supply net VDDI; system clock is 80 MHz.

Figure 45  PG-LQFP-64; Worst-case; VDDI conducted; 80 MHz

Figure 46  PG-LQFP-100; Worst-case; VDDI conducted; 80 MHz

Figure 47  PG-LQFP-144; Worst-case; VDDI conducted; 80 MHz
Worst-case conducted emission on I/O supply net VDDP; system clock is 20 MHz.

**Figure 48** PG-LQFP-64; Worst-case; VDDP conducted; 20 MHz

**Figure 49** PG-LQFP-100; Worst-case; VDDP conducted; 20 MHz

**Figure 50** PG-LQFP-144; Worst-case; VDDP conducted; 20 MHz
Worst-case conducted emission on I/O supply net VDDP; system clock is 80 MHz.

Figure 51  PG-LQFP-64; Worst-case; VDDP conducted; 80 MHz

Figure 52  PG-LQFP-100; Worst-case; VDDP conducted; 80 MHz

Figure 53  PG-LQFP-144; Worst-case; VDDP conducted; 80 MHz
Worst-case conducted emission on I/O net at upper package edge; system clock is 20 MHz.

Figure 54  PG-LQFP-64; Worst-case; P10.14 conducted; 20 MHz

Figure 55  PG-LQFP-100; Worst-case; P1.4 conducted; 20 MHz

Figure 56  PG-LQFP-144; Worst-case; P9.5 conducted; 20 MHz
Worst-case conducted emission on I/O net at upper package edge; system clock is 80 MHz.

Figure 57  PG-LQFP-64; Worst-case; P10.14 conducted; 80 MHz

Figure 58  PG-LQFP-100; Worst-case; P1.4 conducted; 80 MHz

Figure 59  PG-LQFP-144; Worst-case; P9.5 conducted; 80 MHz
Worst-case conducted emission on I/O net at left package edge; system clock is 20 MHz.

Figure 60  PG-LQFP-64; Worst-case; P6.1 conducted; 20 MHz

Figure 61  PG-LQFP-100; Worst-case; VAREF conducted; 20 MHz

Figure 62  PG-LQFP-144; Worst-case; VAREF conducted; 20 MHz
Worst-case conducted emission on I/O net at left package edge; system clock is 80 MHz.

Figure 63  PG-LQFP-64; Worst-case; P6.1 conducted; 80 MHz

Figure 64  PG-LQFP-100; Worst-case; VAREF conducted; 80 MHz

Figure 65  PG-LQFP-144; Worst-case; VAREF conducted; 80 MHz
Worst-case radiated emission; system clock is 20 MHz.

Figure 66  PG-LQFP-64; Worst-case; radiated; 20 MHz

Figure 67  PG-LQFP-100; Worst-case; radiated; 20 MHz

Figure 68  PG-LQFP-144; Worst-case; radiated; 20 MHz
Worst-case radiated emission; system clock is 80 MHz.

Figure 69  PG-LQFP-64; Worst-case; radiated; 80 MHz

Figure 70  PG-LQFP-100; Worst-case; radiated; 80 MHz

Figure 71  PG-LQFP-144; Worst-case; radiated; 80 MHz
7 References

These documents can be downloaded from the Infineon microcontroller internet pages:

http://www.infineon.com/cms/en/product/channel.html?channel=db3a30431c69a49d011c8a7c069203dc


http://www.infineon.com/cms/en/product/channel.html?channel=ff80808112ab681d0112ab6b2dfc0756


These documents are available on request:

- Generic IC EMC Test Specification ("BISS paper"), open copyright 2004 by Robert Bosch GmbH, Infineon Technologies AG, Continental AG (former Siemens-VDO)
8 Executive Summary

1) Conducted and radiated emissions of all XC2000 and XE166 Family Base Line Derivatives stay below the BISS limits for application-typical operation up to 80 MHz and thus should not cause any severe problems for low-emission PCB design.

2) PG-LQFP-64 derivatives show higher emission than PG-LQFP-100 and PG-LQFP-144 due to missing VSS e-pad. Thus more care on power routing and noise decoupling should be taken for PCBs using PG-LQFP-64 devices. For PG-LQFP-100 and PG-LQFP-144 it is strongly recommended to solder the VSS e-pad.

3) Since all microcontrollers use internal voltage regulators, the VDDI pins should only be connected to local decoupling capacitors. Thus no effective antenna structure to radiate emission from VDDI should be provided on the PCB, and the VDDI emission should not be system-relevant.

4) Core noise coupling from VDDI to VDDP is efficiently suppressed in PG-LQFP-100 and PG-LQFP-144 devices, but some coupling happens on the PG-LQFP-64 package which is again due to the missing VSS e-pad which offers a low-impedance common reference point for the VDDI and VDDP noise.

5) I/O emission (i.e. noise propagation through inactive pads) is – in contrast to supply emission – visible up to 1 GHz. Reason is that there is no available on-chip space to design decoupling capacitors for the VDDP system. Also I/O pins can neither be decoupled on chip nor on PCB. Special care on PCB layout is advisable to prevent I/O noise from being coupled to any antenna structures on the PCB:
   - Keep signal traces short
   - Route signal traces as micro-strip or stripline (ground shielding)
   - Avoid signal trace vias through power or ground planes
   - Use lowest permissible data rates
   - Use weakest permissible pad driver settings

   For further recommendations please refer to Infineon’s application notes listed in chapter 7.

6) Conducted and radiated emission exceeds the BISS limits if the strongest pad drivers are selected for high-speed signals. The level can be significantly decreased when operating I/Os at lower speed and select weaker driver strengths, as discussed above. All packages show similar emission, where the smallest PG-LQFP-64 stays ca. 6 dB below the bigger ones.

7) I/O noise is visible on VDDP, but also coupled to VDDI, especially in the smallest PG-LQFP-64 package. VDDI emission from CLKOUT is less in PG-LQFP-100 and PG-LQFP-144, where the PG-LQFP-144 shows the lowest CLKOUT coupling. I/O pin emission is highest between 500 MHz and 700 MHz. Reason is that crosstalk from VDDP to the port pins becomes more efficient at higher frequency. Above 700 MHz, the natural damping occurs.

8) The part of conducted and radiated emission which is caused by switching I/O noise will decrease when the VDDP voltage is lowered from 5.0 V to 3.3 V. In this case emission peaks may be reduced by ca. 6 dB.

9) The activation of any high-speed clock or data driver with strongest settings rise real layout challenges for low-emission PCB layout. Thus high-speed signals should be avoided. If this is not possible, they should be limited by clock rate and driver strength. In case of strong high-speed signals, the smallest package PG-LQFP-64 shows lowest emission on I/O signals; minor differences are visible between PG-LQFP-100 and PG-LQFP-144.