Never stop thinking

XC2000/XE166 Family

AP16146

Pin Configuration, Power Supply and Reset

Application Note

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Device1

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Previous Version: none

Page	Subjects (major changes since last revision)
5	Enhance to further product
9	Add a table with new cap values, packages

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1 Introduction

The XC2000/XE166 family from Infineon offers a new generation of 16-bit microcontrollers based on the high-performance C166S V2 core, with new features to reduce system costs.

This application note focuses on basic hardware related features such as EVR (Embedded Voltage Regulator), PORST (Power ON RESET) and the configuration of special function pins. This document covers the functionality of the following product families:

- XC22xxM, XC22xxN, XC22xxH, XC22xxI
- XC23xxA, XC23xxB, XC23xxC, XC23xxE
- XC27x5X, XC27x4X, XC27x7X, XC27x8X
- XE166M, XE166N, XE166H

This application note does not support completely the following product families.

- XC22xx, XC22xxL, XC22xxU
- XC23xx, XC23xxD, XC22xxS
- XC27x6X, XC27x3X, XC27x2X
- XE166, XE166L, XE166U

For detailed and updated information please refer to the latest datasheet.

2 Basic Configuration

For correct operation, the connection of several pins must be considered:

- Test (/TRST, /TESTM)
- Power (VDDIM, VDDI1,VDDPA, VDDPB,VSS)
- Reset (/PORST, ESR0, ESR1,ESR2)
- Start-up (Port 10)

2.1 Test

The **/TESTM** pin enables factory test modes.

For normal operation **/TESTM** must be connected directly to VDDPB (Digital Pad Supply Voltage for Domain B).

After **/PORST,** the internal startup software uses the initial value of the **/TRST** pin to decide if normal internal startup, other startup modes, or a debug mode is to be initialized.

For normal operation, it should have a pull-down resistor to Vss (Digital Ground). A high level at this pin plus a rising edge of **/PORST**, activates the debug system or other startup modes.

2.2 Power

The device operates in the voltage range of 3.0V to 5.5V. The on-chip embedded voltage supply consists of two separated voltage regulators, **VDDIM** and **VDDI1**, generating the core voltage of 1.5V. Different power-down modes reduce or switch off the core voltages.

There are two groups of I/O pins, which can either be operated with the same voltage or with different voltages. For example the A/D conversion and some other pins, need 5 Volts, while an external data memory needs 3.3 Volts. In this case pin **VDDPA** (Digital Pad Supply Voltage for Domain A) is connected to 5 Volts and the pins **VDDPB** (Digital Pad Supply Voltage for Domain B) are connected to 3.3 Volts.

The embedded voltage regulator is divided in domain M (pin **VDDIM**) and domain 1 (**VDDI1**). In low power mode, domain 1 can be switched off for power reduction. The **VDDIM** pin should be connected with a ceramic capacitor of at least 1µF. Do not overstep the maximum value of 4.7µF.

All **VDDI1** pins should be connected to each other. Each pin needs at least 470nF or 680nF ceramic capacitor (see table 3, 4). The maximum value of 2.2µF for each voltage domain 1 should not be overstepped. Please thinks about the tolerance of capacitors.

2.3 RESET

The pins **/ESR0**, **/ESR1** and **/ESR2** can serve as an external reset input as well as a reset output (open drain) for Internal Application and Application Resets.

By default the reset functionality of **/ESR1** and **/ESR2** is disabled, and an internal weak pull-up resistor is active. There is no special recommendation for the configuration for these pins.

The **/ESR0** is configured by default as a bi-directional pin with pull-up device. The **/ESR0** pin serves as an external reset output (open drain) as well as a reset input for Application Reset and Internal Application Reset. After reset, a short reset pulse (~20µs) is generated. An internal weak pull-up resistor is then active for **/ESR0**.

To reduce the noise sensitivity of **/ESR0** it is recommended to use either a block capacitor (100nF) to ground, or use an additional pull-up resistor to tie the pin to **VDDPB**. The reset function of **/ESR0** can be disabled in the register **RSTCON1**. The System Reset is not supported.

The supply voltage **VDDPB** is monitored to validate the overall power supply. The supply watchdog detects ramp-up or ramp-down of the external supply voltage and generates a power-on reset. Thanks to this module, only a simple low cost (3 pin device) voltage regulator is required. Up to 16 selectable threshold levels, from 2.9 Volts to 5.5 Volts allow monitoring of the external power supply and generates an interrupt or reset if specified.

It is recommended to use a pull-up resistor to tie **/PORST** to **VDDPB**. If an additional power on reset is requested the **/PORST** pin must be driven low. **/PORST** is equipped with a noise suppression filter that suppresses glitches below 10ns pulse width. **/PORST** pulses with a width above 100ns are safely recognized.

2.4 Startup Mode

To enter the startup mode **Internal Flash,** the **/TRST** pin needs to be tied to ground. To select different startup modes such as UART/SPI/CAN Bootstrap Loader, or to select Debug Modes, the **/TRST** pin needs to be tied to **VDDPB** and some dedicated pins on **Port10** have to be configured. Typically these modes are used to program the internal flash. The different modes can be triggered after a power-on reset or an application reset:

Table 1 Startup Mode

Startup Mode	Configuration Pins							
	/TRST	P10 (6:0)						
Internal Start from Flash	0	x	x	x	x	x	x	x
UART Bootloader (TxD = P7.3, RxD = P7.4) [1)]	1	x	x	x	x	1	1	0
SPI Bootloader (MRST = P2.4, MTSR = P2.3, SCLK = 2.5, SLS = 2.6)	1	x	x	x	1	0	0	1
CAN Bootloader (RxD = P2.6, TxD = P2.5)	1	x	x	x	1	1	0	1
External Start	1	1	1	1	0	0	0	0

Table 2 Debug Modes

Debug Mode (Internal Start from Flash)	Configuration Pins							
	/TRST	P10 (6:0)						
JTAG Default mode (P2.9, P5.2, P5.4, P7.0)	1	x	x	x	x	1	1	1
JTAG pos.B (P10.9, P10.10,P10.11,P10.12)	1	x	x	x	x	0	1	1
JTAG pos.C (P7.0, P7.2, P7.3, P7.4) [1)]	1	1	0	0	0	0	0	0
JTAG pos.D (P8.3, P8.4, P8.5, P10.12) [1)]	1	1	0	1	0	0	0	0
DAP pos. 0 (P2.9, P7.0)	1	x	x	x	0	0	0	1
DAP pos. 1 (P10.9, P10.12)	1	x	x	x	x	1	0	0
DAP pos. 2 (P7.0, P7.4) [1)]	1	x	x	x	0	1	0	1

Note: Some modes allow the re-routing of debug functionalities.

Note: For all configuration modes please refer to the user manual.

Note: [1)] Not available in 64 pin package

2.5 Start from Internal Flash

Figure 1 illustrates a possible configuration.

- The values for the oscillator circuit are dependent on the crystal type used.
- The “optional” resistors are required if the debug interface is used.

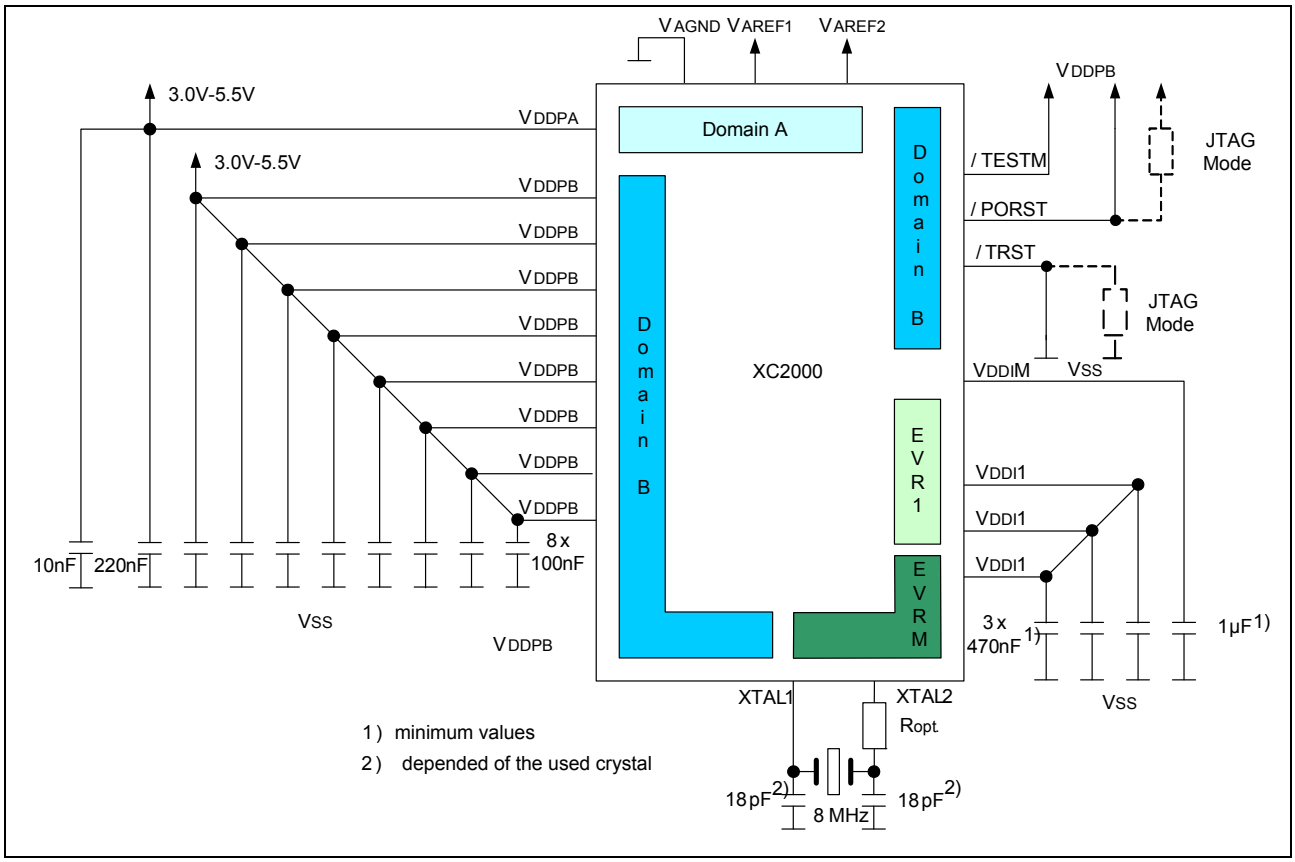

Figure 1 Start from Internal Flash (example XC22xxM)

Table 3 Decoupling Capacitor List(XC22xxM, XC22xxN, XC23xxA, XC23xxB, XC27x5X, XC27x4X, XE166M, XE166N)

Capacitor	Supply	Pins (QFP-144)	Pins (QFP-100)	Pins (QFP-64)
100nF	VDDPB	2	2	2
100nF	VDDPB	36	25	16
100nF	VDDPB	38	27	18
100nF	VDDPB	72	50	32
100nF	VDDPB	74	52	34
100nF	VDDPB	108	75	48
100nF	VDDPB	110	77	50
100nF	VDDPB	144	100	64
>= 1 µF	VDDIM	15	10	6
220nF	VDDPA	20	14	9
>= 470nF	VDDI1	54	38	24
>= 470nF	VDDI1	91	64	41
>= 470nF	VDDI1	127	88	57

Table 4 Decoupling Capacitor List (XC22xxH, XC22xxI, XC23xxC, XC23xxE, XC27x7X, XC27x8X, XE166H)

Capacitor	Supply	Pins (QFP-176)	Pins (QFP-144)	Pins (QFP-100)
100nF	VDDPB	2	2	2
100nF	VDDPB	44	36	25
100nF	VDDPB	46	38	27
100nF	VDDPB	88	72	50
100nF	VDDPB	90	74	52
100nF	VDDPB	132	108	75
100nF	VDDPB	134	110	77
100nF	VDDPB	176	144	100
>= 1 µF	VDDIM	17	15	10
220nF	VDDPA	22	20	14
>= 680nF	VDDI1	16	14	8
>= 680nF	VDDI1	66	54	38
>= 680nF	VDDI1	111	91	64
>= 680nF	VDDI1	155	127	88

Note: For a better power dissipation,a package with an exposed pad is offered. To reach the minimum thermal resistance Junction-Ambient (<= 22K/W), a 4-layer board with thermal vias should be used. The exposed pad needs to be soldered and tied to ground.

2.6 Debug Configuration

Figure 2 illustrates how a debug configuration can be realized. For configuration of a DAP (Device Access Port) interface, three pins are required. The debug mode becomes active after the rising edge of **/PORST** and with **/TRST** = 1.

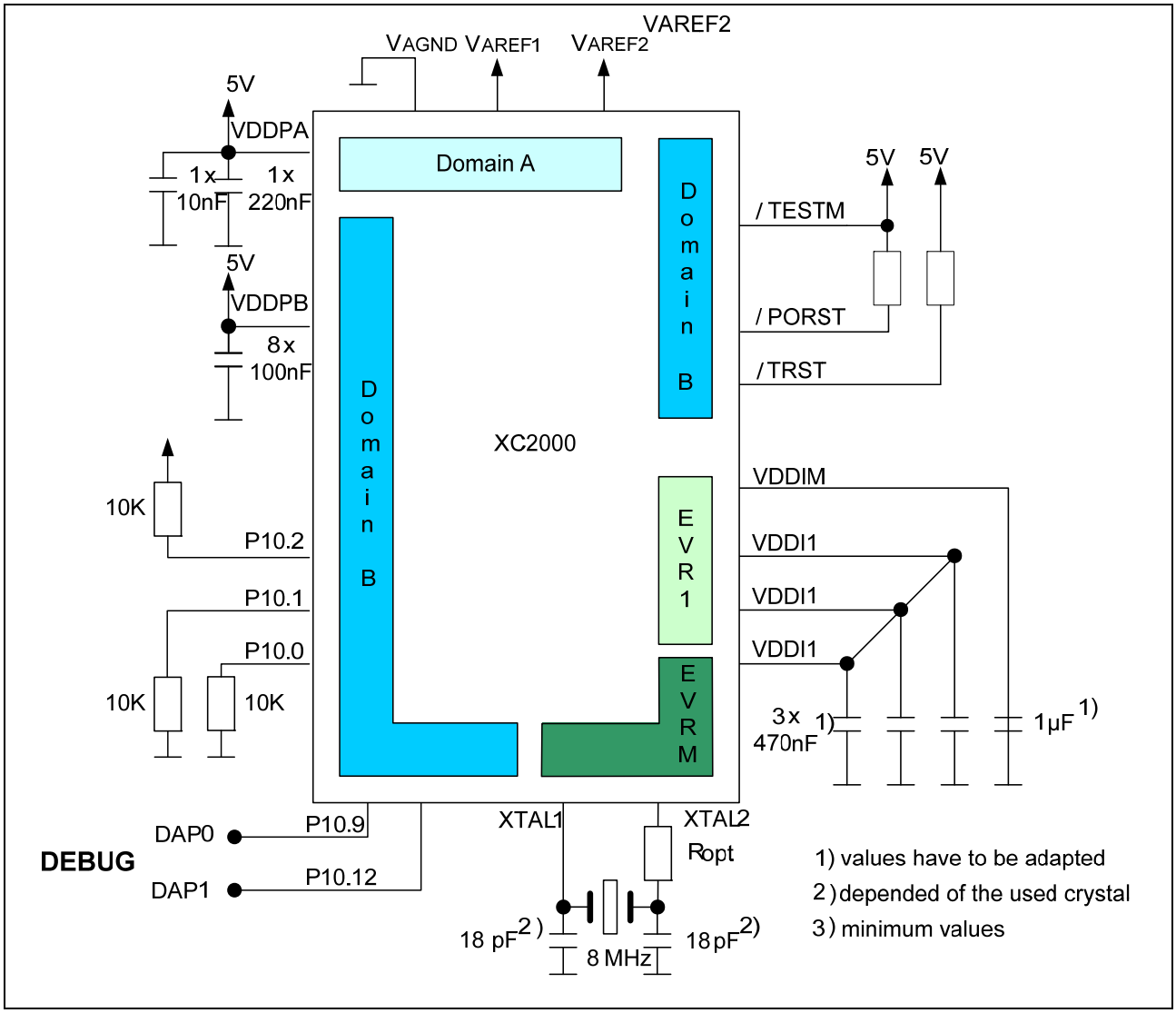

Figure 2 DAP Debug Configuration (example XC22xxM)

3 Power Supply

Monitoring the external power supply allows the use of a low-cost regulator without additional status signals.

This chapter discusses the following items:

- Single power supply
- Dual power supply

3.1 Single Power Supply

Typically, most systems need only one power supply. With the embedded voltage regulator and the supply watchdog, a 3 pin low cost voltage regulator meets all requirements.

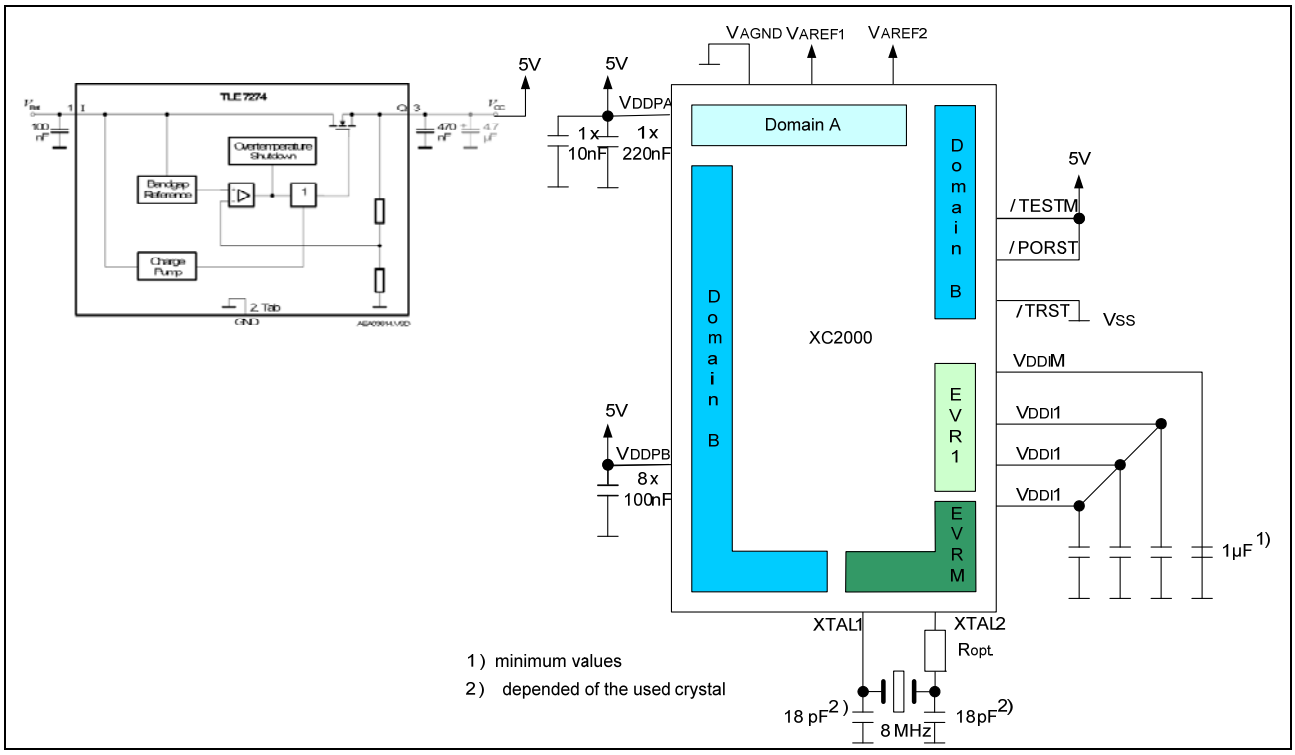

Figure 3 Single Power Supply using the TLE7274

The TLE 7274 is a monolithic integrated low-drop voltage regulator for load currents up to 300 mA. An input voltage up to 42 Volts is regulated to VQ, nom = 5.0 Volts, with a precision of ±2%. The stand-by current consumption is typically 20µA. Therefore the device is dedicated for use in applications which are permanently connected to VBAT.

If the system can be switched off completely the TLE 7276 can be chosen. This voltage regulator has an additional control pin (Inhibit) that disables the 5 Volt supply.

3.2 Dual Power Supply

Some applications require two external voltage domains. One reason for this can be that the board voltage supply is 3.3 Volts but some external components such as sensors, provide 5 Volt signals. The XC2000/XE166 family supports such requirements with their flexible voltage domain concept.

The digital supply voltage for domain B and the embedded voltage regulator is supplied with 3.3 Volts, the domain A is supplied with 5 Volts.

The domain B supplies all ports, except Port5, Port6 and Port15, with 3.3 Volts. To assure that both voltage sources are nearly synchronized, the inhibit functionality is used. The total power dissipation is explicitly reduced.

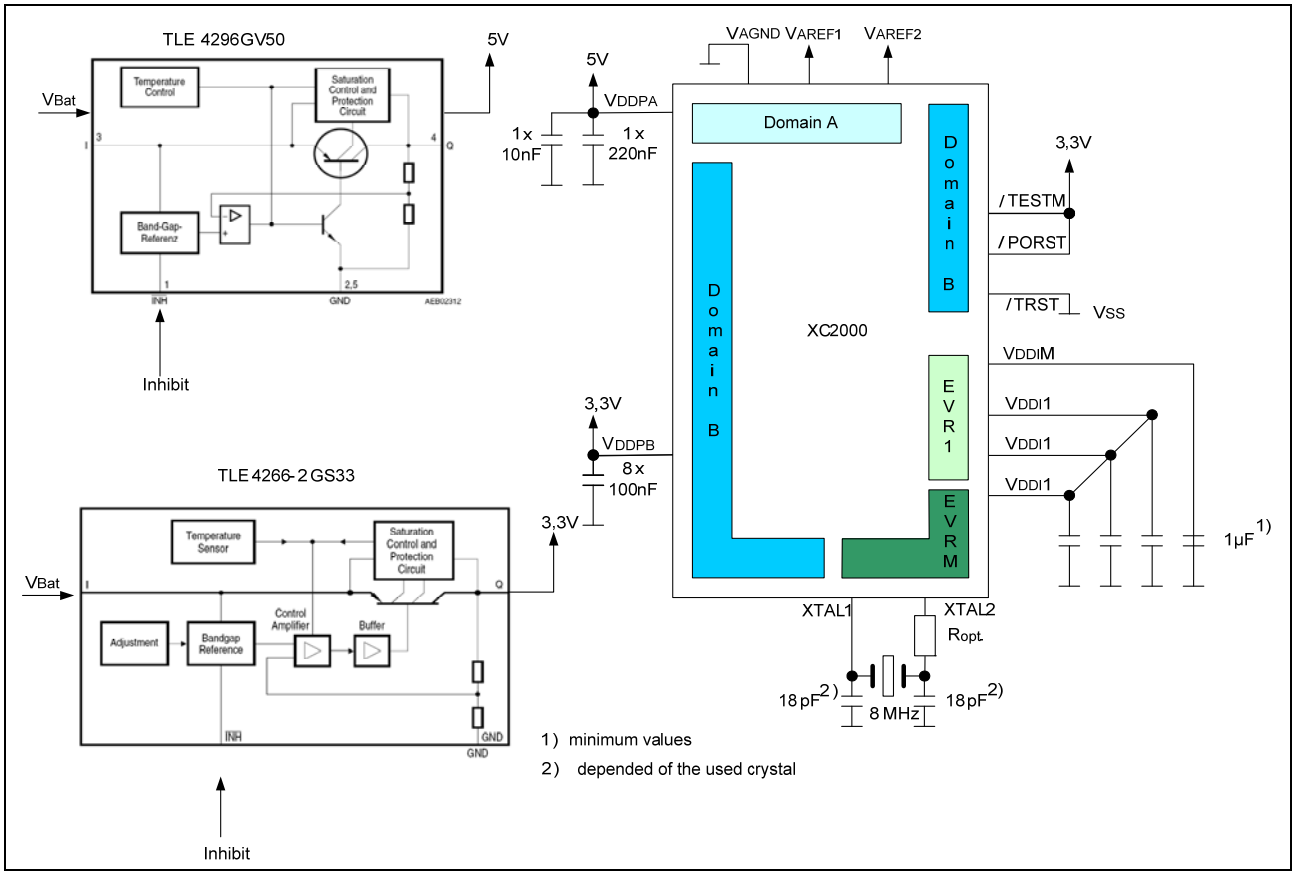

Figure 4 Dual Power Supply using TLE4296 GV 50 and TLE4266-2-GS33

The TLE 4296-2 G is a monolithic, integrated, low-drop voltage regulator in the very small SMD package P-SCT595-5. The output is able to drive a load of more than 30 mA while it regulates the output voltage within a 4% accuracy.

The **TLE 4266-2** is a monolithic, integrated, low-drop fixed voltage regulator which can supply loads up to 150 mA.

4 Special Reset Configurations

4.1 Using ESR Pins to Trigger a PORST Reset

In some Application Software or Hardware states (TRAPS or exceptional hardware events), a Power on Reset is required. Since the XC2000/XE166 can not trigger a **PORST** via software or internal Hardware, an external connection must be used.

The ESR pins serve as multi-functional pins with a wide range of different options, such as reset input/output. After power-on, **ESR0** is configured as reset input for an internal application reset in open drain mode. **ESR0** drives an active low signal after power-on for the time the internal reset counter is running (see Figure 6). For this reason **ESR0** can not be directly connected to the **/PORST** pin.

ESR1 and **ESR2** are configured after start-up as normal input pins, pull-up device activated. One of the two pins could be connected directly to the **/PORST** pin (Figure 5). To trigger a **PORST** the register **ESRCFG1** or **ESRCFG2** of the respective ESR pin needs to be written with the corresponding value for reset output drives; a 0 for an Internal Application or Application Reset in open drain mode. The Reset counter **RSTCNTA** in register **RSTCNTCON** should be set to the maximum value.

The ESR pin could also be used as an I/O pin, so that Software could trigger a PORST by setting the respective ESR pin to 0 to achieve a proper external reset pulse outside. If the Watchdog Timer (WDT) should trigger a PORST, the **ESRCFGx** register needs to be setup for the same type of reset as the WDT.

In some Applications with a higher Safety level, an external Supply Watchdog is used. Figure 5 shows that the **/RESETIN** of the Supply Watchdog can be used to trigger a PORST.

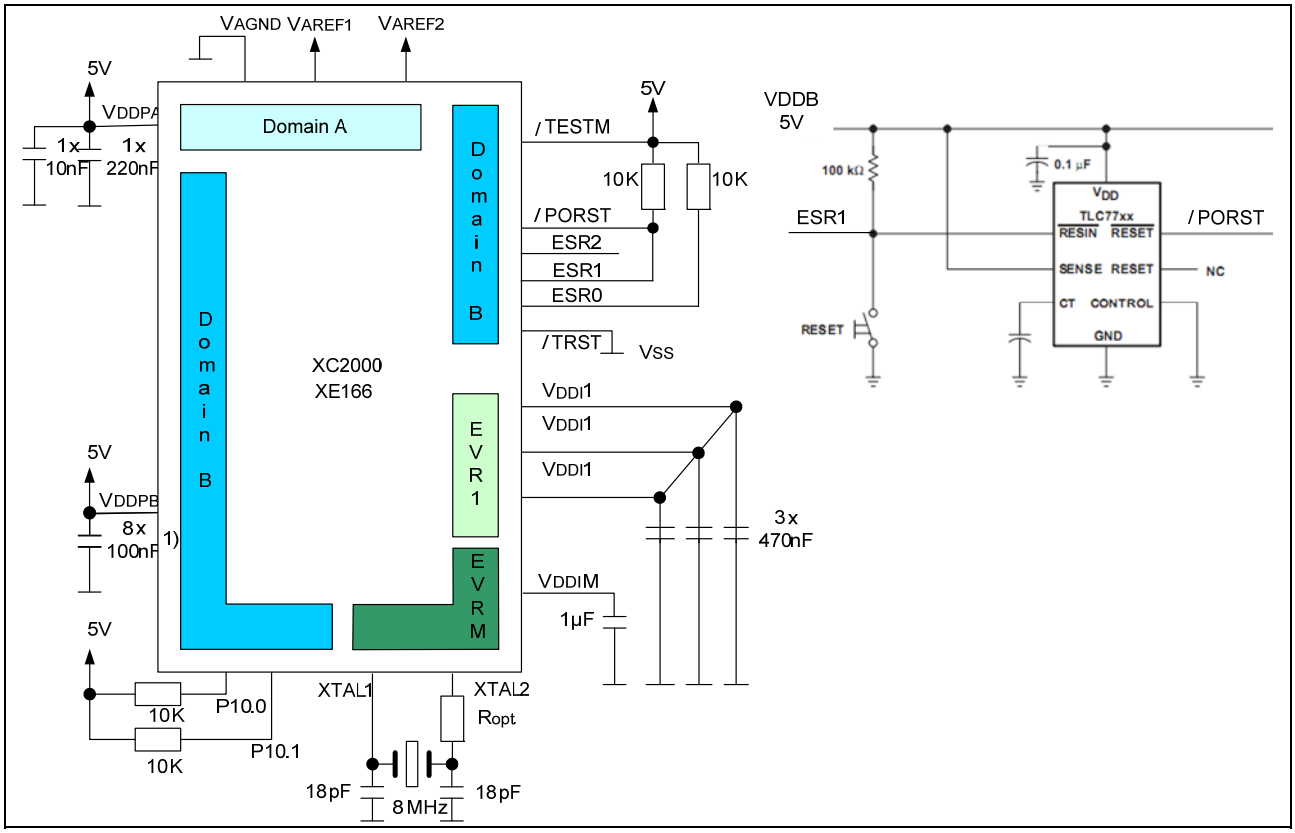

Figure 5 Trigger a PORST with the ESR1 Pin (Example XC22xx)

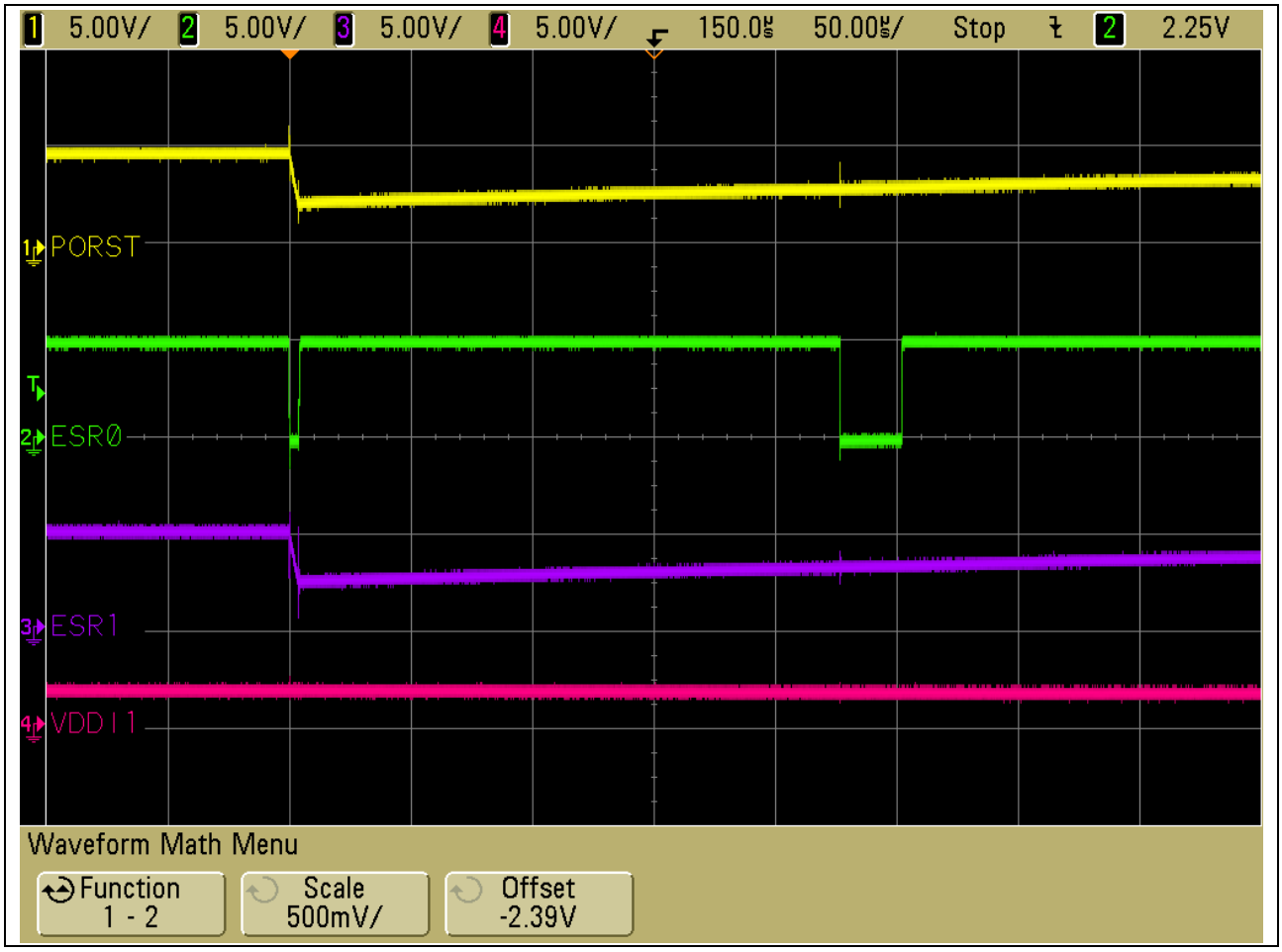

Figure 6 Trigger a PORST with the ESR1 Pin

Figure 6 show the ESR1 driving a low level during the WDT (WatchDog Timer) reset on the PORST pin. If the power-on reset is detected by the PORST pin, the ESR Pins switch to incative. The internal EVR are reset and the device boots up.

On the **ESR0** pin the short reset pulse (~20µs) is generated. An internal weak pull-up resistor is then active.

4.2 Using the ESR Pins to Generate a Reset Out (RSTOUT) Delay

Some Applications require a reset out signal together with a reset out delay after power-up, as long as the initialization is complete.

The former XC166 family had a special pin for this function, the **RSTOUT** pin (Figure 7).

The new XC2000/XE166 offers a wide range of reset functions but can also still be used in the same way as originally used in the XC166 16Bit family.

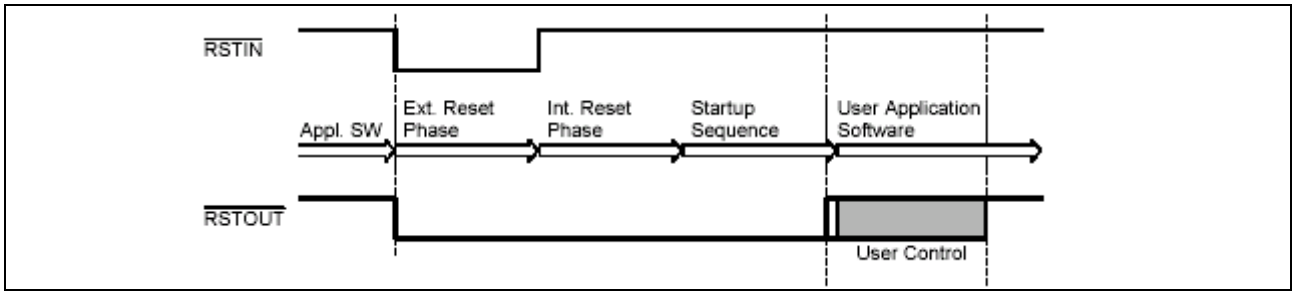

Figure 7 RESET Out of XC166 Family

The ESR pins serve as multi-functional pins with a wide range of different options, such as reset input/output. **ESR0** is configured as reset input (active low) after power-up. For this reason **ESR0** can not be used as the **RSTOUT** signal of the XC166 family shown in figure 7.

ESR1 and **ESR2** are configured after start-up as normal input pins, pull-up device activated. One of these pins can be used together with an external pull-down, to hold the signal at a low level. Later in the application software, the pin can be switched to push-pull output driving a high level. In Figure 8, the **SCU_ESRCFG1** was written with a 0x000A; at the end of system init.

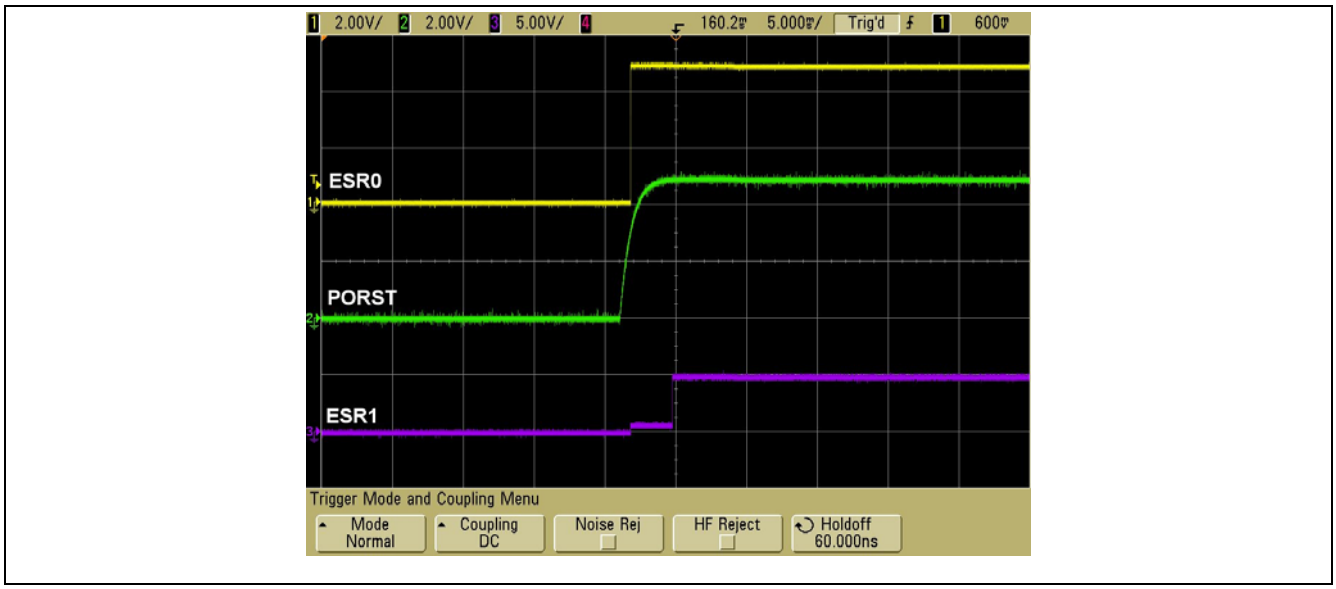

Figure 8 ESR1 as Reset Out Signal with Reset Out Delay after Power-up

5 Conclusion

The XC2000/XE166 family supports several powerful mechanisms to address different application scenarios, such as an embedded voltage regulator, power-on reset, two independent voltage domains and a supply watchdog.

Through the product ‘family’ concept, Infineon is able to offer a wide range of different devices to meet the diverse requirements in the market today and in the future.

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