Application Note, V1.1, September 2006

AP16099

# Scalable Pads

## Electrical Specification of Scalable Output Drivers in 250nm CMOS Technology

## XC166 Microcontroller Family

Microcontrollers

Never stop thinking.

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| 11 | Corrected “strong-soft” in Table 2 to “strong-sharp” | |
| 125 | Corrected strong-sharp driver assessment for driving a 35pF load at 15MHz | |
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# 1 Preface

Output driver scaling, also referred to as „slew rate control“, is an effective technique to reduce the electromagnetic emission of an integrated circuit by reducing the driver strength and/or smoothing the rising and falling edges of one or more pad output drivers.

Output driver scaling makes sense only when a certain margin regarding signal frequency and/or capacitive output load is available. Any driver scaling must maintain proper signal integrity.

This application note presents a huge set of output driver characterization data, which shall enable the system designers to select proper driver settings to reduce the electromagnetic emission caused by the driver switching, while maintaining the desired signal integrity. Parameters under consideration are switching frequency, capacitive output load, and ambient temperature.

Chapter 2 introduces physical basics behind the scaling.

Chapter 3 provides a set of measured rise/fall times under various conditions.

Chapter 4 documents rise/fall time simulations performed on PCB models of different signal routing structures.

Chapter 5 shows a set of measured electromagnetic emission under various conditions.

Chapter 6 discusses these emission results using a lot of comparison diagrams.

Chapter 7 recommends useful settings for the drivers by introducing signal categories and giving lots of decision tables and graphs.

The application note ends with a glossary.

*The data provided in chapter 7 should be preferrably referenced if a suitable pad driver setting is searched for a given signal data rate and a given capacitive load connected to this signal. This suitable pad driver setting leads to minimum electromagnetic emission under the given constraints for data rate and capacitive load.*

Chapters 3 to 6 serve as data pool for detailled timing and electromagnetic emission behaviour for all pad driver settings under various temperature and capacitve load conditions.

The information given in this application note is valid for Infineon microcontrollers of the XC166 Family, fabricated in 250 nm CMOS technology.

Please note that all numbers given in this application note are no specification values. They are verified by design without being monitored during the IC fabrication process. The numbers are based on timing measurements performed on center lot devices. Thus all values are subject to approx. 10% offset, depending on parameter variations such as fabrication process and pad supply voltages different from nominal conditions. The final selection of driver settings in system applications should consider this offset.

# 2 Introduction

Output driver scaling is introduced by setting corresponding control bits in registers. Fig. 1 shows an example of a pad driver control register, taken from the XC161 specification. While the location and function of the control bits may differ among the available Infineon microcontrollers, the electrical effects caused by these bits remain similar for a given technology.

## 2.1 Pad driver scaling in detail

### 2.1.1 Driver characteristics

Basically, we distinguish between driver control and edge control. Driver control bits set the general DC driving capability of the respective driver. Reducing the driver strength increases the output's internal resistance which attenuates noise that is imported/exported via the output line.

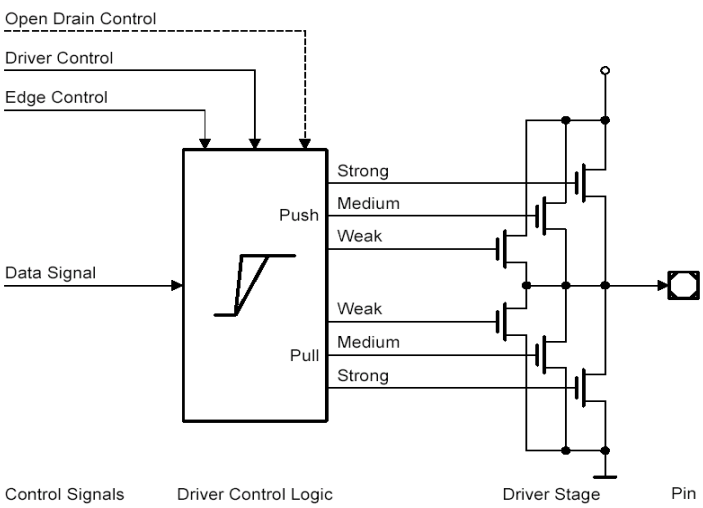


*Figure 1: Pad output driver schematic*

For a given external load, charging and discharging time varies with the driver strength, thus the rise/fall times will change accordingly. For driving LEDs or power transistors, however, a stable high output current may still be required independent of low toggle rates which would normally allow to decide for weak drivers due to their low transitions and thus low noise emission.

The controllable output drivers of the XC161 pins feature three differently sized transistors (strong, medium, and weak) for each direction (push and pull). The time of activating/deactivating these transistors determines the output characteristics of the respective port driver.

The strength of the driver can be selected to adapt the driver characteristics to the application's requirements:

In **Strong Driver Mode**, the medium and strong transistors are activated. In this mode the driver provides maximum output current even after the target signal level is reached.

In **Medium Driver Mode**, only the medium transistor is activated while the other transistors remain off.

In **Weak Driver Mode**, only the weak transistor is activated while the other transistors remain off. This results in smooth transitions with low current peaks (and reduced susceptibility for noise) on the cost of increased transition times, i.e. slower edges, depending on the capacitive load, and low static current.

**POCON***
**Port Output Ctrl. Reg.*** **ESFR ($F0xx_H/yy_H$)** **Reset Value: $0000_H$**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PDM3N | | | | PDM2N | | | | PDM1N | | | | PDM0N | | | |
| rw | | | | rw | | | | rw | | | | rw | | | |

| Field | Bit | Type | Description |
|---|---|---|---|
| PDMxN | [3:0], x = 0<br>[7:4], x = 1<br>[11:8], x = 2<br>[15:12], x = 3 | rw | **Port Driver Mode, Nibble x**<br>**Code, Driver strength[1], Edge Shape[2]**<br>0000 Strong driver, Sharp edge mode<br>0001 Strong driver, Medium edge mode<br>0010 Strong driver, Soft edge mode<br>0011 Weak driver, Standard edge[3]<br>0100 Medium driver, Standard edge[3]<br>0101 Reserved, do not use!<br>0110 Reserved, do not use!<br>0111 Reserved, do not use!<br>1xxx Reserved, do not use! |

1) Defines the current the respective driver can deliver to the external circuitry.
2) Defines the switching characteristics to the respective new output level. This also influences the peak currents through the driver when producing an edge, i.e. when changing the output level.
3) No additional edge shaping can be selected at this driver level.

*Figure 2: Port output control register example*

### 2.1.2 Edge Characteristics

This defines the rise/fall time for the respective output, i.e. the output transition time. Soft edges reduce the peak currents that are drawn when changing the voltage level of an external capacitive load. For a bus interface, however, sharp edges may still be required. Edge characteristic effects the pre-driver which controls the final output driver stage.

The Port Output Control registers POCONx provide the corresponding control bits. A 4-bit control field configures the driver strength and the edge shape. Word ports consume four control nibbles each, byte ports consume two control nibbles each, where each control nibble controls 4 pins of the respective port. Fig. 2 shows an example of a POCON register and the allocation of control bit fields and port pins.

In this guideline, the scaling effects of output drivers fabricated in 250nm CMOS technology is described. It serves as a reference addendum to the respective microcontroller product specifications where the individual bit settings can be found.

## 2.2 Physical basics

Two main constraints have to be met when deciding for a certain clock driver setting: signal integrity and power integrity. Both issues will be discussed after a general introduction to capacitive load charging.

### 2.2.1 Load charging

Generally, a switching transistor output stage delivers charge to its corresponding load capacitor during rising edge and draws charge from its load capacitor during falling edge. Timing diagrams normally show the signal's voltage over time characteristics. However, the resulting timing is a result of the electrical charge transfer described above. Charge is transferred by flowing current.

A bigger pad driver means a smaller resistance in the loading path of the external load. Fig. 3 shows the load current and voltage of two examples of pad drivers connected to a load of C=40pF. The strong driver has on output resistance of 25Ω, the weak driver 50Ω. For times t<0, the output voltage is 0V. At t=0, the load capacitor C is connected to the target output voltage U=5V via the respective driver pullup transistor. As a reaction, the load current steps immediately to the value I=U/R. I is bigger for smaller values of R. This means that the strong driver generates a bigger current jump and charges the load capacitor in a shorter time.

In time domain this leads to bigger reflections for not adapted driver impedances. Since typical trace impedances range from 60 to 120Ω , a strong driver with Z=10Ω is poorly adapted and may cause big voltage over- and undershoots. A weak driver with Z=100Ω may fit perfectly and generate a clean voltage switching signal without over- or undershoots. These effects are discussed in chapter 2.2.2.

In frequency domain, the current peak which is resulting from the charging of the load capacitor and from the over- or undershoots, causes significant RF energy and thus electromagnetic emission on the pad power supply. These effects are discussed in chapter 2.2.3.

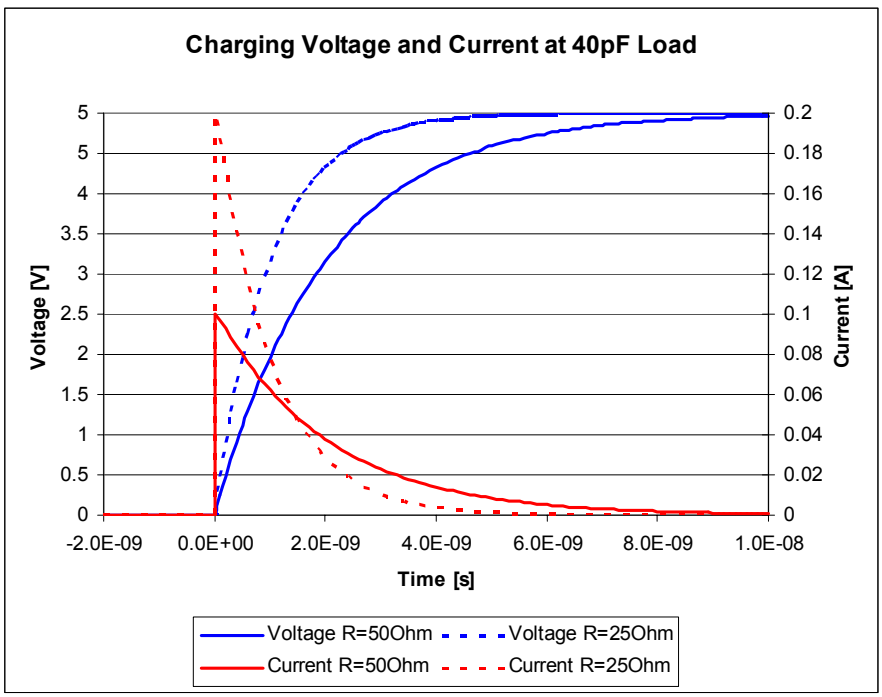


*Figure 3: Current-/voltage charging curves for different driver strengths*

Not only the pad driver impedance, but also the connected capacitive load determines the electromagnetic emission amplitudes. Fig. 4 illustrates the differences in charging current and voltage between a capacitive load of 40pF and one of 20pF. In both cases, the driver impedance is set to 50Ω.

As expected, the charging voltage increases faster for a smaller load. However, the starting value of the charging current is only determined by the driver impedance and is thus load-independent. The

load affects only the speed of load current decrease. It decreases faster if the load is smaller. This means on the other hand a bigger di/dt for smaller loads, resulting in higer emission for smaller loads.

This disadvantage can be compensated by chosing a smaller pad driver, i.e. a weaker driver setting, causing bigger driver impedance and thus smaller di/dt for the charging current.

The selection of a weaker driver setting slows down the pad switching time, so care must be taken to maintain the required signal integrity.

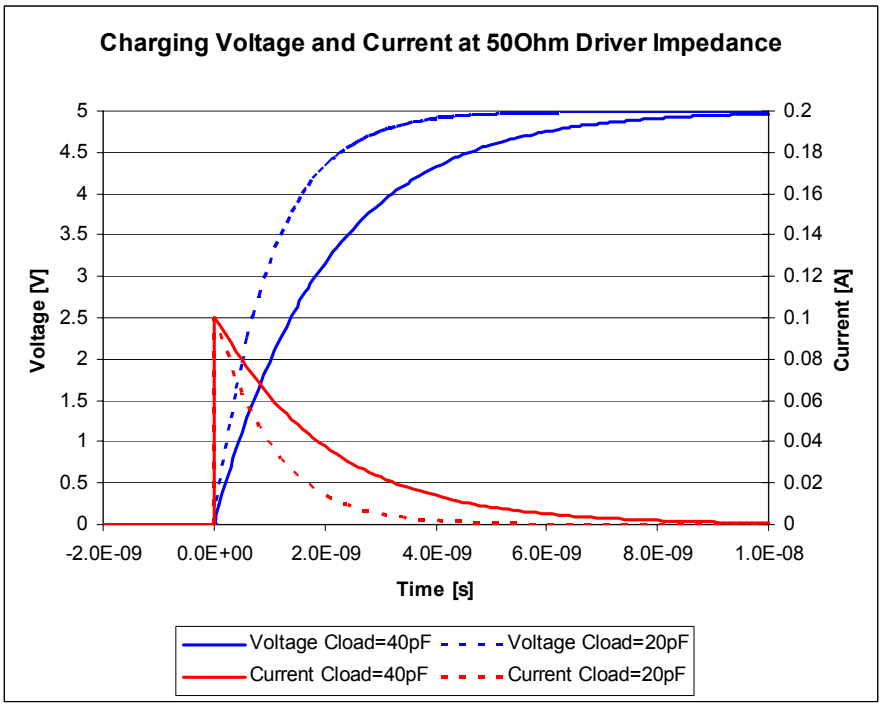


*Figure 4: Current-/voltage charging curves for different capacitive loads*

### 2.2.2 Signal integrity

Maintaining signal integrity means to select the rise/fall times such that all signal handshaking and data communication timing and levels are ensured for proper system operation. This means the data interchange between the microcontroller and external ICs like Flash memory, line drivers, receivers and transmitters etc. runs properly.

Therefore, it has to be taken into account that CMOS transistors become slower with rising temperature. Thus the timing of a critical signal has to be matched for proper operation at highest ambient temperature. Depending on the application, common temperature ranges are up to 85°C or up to 125°C. Several automotive control units specify an ambient temperature range from -40°C up to 125°C. The die temperature may reach values up to 150°C during operation.

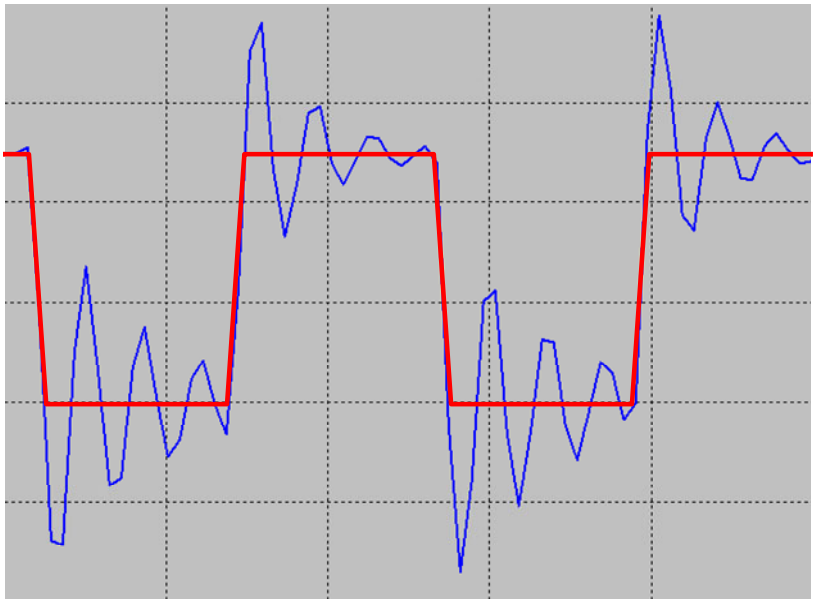

*Figure 5: Signal over- and undershoots*

Rules:

- Choose driver characteristics to meet the DC driving requirements. Make sure that the DC current provided by the microcontroller's pad drivers is sufficient to drive actuators into the desired logic state.
- Choose edge settings to meet system timing constraints at the highest system temperature. Make sure that no too strong driver settings are selected. This would lead to unnecessarily fast signal edges, causing two disadvantages regarding electromagnetic emission: (1) The slopes are too fast and cause undesired high emission energy at higher frequencies; (2) Over- and undershoot appears with the danger of latchup, spikes leading to wrong logic states or increased data stable delays and undesired high frequency emission.

- If system timing requires short signal rise/fall times, series termination is recommended to avoid over-/undershoot at signal transitions, see Fig. 5. The value of the termination resistor has to be chosen identical to the signal line impedance.

### 2.2.3 Power integrity / Electromagnetic emission

Any switching between low and high voltage levels generates RF noise. This happens whenever the switching voltage or the switching current has no sinusoidal shape. Switching currents are mainly responsible for electromagnetic emission because of the voltage drop across line inductances such as bond wires and lead frames. Any shapes other than sinusoidal are composed by the overlay of multiple frequencies, also known as harmonics. To reach a significantly steep edge of a trapezoidal voltage of a clock signal, short current pulses during the edges are required. These switching currents are outlined as nearly triangular peaks which are composed from the base frequency and a set of odd and even harmonics, depending on the exact pulse shape.

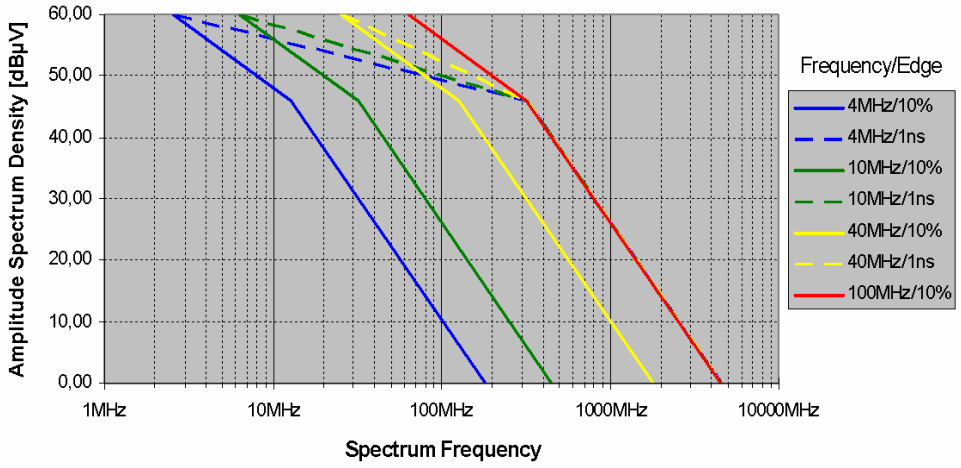


*Figure 6: Spectrum envelope for different clocks and edges*

The steeper a switching pulse is, the higher frequencies are required to form the rising and falling edges. A rise time of 1ns leads to a spectrum composed from harmonics up to at least 500 MHz.

A typical clock signal consists of 10% rise time, 40% high level, 10% fall time and 40% low level. Operating at 100MHz – equal to 10ns period time – this clock signal already generates at least harmonics up to 500MHz.

Unfortunately not the clock frequency, but the rise/fall times determine the resulting RF spectrum. Even if a clock driver operates at a relatively low toggle rate, it may generate the same RF spectrum as if it would operate at a significantly higher toggle rate – as long as its rise/fall times are not adjusted to the lower toggle rate by slowing down the transitions. For example, if the mentioned 100MHz clock driver operates at only 10 MHz, its rise/fall times should be extended from 1 ns to 10 ns, still maintaining the 10% ratio relatively to the clock period time. Fig. 6 illustrates that behaviour.

Rule:

- Choose driver and edge characteristics to result in lowest electromagnetic emission while meeting all system timing requirements at highest system temperature.

# 3 Measured Timings

## 3.1 Load conditions and ambient temperatures

The XC16x microcontroller family uses two types of pad drivers: CLKOUT serving as a timing reference signal provides stronger drivers than all other port pins. These other port pins are referred to as “General Purpose I/Os” (GPIO).

### 3.1.1 Measurement conditions used in this document

- A temperature range from $T_A$=25°C to $T_A$=150°C is covered for the timings. Please note that the IC operating conditions are specified from $T_A$=-40°C to $T_A$=125°C. Since switching times decrease with lower temperature, no timing problems should occur when an appropriate driver setting for high temperature has been selected. However, eventual over- or undershoot resulting from improper impedance matching between pad drivers and external load may increase at low temperature. The timing at $T_A$=125°C is a little bit faster than that documented in this guideline at $T_A$=150°C.
- If the user is interested in rise/fall time values at other temperatures, a linear interpolation between 25°C and 150°C can be done. For temperatures below 25°C, a linear extrapolation can be applied.
- Electromagnetic emission is always measured at $T_A$=25°C.
- The supply voltage for pad drivers is 5.0V for measurements at $T_A$=25°C.
- The supply voltage for pad drivers is 4.5V for measurements at $T_A$=150°C.

Load capacitors are selected in a way that together with the measurement probe capacitance of 8pF total capacitance values of 18pF up to 55pF are reached. Table 1 shows the reference between real loads and numbers given in the result diagrams. For easy reading, these capacitances are referred to as 20, 30, 40 and 50 pF in the result diagrams.

| Probe capacitance | SMD load capacitor | Resulting physical C | Referred capacitance |
|---|---|---|---|
| **8 pF** | **10 pF** | **18 pF** | **20 pF** |
| **8 pF** | **22 pF** | **30 pF** | **30 pF** |
| **8 pF** | **33 pF** | **41 pF** | **40 pF** |
| **8 pF** | **47 pF** | **55 pF** | **50 pF** |

Table 1: Overview of capacitive loads used for timing measurements

The result diagrams show the measured rising and falling edge timing using an oscilloscope probe of 8pF||1MΩ. The reference points are 10% and 90% as indicated in Fig. 7.

For measurements at $T_A$=150°C, the pad supply voltage VDDP has been decreased to 4.50V (nominal VDDP minus 10%). Thus the voltage levels references for timing measurements at $T_A$=150°C are: 0.45V (low reference) and 4.05V (high reference).

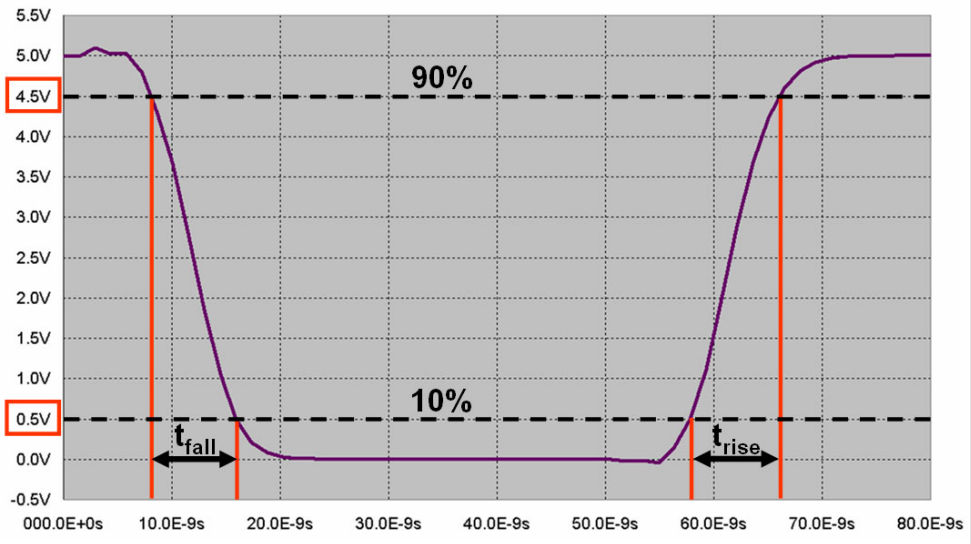


*Figure 7: Voltage level references for timing measurement*

### 3.1.2 Measured rise and fall times

The following diagrams show the 10-90% rise times and 90-10% fall times of all CLKOUT and GPIO driver strengths at $T_A$=25°C and $T_A$=150°C. The physically connected load capacitor values are according the “Referred capacitances” listed in Table 1. The abbreviations used for driver strangth and load description are listed in Table 2. The respective load capacitor is connected close to the pin of the CLKOUT or GPIO driver pin. It is connected from the pin to GND. GPIO measurements have been done at Port 3.13 of the XC161CS and are valid for all other GPIO pins of the XC166 Family members fabricated in 0.25µm CMOS technology.

In Fig. 8-13 the rise and fall times are given for CLKOUT and GPIO set to different driver strengths. Fig. 14-23 extrapolate the measurement temperatures of 25°C and 150°C down to -40°C in a linear way (which reflects reality with good approximation).

| Abbreviation | Driver strength | Resulting physical capacitor |
|---|---|---|
| SSH-20pF | Strong-sharp | 18 pF |
| SSH-30pF | Strong-sharp | 30 pF |
| SSH-40pF | Strong-sharp | 41 pF |
| SSH-50pF | Strong-sharp | 55 pF |
| SME-20pF | Strong-medium | 18 pF |
| SME-30pF | Strong-medium | 30 pF |
| SME-40pF | Strong-medium | 41 pF |
| SME-50pF | Strong-medium | 55 pF |
| SSO-20pF | Strong-soft | 18 pF |
| SSO-30pF | Strong-soft | 30 pF |
| SSO-40pF | Strong-soft | 41 pF |
| SSO-50pF | Strong-soft | 55 pF |
| MED-20pF | Medium | 18 pF |
| MED-30pF | Medium | 30 pF |
| MED-40pF | Medium | 41 pF |
| MED-50pF | Medium | 55 pF |
| WEA-20pF | Weak | 18 pF |
| WEA-30pF | Weak | 30 pF |
| WEA-40pF | Weak | 41 pF |
| WEA-50pF | Weak | 55 pF |

Table 2: Abbreviations used in the timing result diagrams

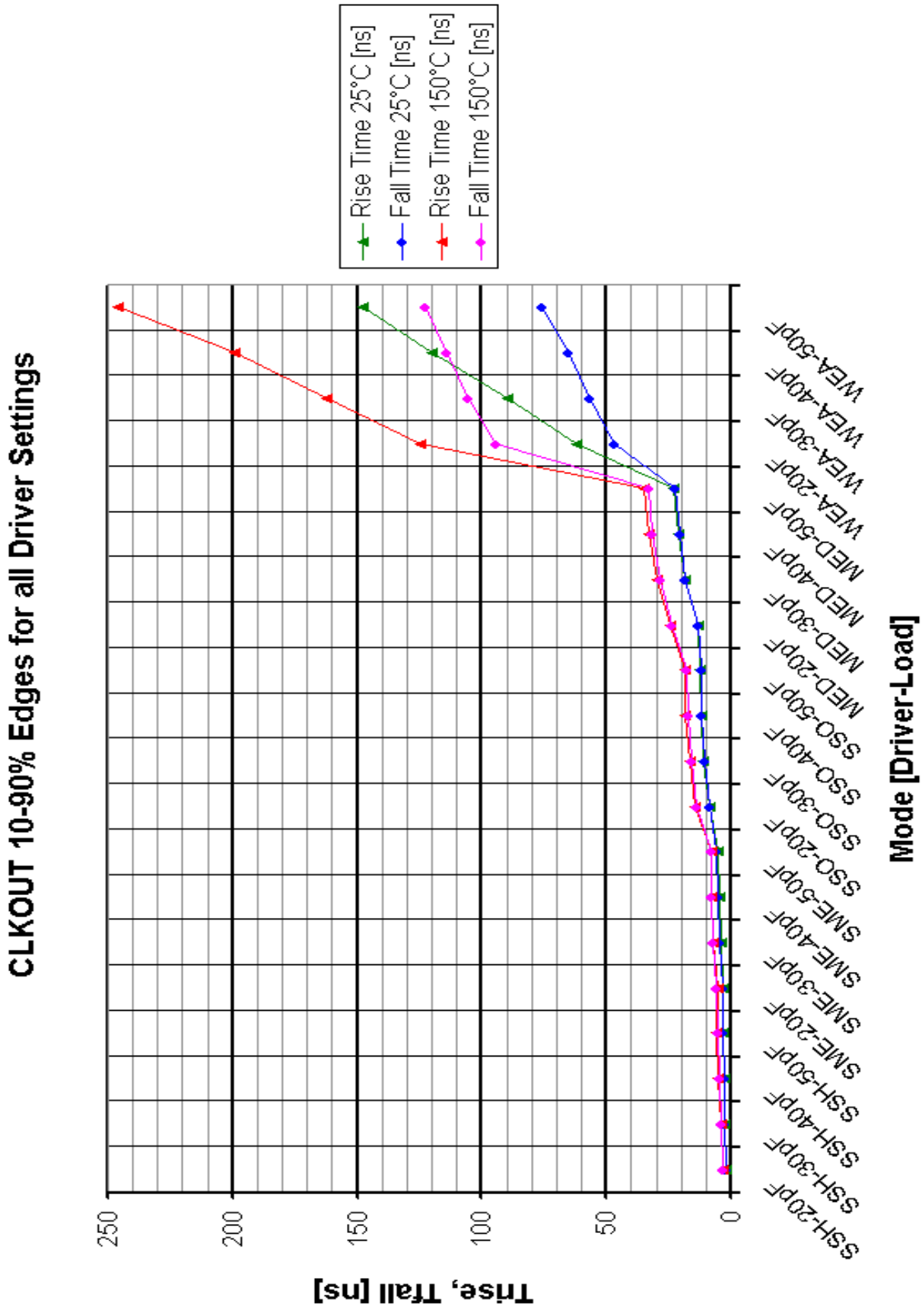


*Figure 8: Timings CLKOUT for all driver settings*

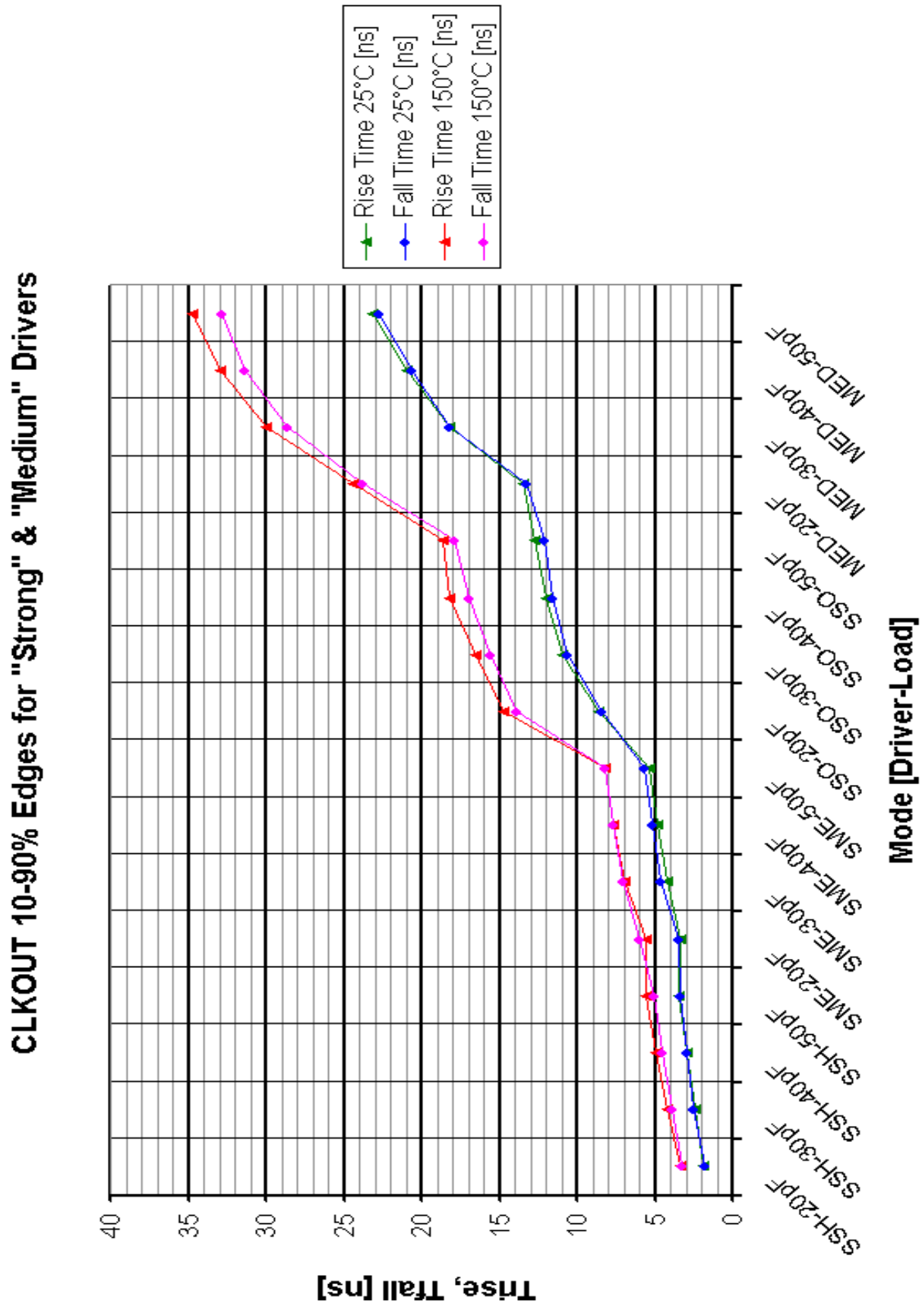


*Figure 9: Zoomed timings CLKOUT for strong and medium driver settings*

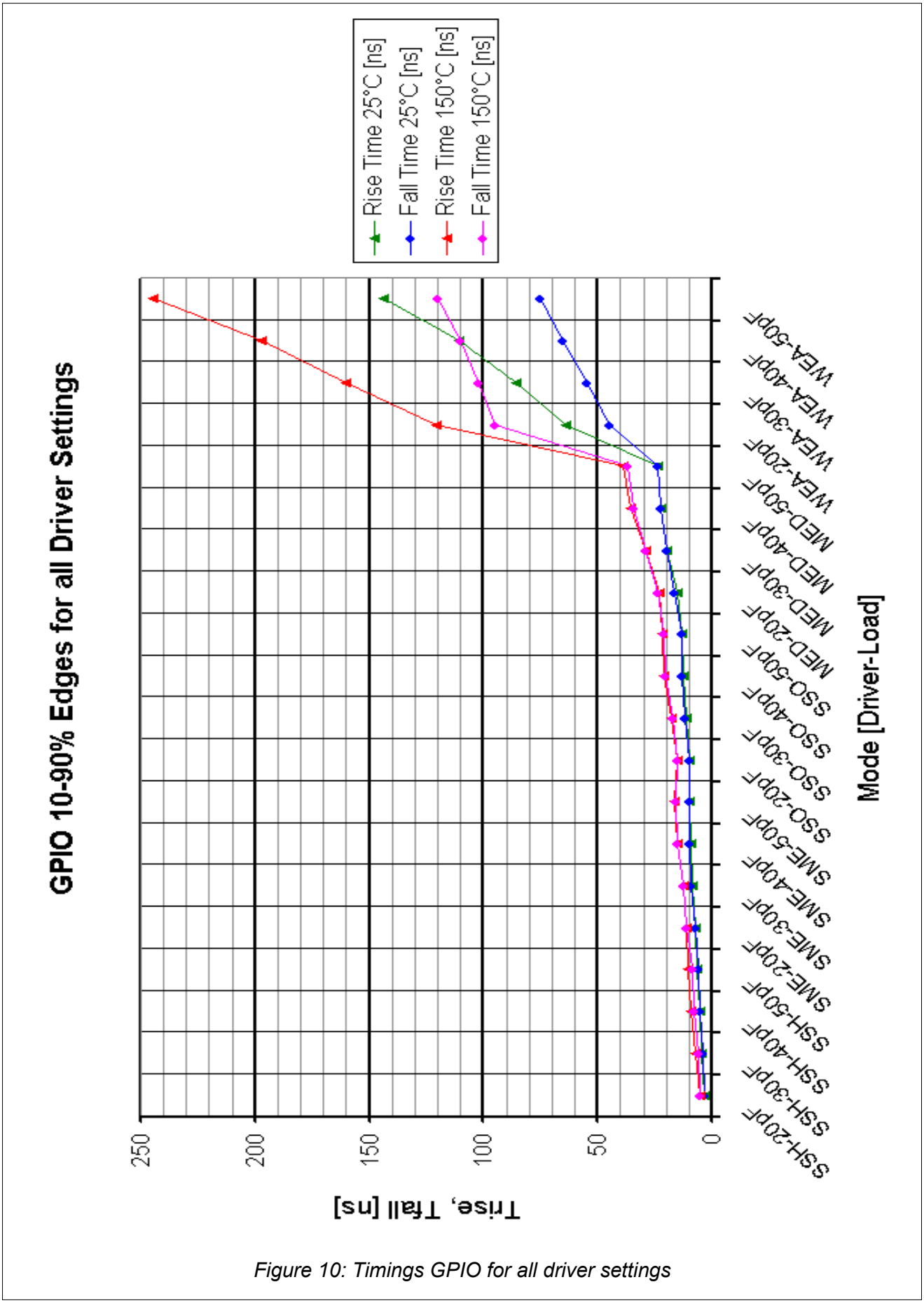


*Figure 10: Timings GPIO for all driver settings*

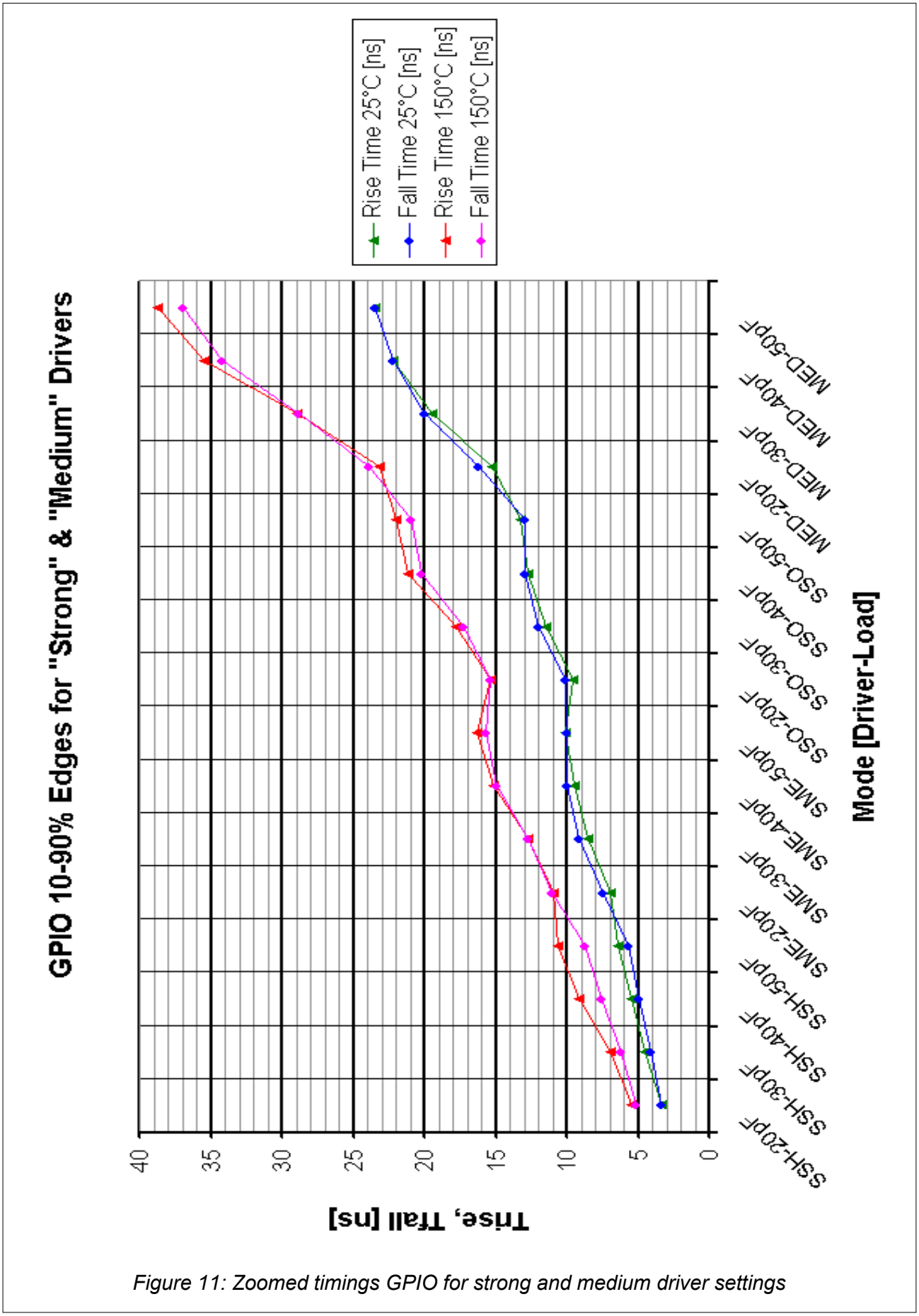


*Figure 11: Zoomed timings GPIO for strong and medium driver settings*

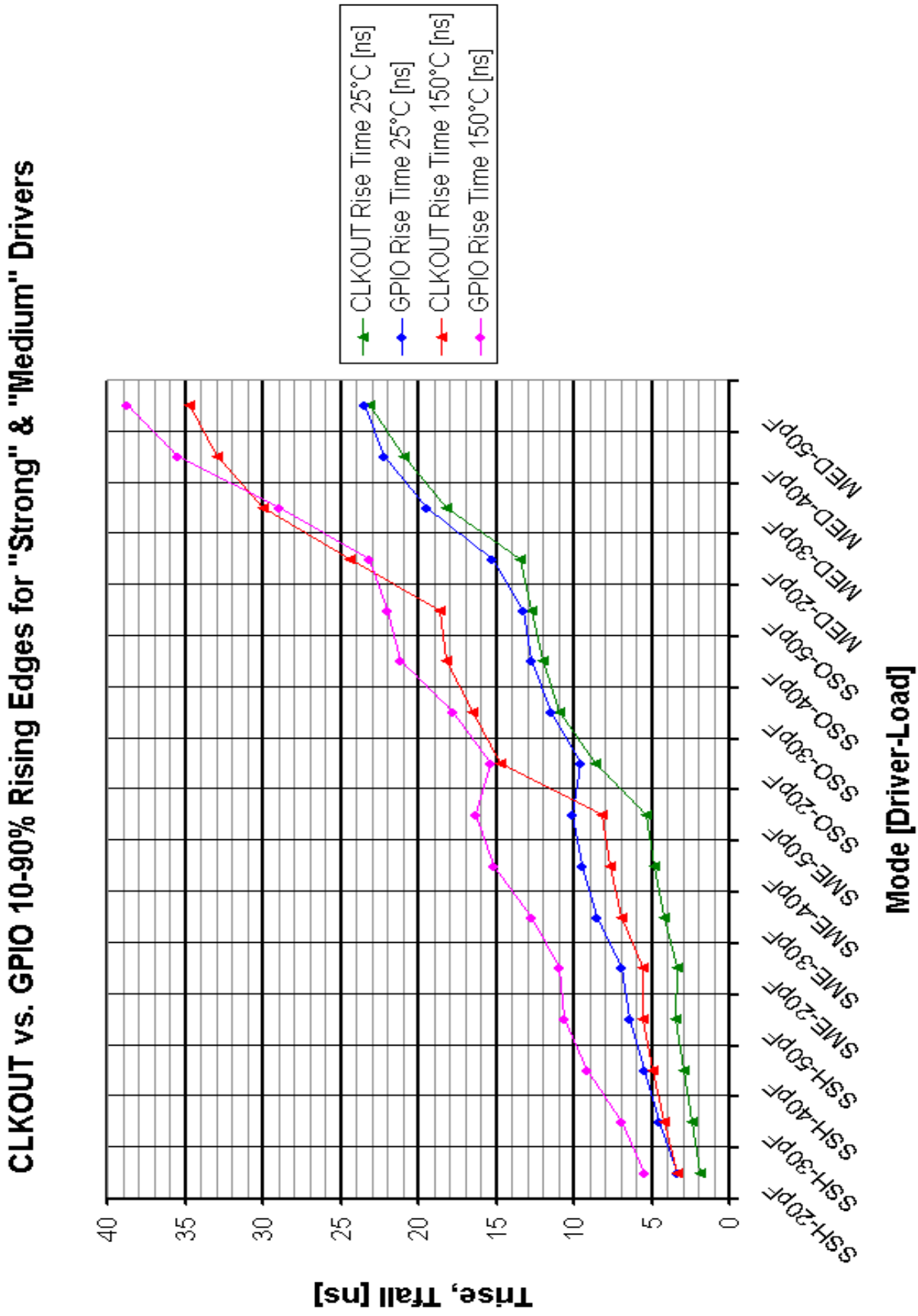


*Figure 12: Zoomed rise times CLKOUT and GPIO for strong and medium driver settings*

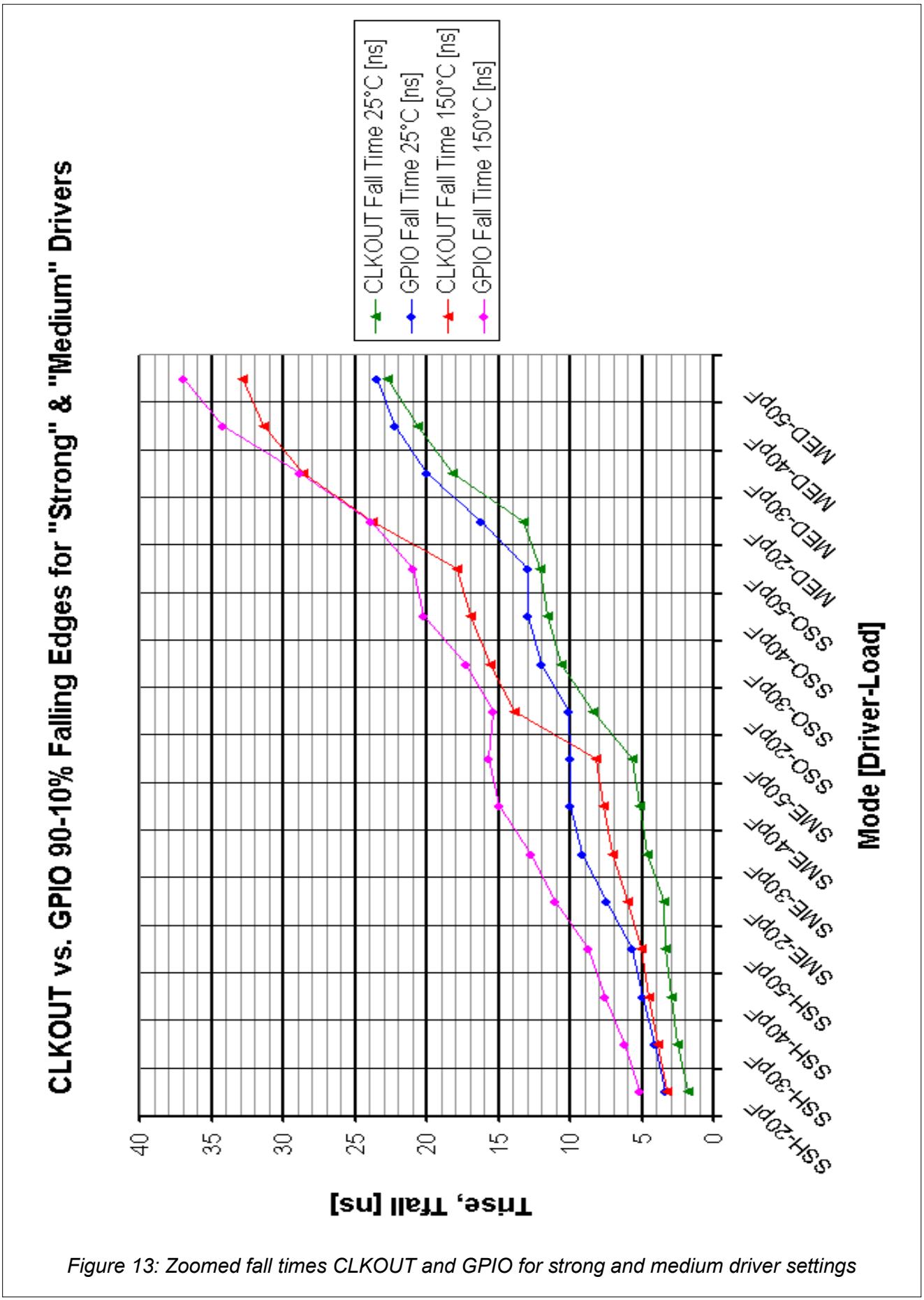


*Figure 13: Zoomed fall times CLKOUT and GPIO for strong and medium driver settings*

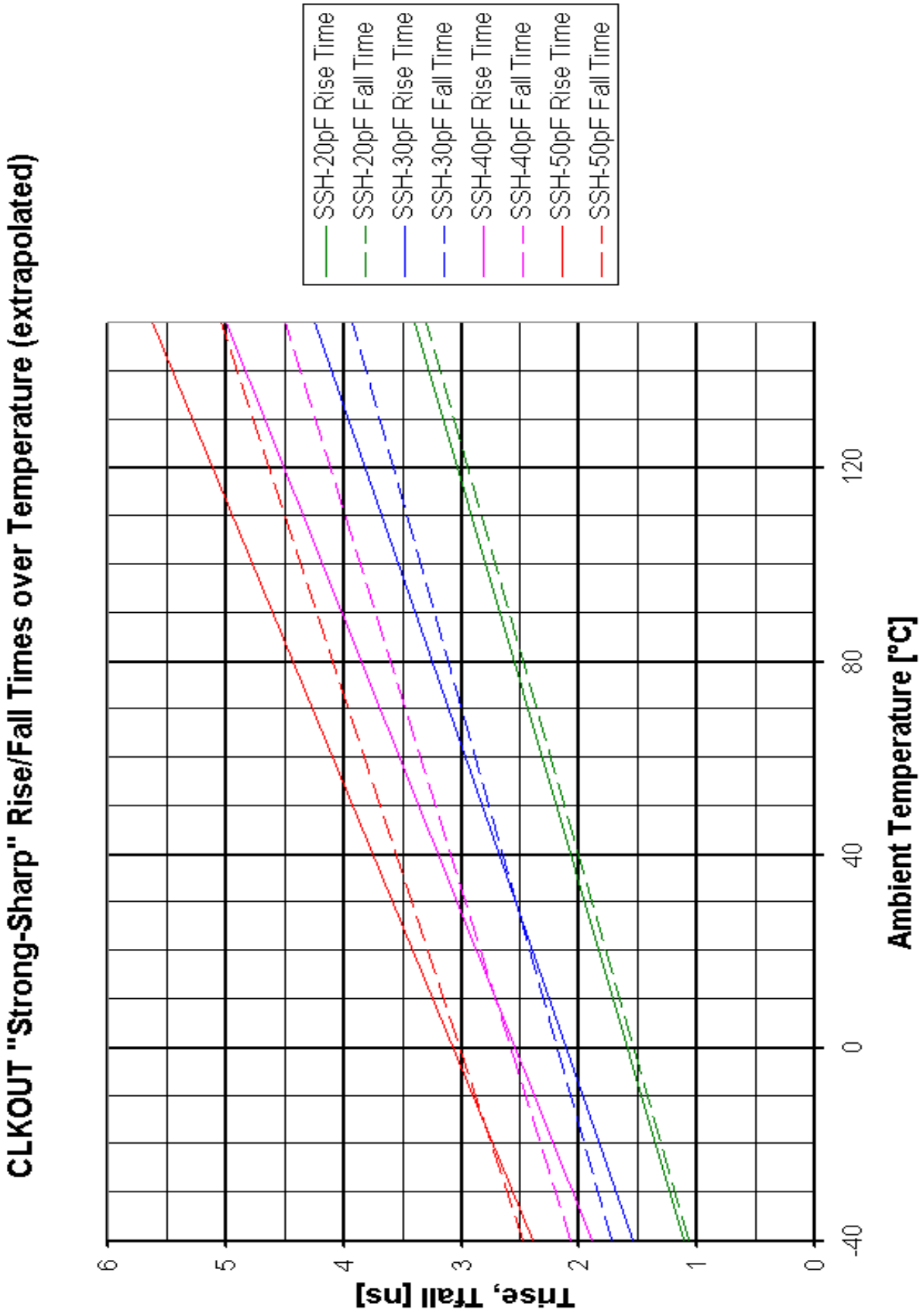


*Figure 14: CLKOUT "strong-sharp" driver rise/fall times over full ambient temperature range*

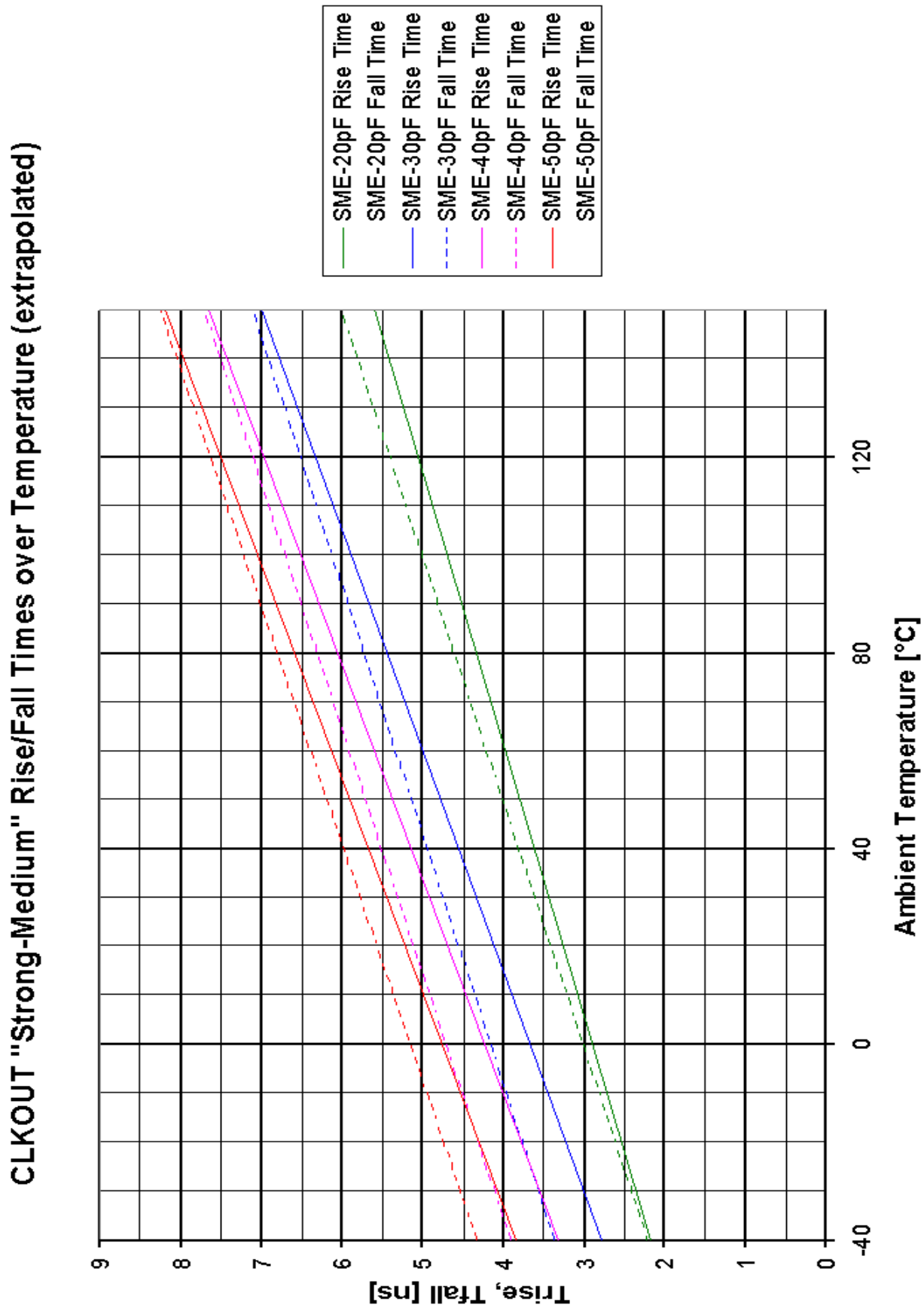


*Figure 15: CLKOUT "strong-medium" driver rise/fall times over full ambient temperature range*

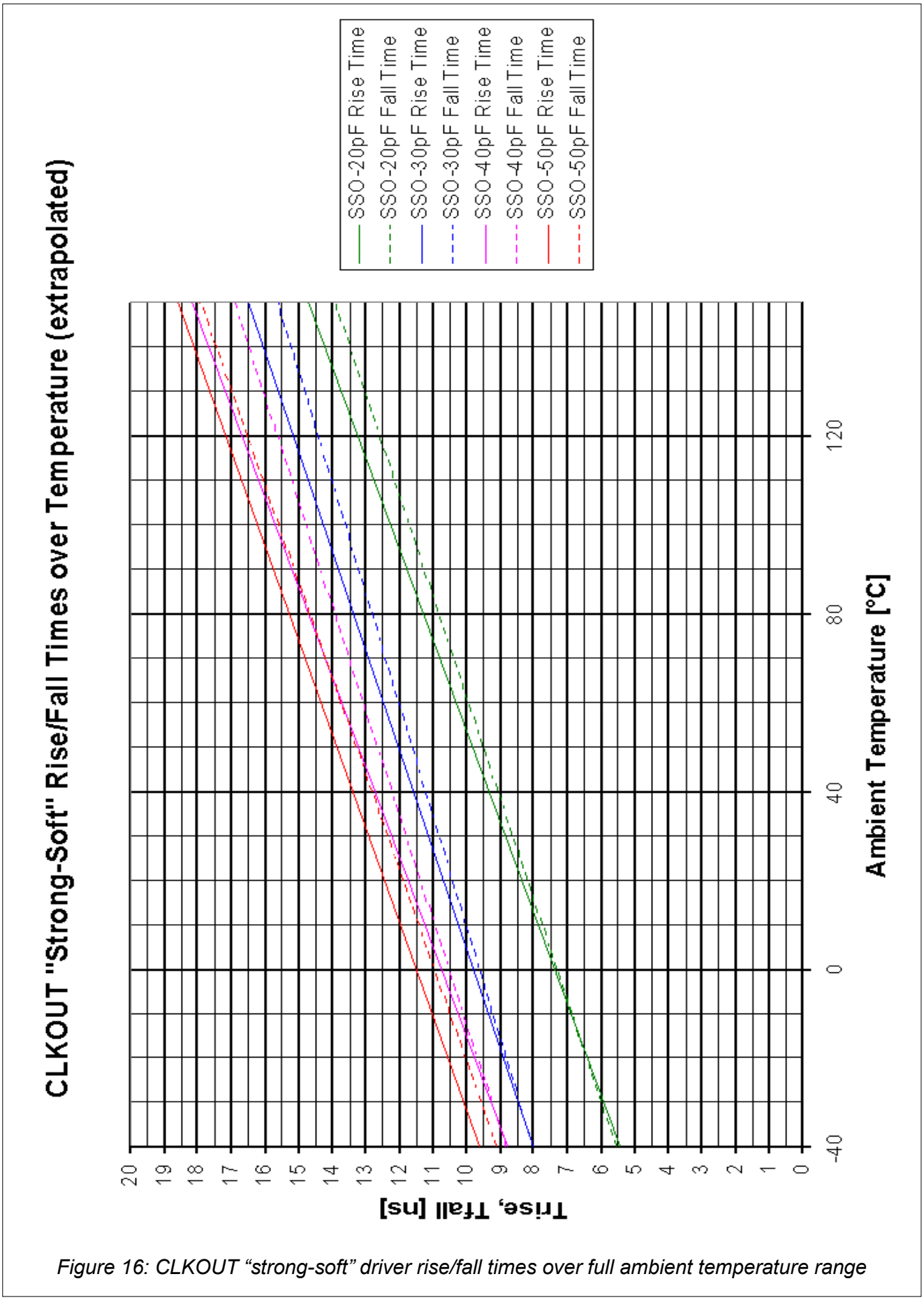


*Figure 16: CLKOUT "strong-soft" driver rise/fall times over full ambient temperature range*

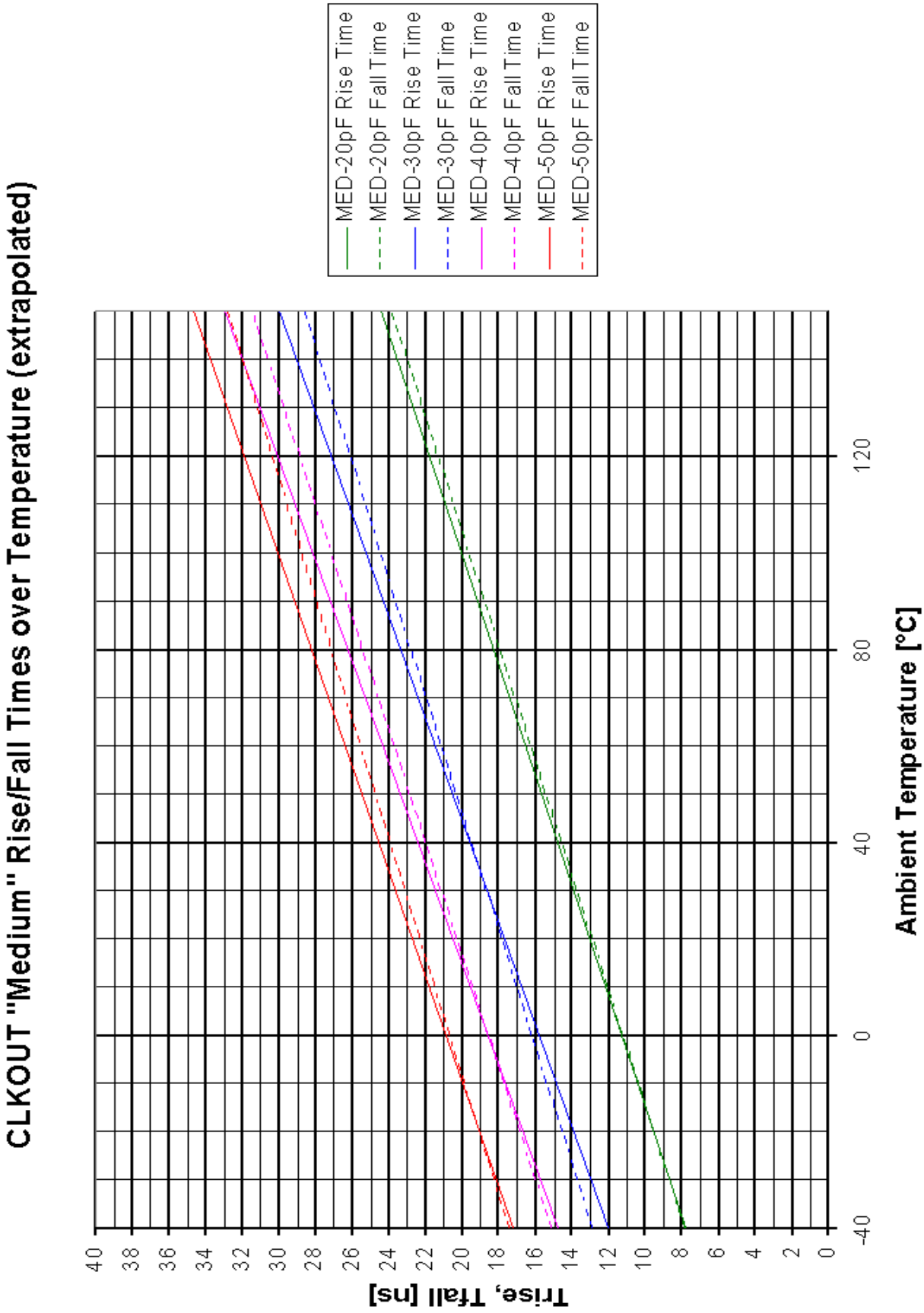


*Figure 17: CLKOUT "medium" driver rise/fall times over full ambient temperature range*

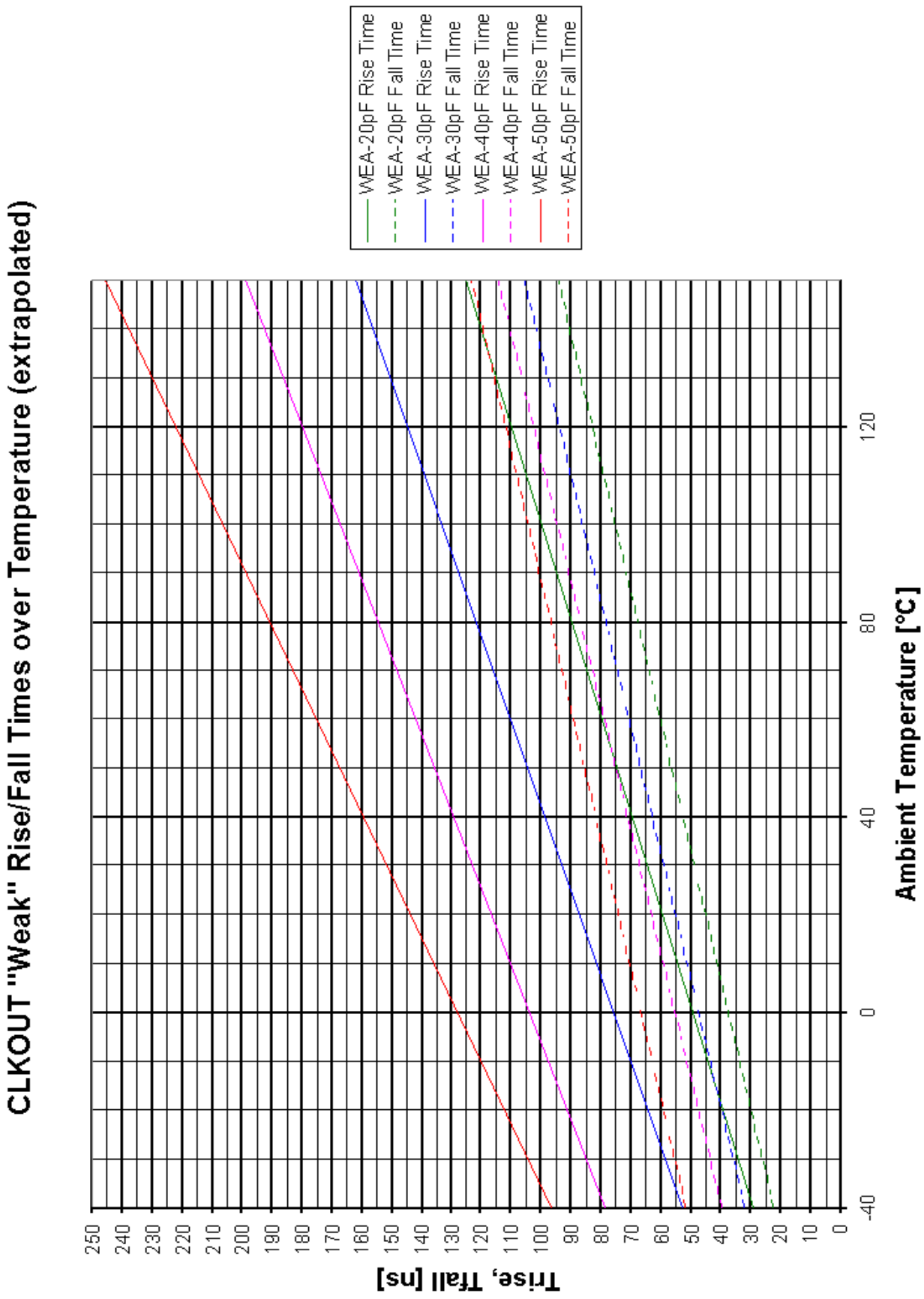


*Figure 18: CLKOUT "weak" driver rise/fall times over full ambient temperature range*

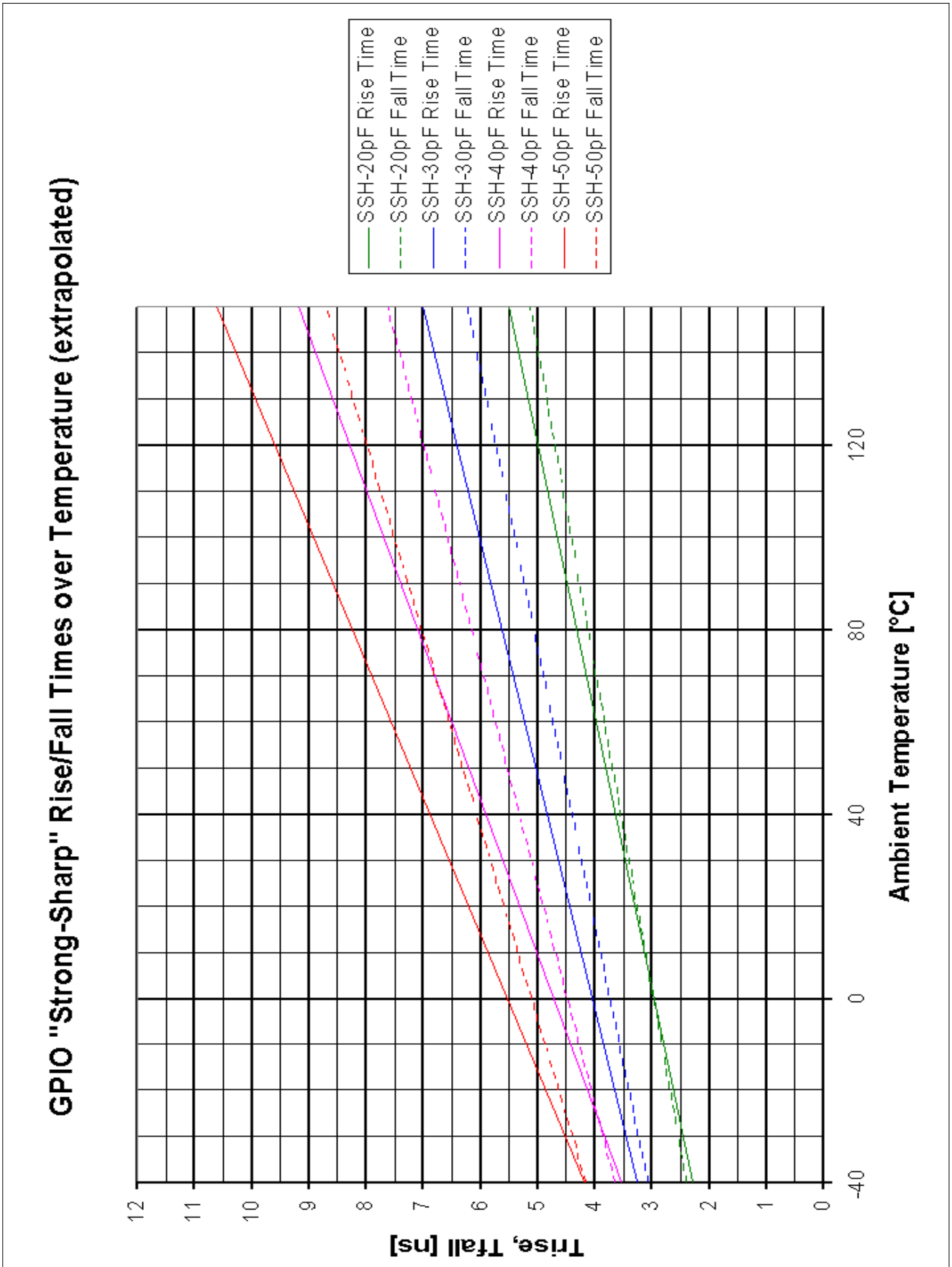


*Figure 19: GPIO “strong-sharp” driver rise/fall times over full ambient temperature range*

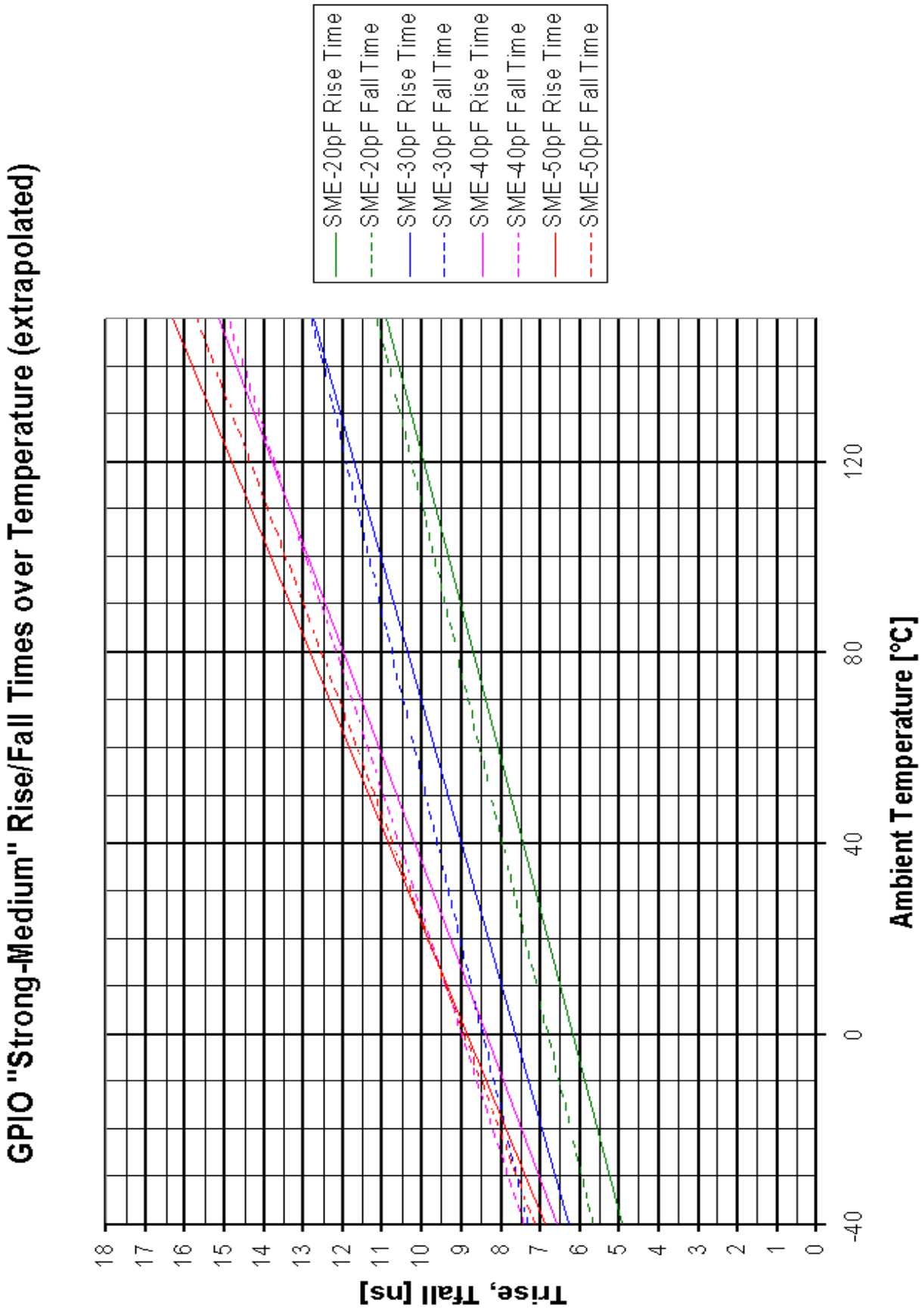


*Figure 20: GPIO "strong-medium" driver rise/fall times over full ambient temperature range*

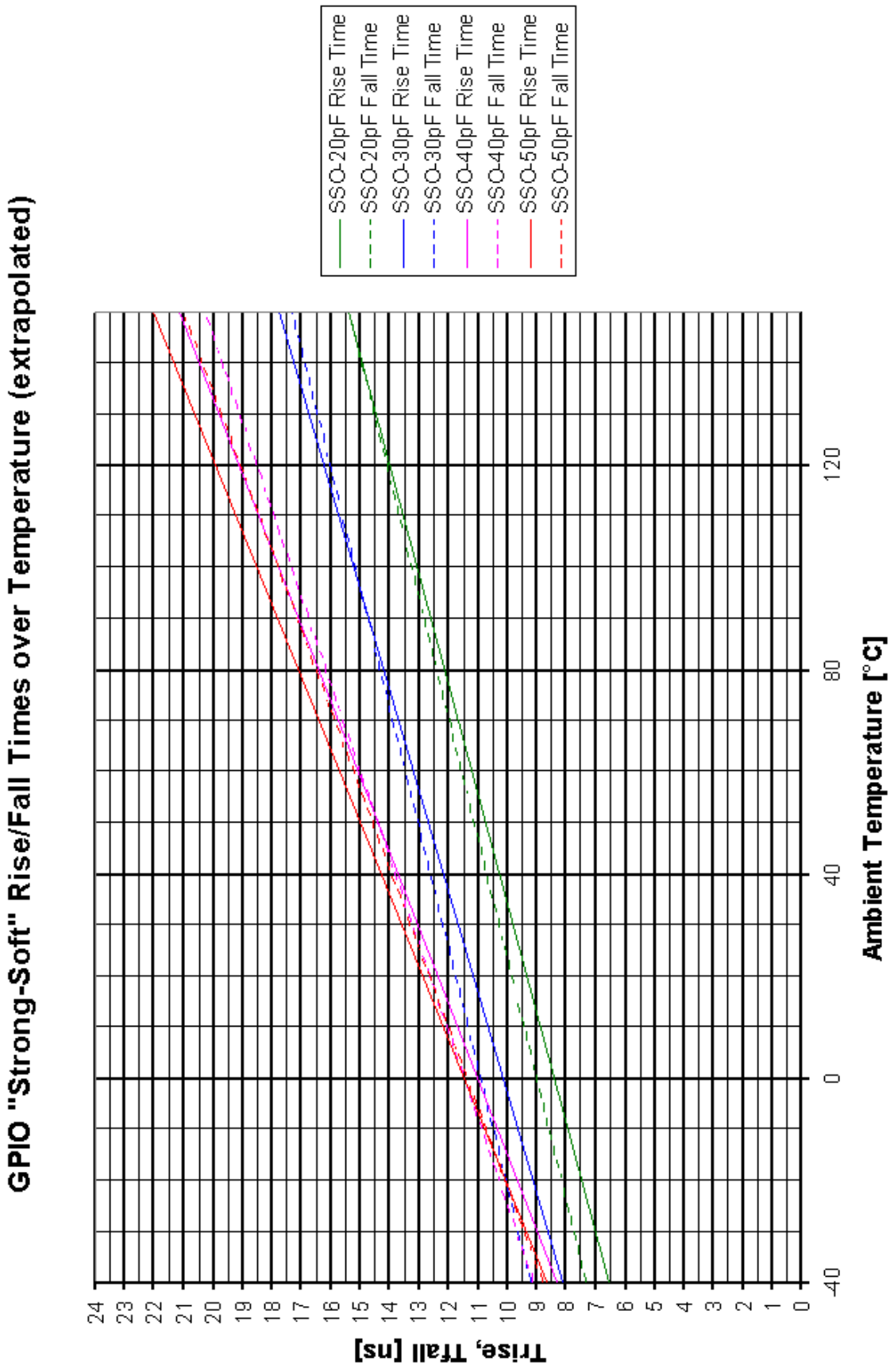


*Figure 21: GPIO "strong-soft" driver rise/fall times over full ambient temperature range*

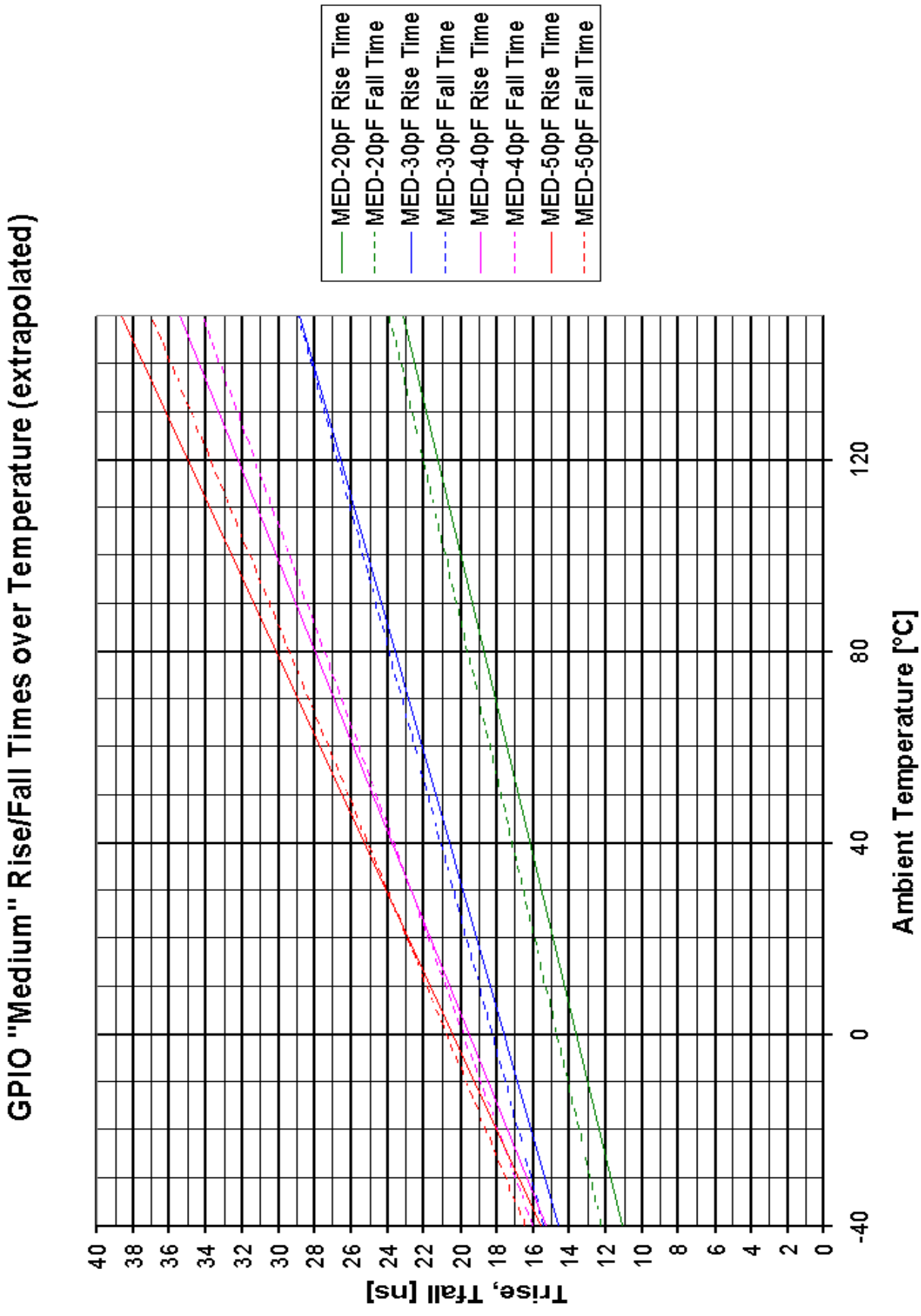


*Figure 22: GPIO "medium" driver rise/fall times over full ambient temperature range*

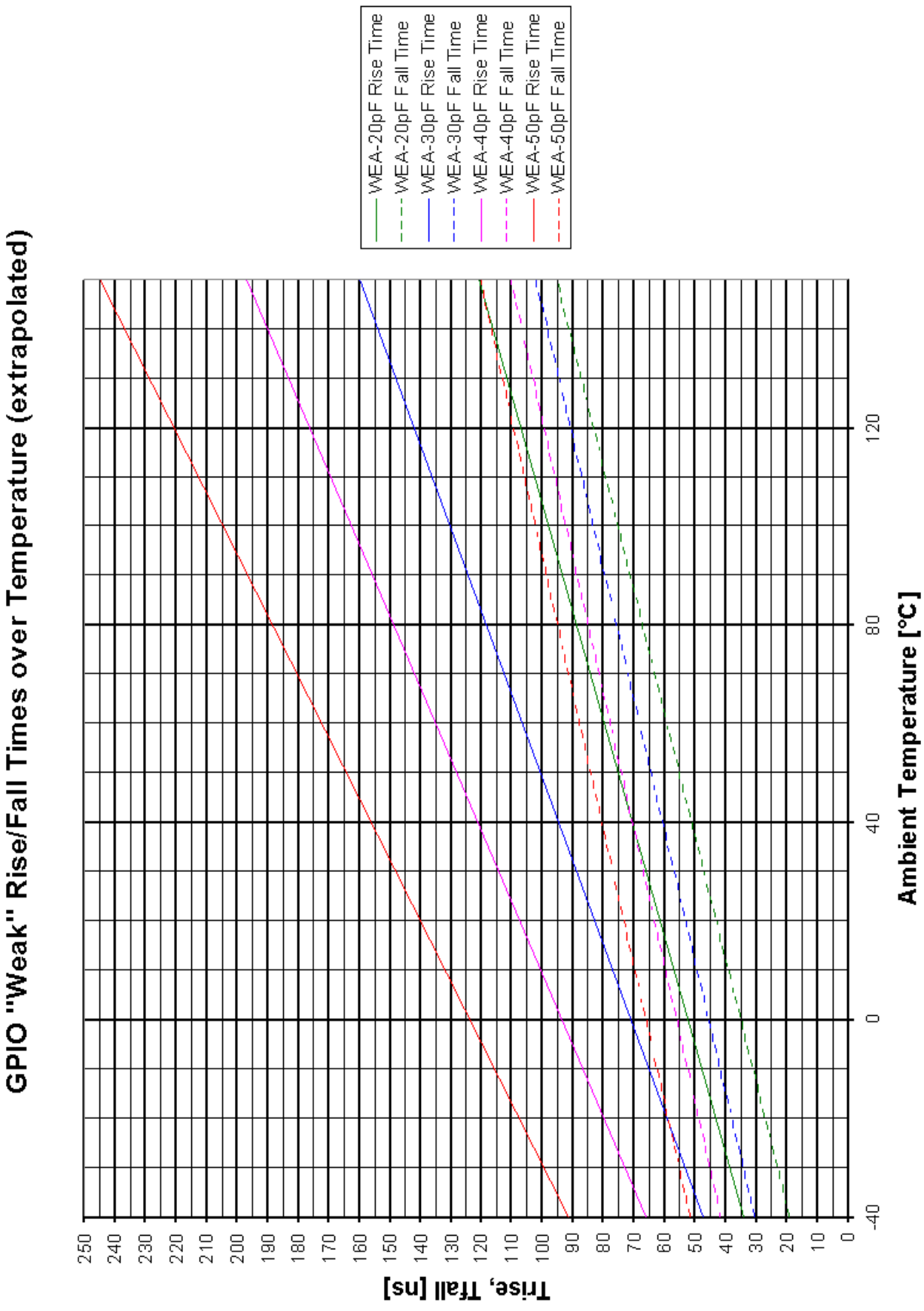


*Figure 23: GPIO "weak" driver rise/fall times over full ambient temperature range*

# 4 Simulated Timings

## 4.1 Simulated timings on selected PCB trace structures

### 4.1.1 Description of structures

A temperature range from $T_A$=25°C to $T_A$=150°C is covered for the timings. Please note that in addition to the measured timings, which use discrete load capacitors, it is interesting to compare timing waveforms for various PCB structures. This overview provides a good guess on the impact of serial termination, the use of via contacts, and the shape of trace structures connected to a pad driver.

We use 4 different structures, shown in Fig. 24:

(a) Point-to-Point,

(b) Bus,

(c) Star,

(d) Tree.

Each of the structures was drawn in 4 versions and simulated with Sigrity Speed2000™. The 4 versions are:

(1) no vias, no series termination,

(2) no vias, series termination at transmitter,

(3) vias, no series termination,

(4) vias, series termination.

In case of no vias, all traces are routed on the top PCB layer where transmitter and receivers are soldered. In case of vias, the red traces in Fig. 24 are routed on the bottom PCB layer. In case of series termination, a 51Ω resistor $R_t$ is connected directly at the transmitter output in the data line.

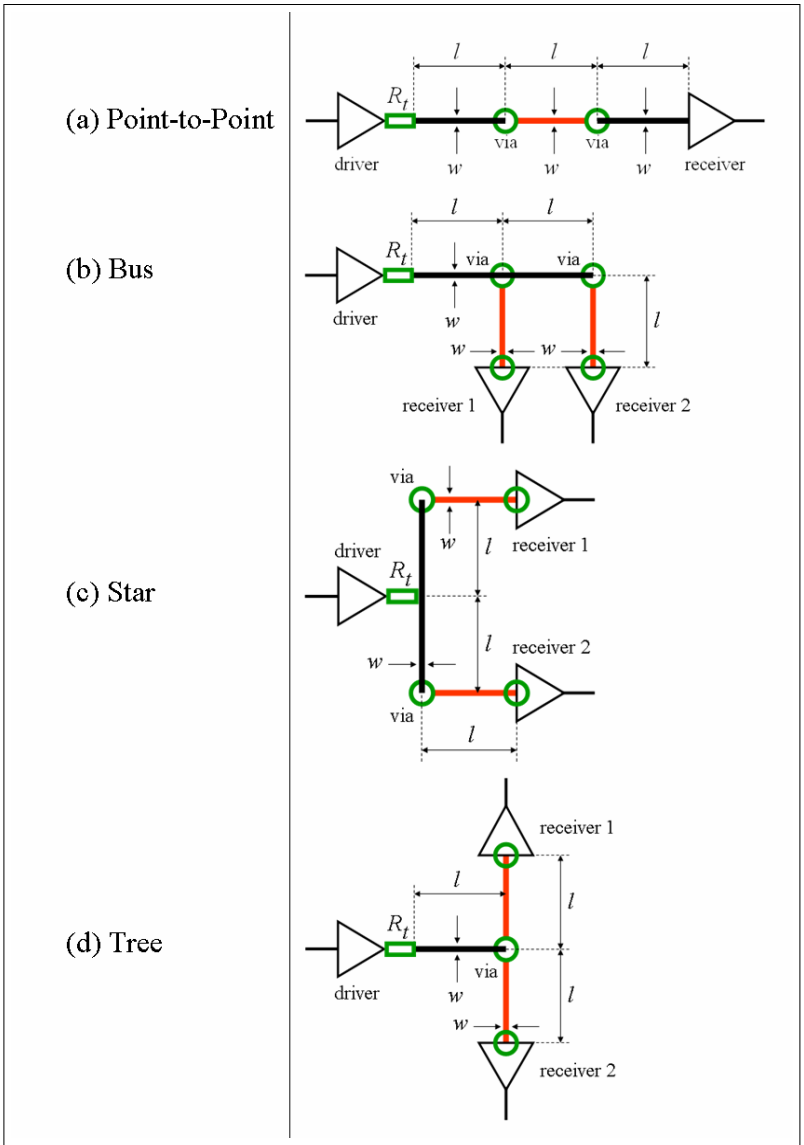


*Figure 24: Set of PCB trace structures*

The layer stack of the printed circuit board model is shown in Fig. 25. It consists of 4 layers in standard FR4 material in the order signal-GND-VCC-signal.

300µm trace width results in a 57Ω trace impedance.

The capacitance per unit length is 1pF/cm.

An input capacitance of 5pF per CMOS receiver input is assumed.

The driver is represented by the IBIS model listed in Appendix A. The driver strength can be selected to be “strong-sharp”, “strong-medium”, “strong-soft”, “medium” and “weak”.

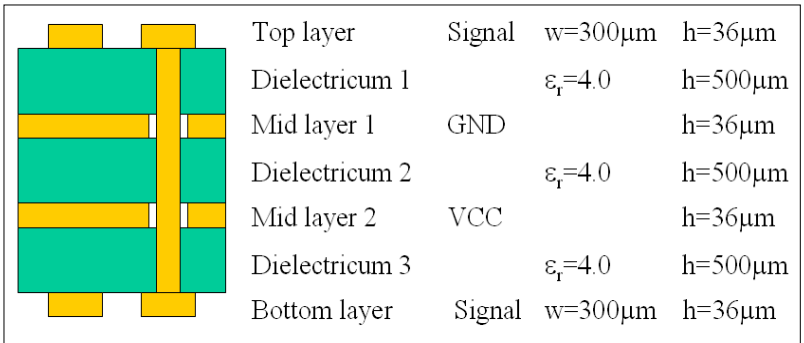


*Figure 25: PCB layer stack*

The length of each trace piece marked "*l*" in Fig. 24 has been dimensioned such that the resulting total trace capacitance plus the receiver gate capacitances are 20pF, 30pF, 40pF and 50pF. Table 3 lists the resulting trace lengths. The via contacts connect signals on the top layer with signals on the bottom layer.

Fig. 26-57 show the simulated rise and fall times as a function of PCB structures with different capacitive loads. In each diagram, the measured timings and the simulated timings with ideal capacitive load are given for reference.

To keep a better overview, one diagram contains only the curves for one structure operating at one temperature. The parameters varied in one diagram are the load capacitance and the driver settings. The abbreviations are as defined in Table 2.

| Structure | Load | Length "*l*" | Width "*w*" |
|---|---|---|---|
| Point-to-Point | 20 pF | 5.1 cm | 300 µm |
| | 30 pF | 8.5 cm | 300 µm |
| | 40pF | 11.9 cm | 300 µm |
| | 50 pF | 15.3 cm | 300 µm |
| Bus | 20 pF | 4.4 cm | 300 µm |
| | 30 pF | 7.9 cm | 300 µm |
| | 40 pF | 12.5 cm | 300 µm |
| | 50 pF | 16.8 cm | 300 µm |
| Star | 20 pF | 4.2 cm | 300 µm |
| | 30 pF | 8.1 cm | 300 µm |
| | 40 pF | 12.2 cm | 300 µm |
| | 50 pF | 16.9 cm | 300 µm |
| Tree | 20 pF | 5.9 cm | 300 µm |
| | 30 pF | 11.4 cm | 300 µm |
| | 40 pF | 17.2 cm | 300 µm |
| | 50 pF | 21.3 cm | 300 µm |

Table 3: Dimensions of PCB structures

### 4.1.2 Rise/fall time diagrams

All rise/fall times refer to the 10-90% rising edge and to the 90-10% falling edge of the transmitter output voltage. Details are identical to the measured timings and levels described in chapter 3.1.1.

Weak driver strength has not been simulated because of the very low rise and fall times. Main purpose is to show the influence of via contacts which are placed on the traces, and series termination resistors placed at the driver outputs.

The 4 via/termination combinations are marked in the diagrams as follows:

"Vias No Term No" = no via contacts, no termination resistor

"Vias Yes Term No" = via contacts, but no termination resistor

"Vias No Term Yes" = no via contacts, but termination resistor

"Vias Yes Term Yes" = via contacts and termination resistor

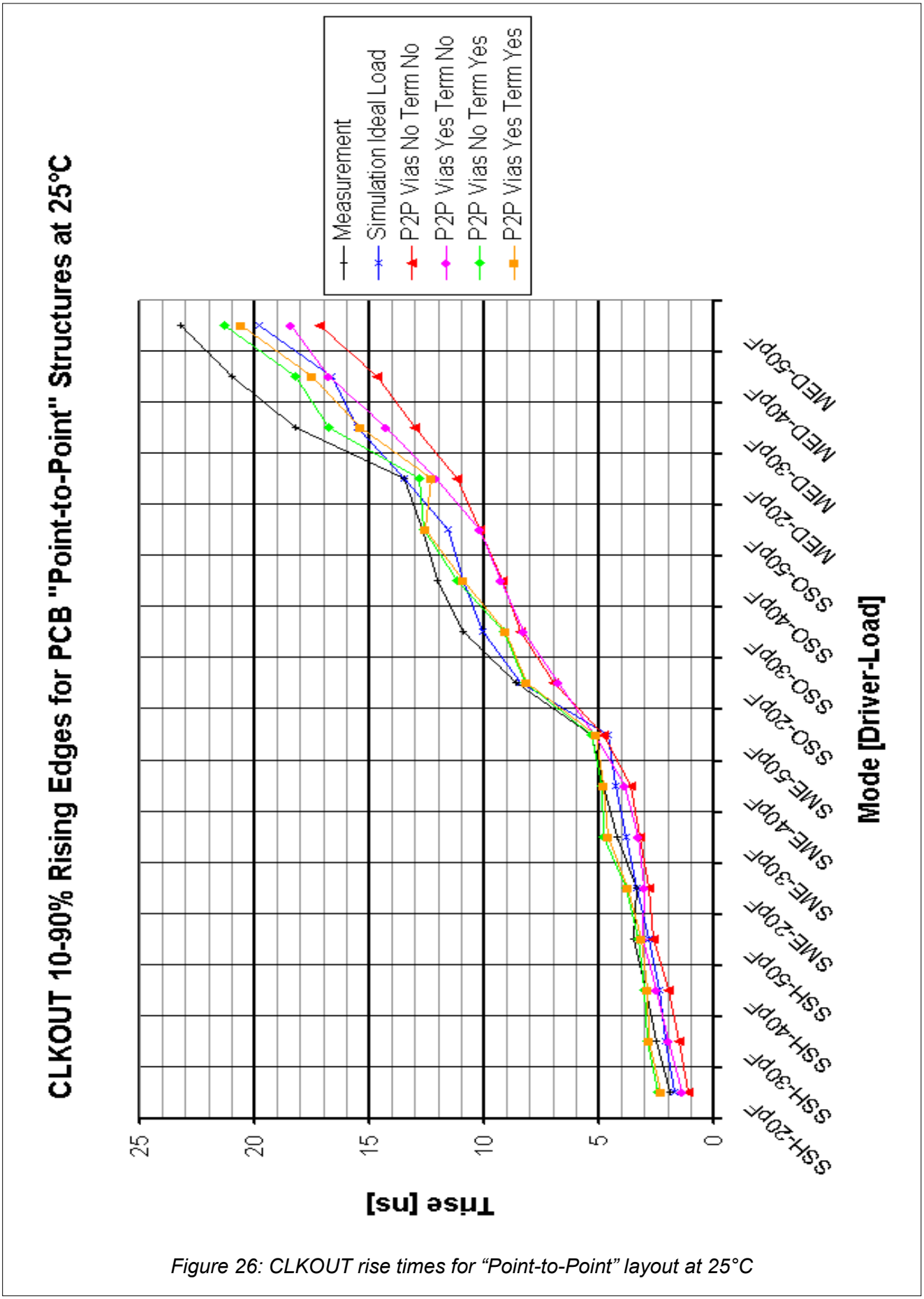


*Figure 26: CLKOUT rise times for “Point-to-Point” layout at 25°C*

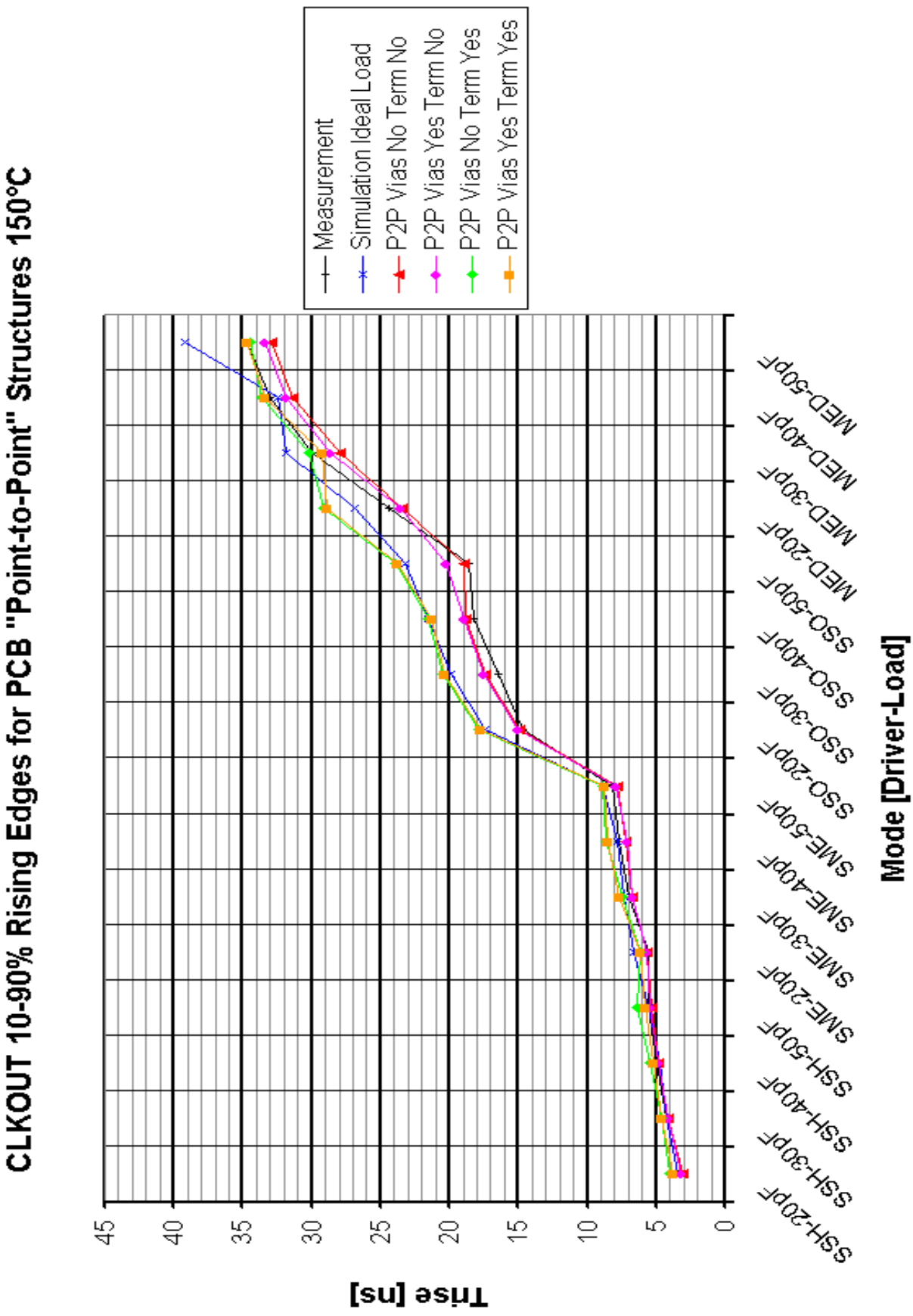


*Figure 27: CLKOUT rise times for “Point-to-Point” layout at 150°C*

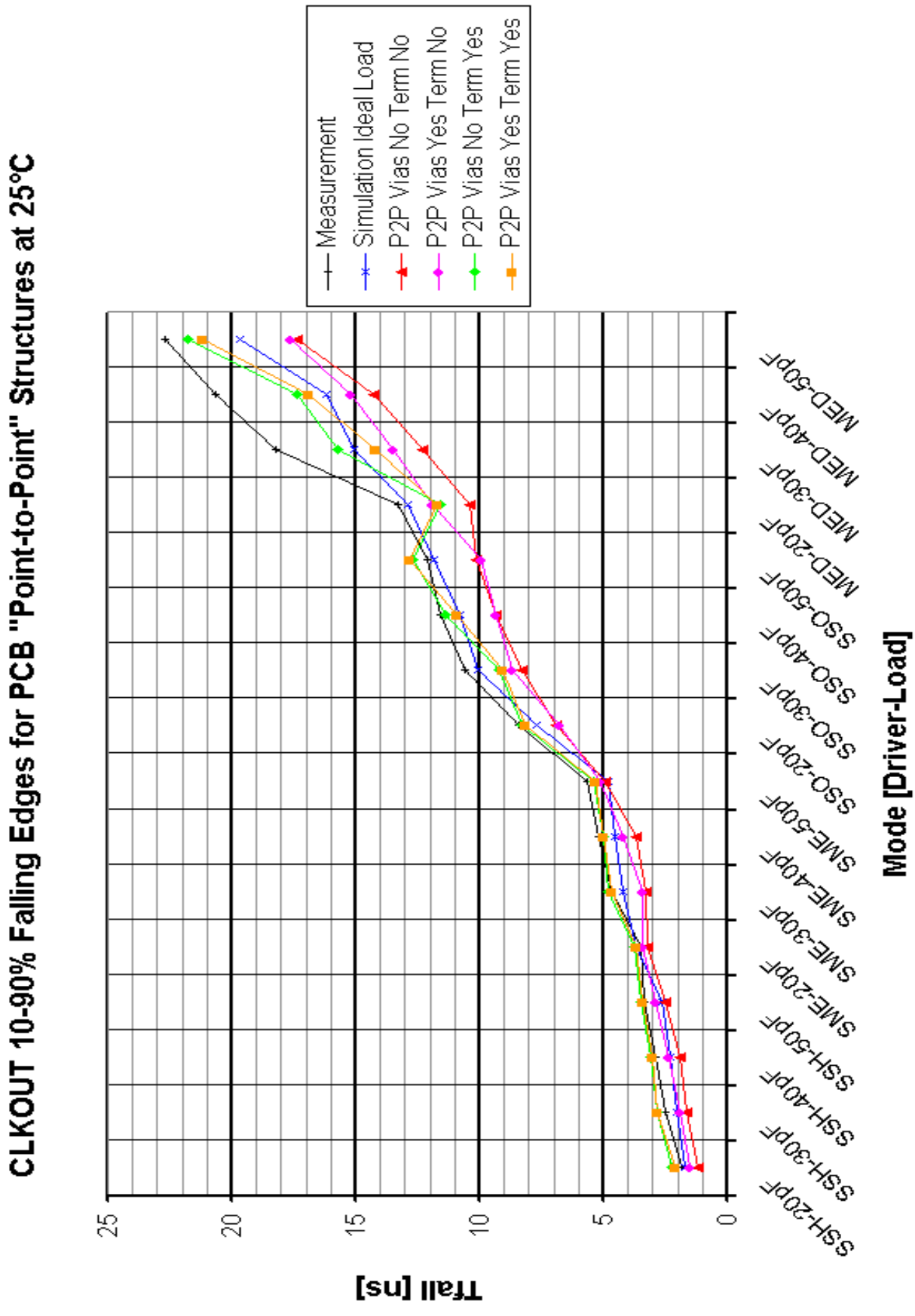


*Figure 28: CLKOUT fall times for “Point-to-Point” layout at 25°C*

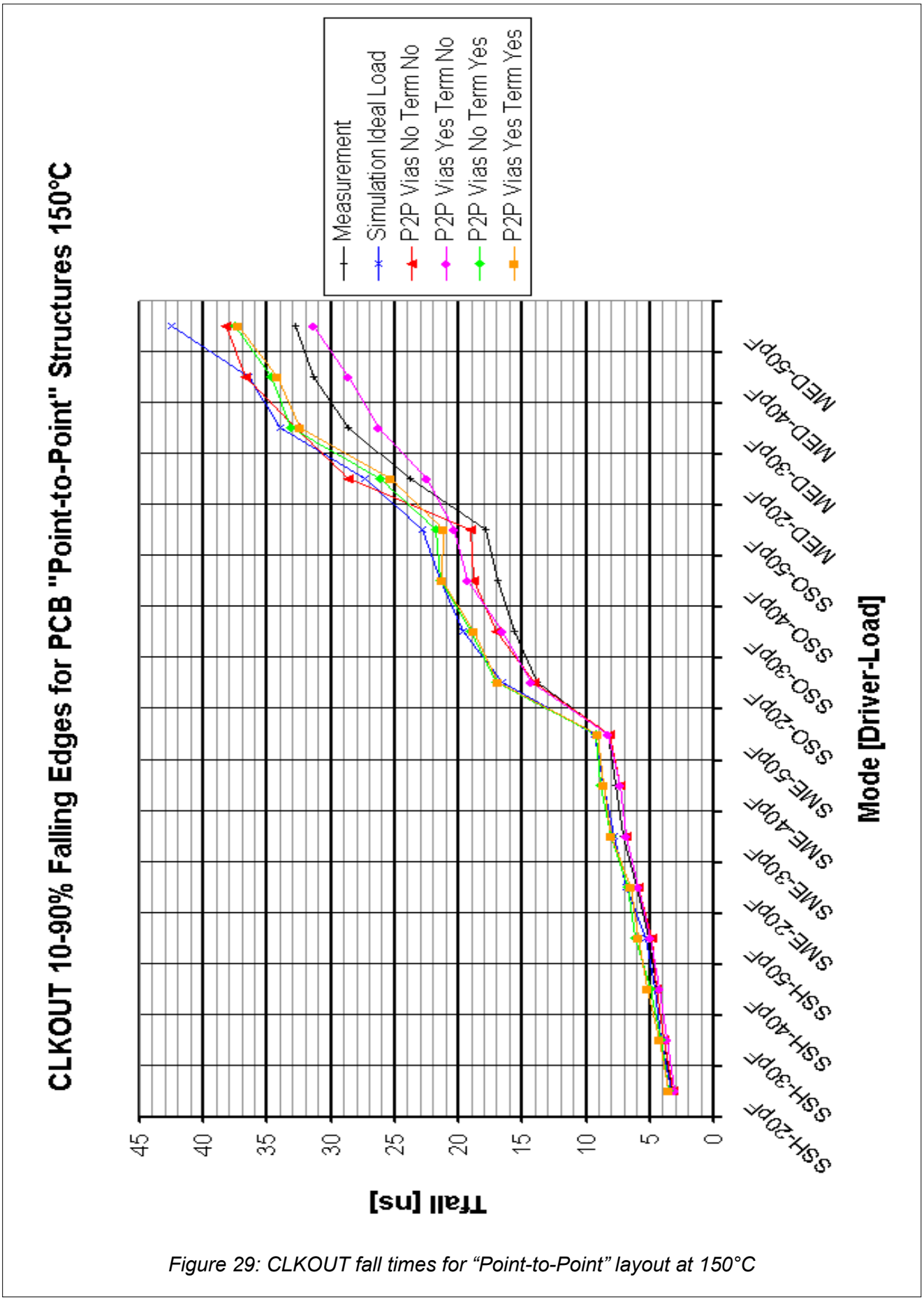


*Figure 29: CLKOUT fall times for “Point-to-Point” layout at 150°C*

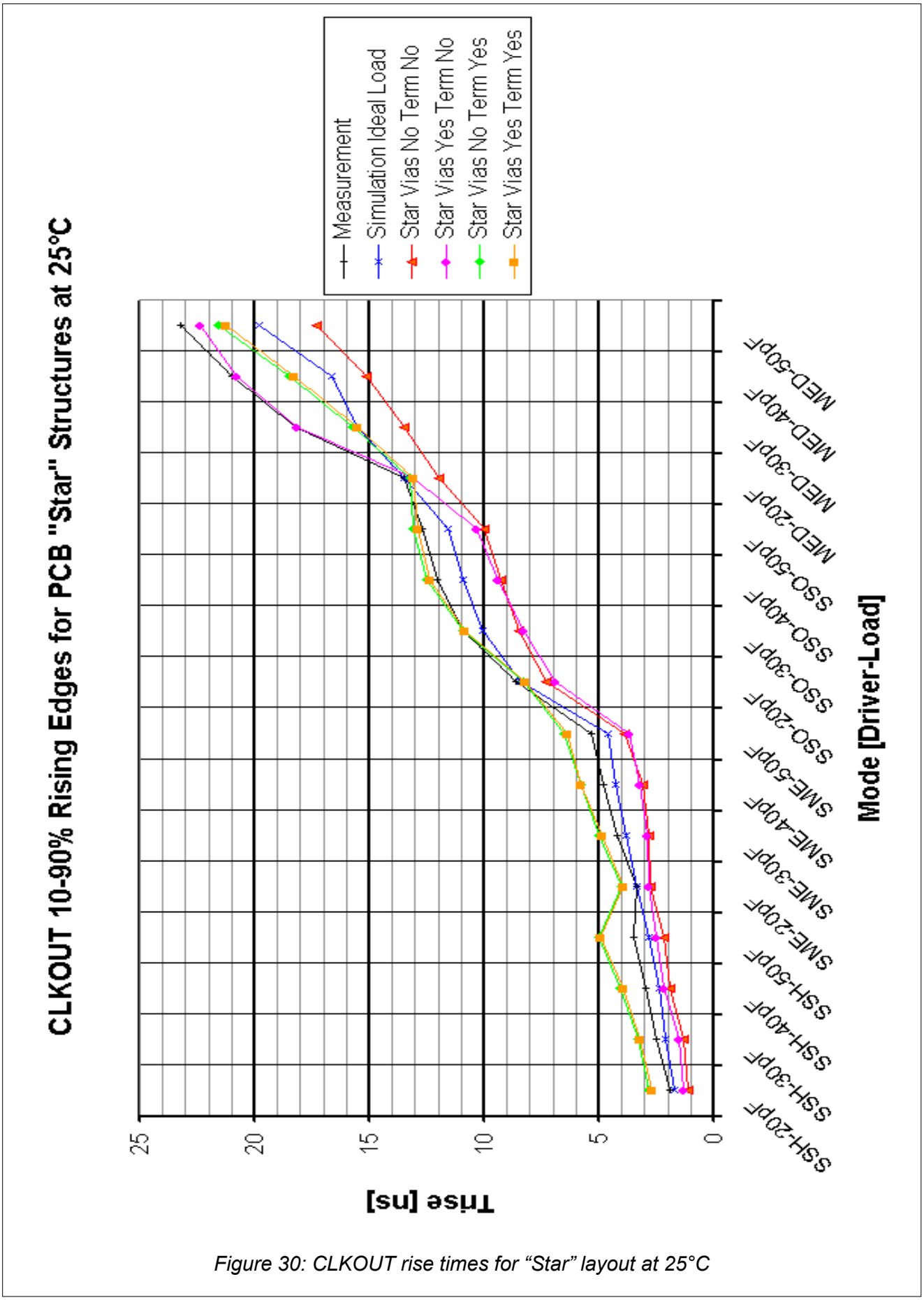


*Figure 30: CLKOUT rise times for “Star” layout at 25°C*

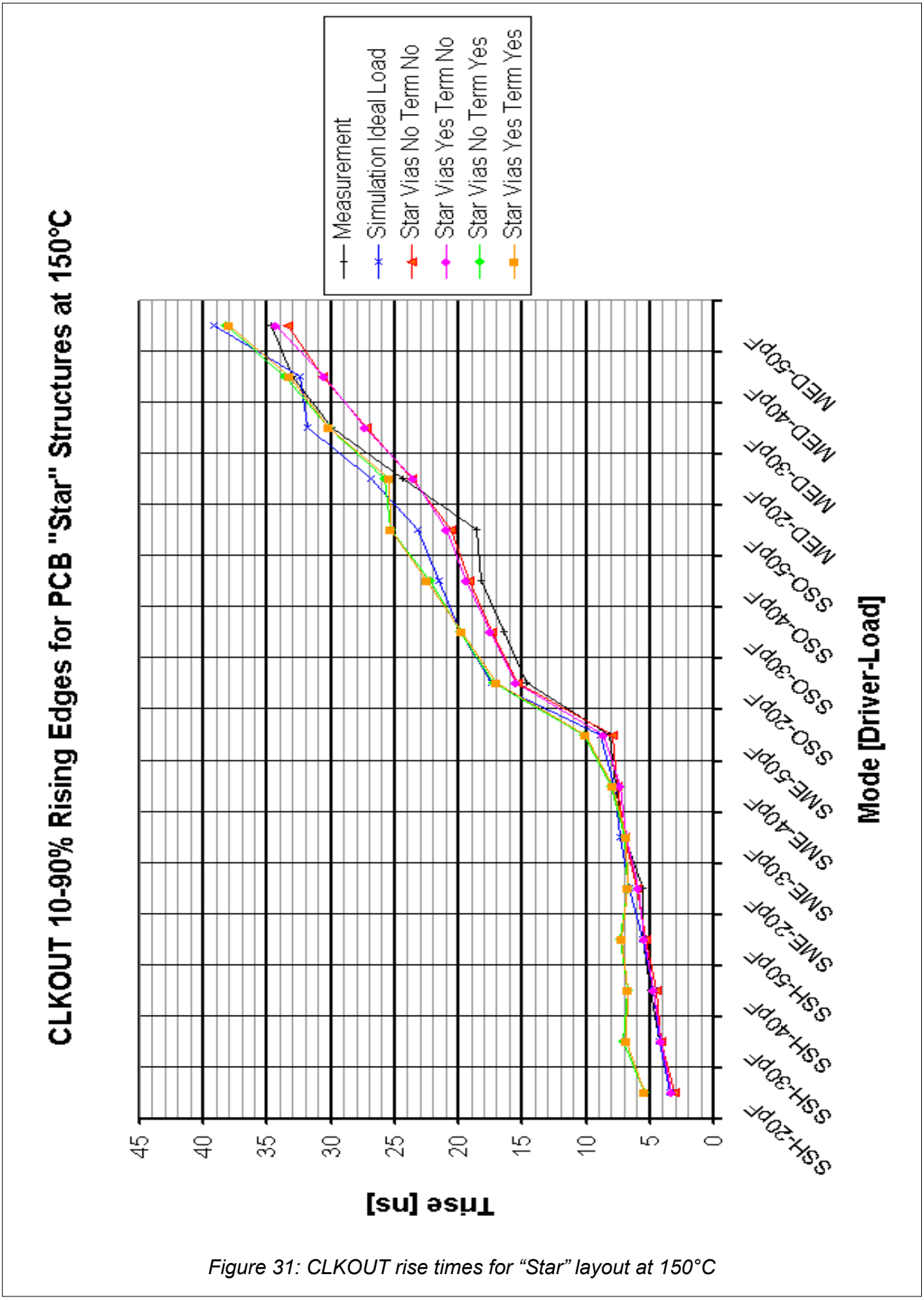


*Figure 31: CLKOUT rise times for “Star” layout at 150°C*

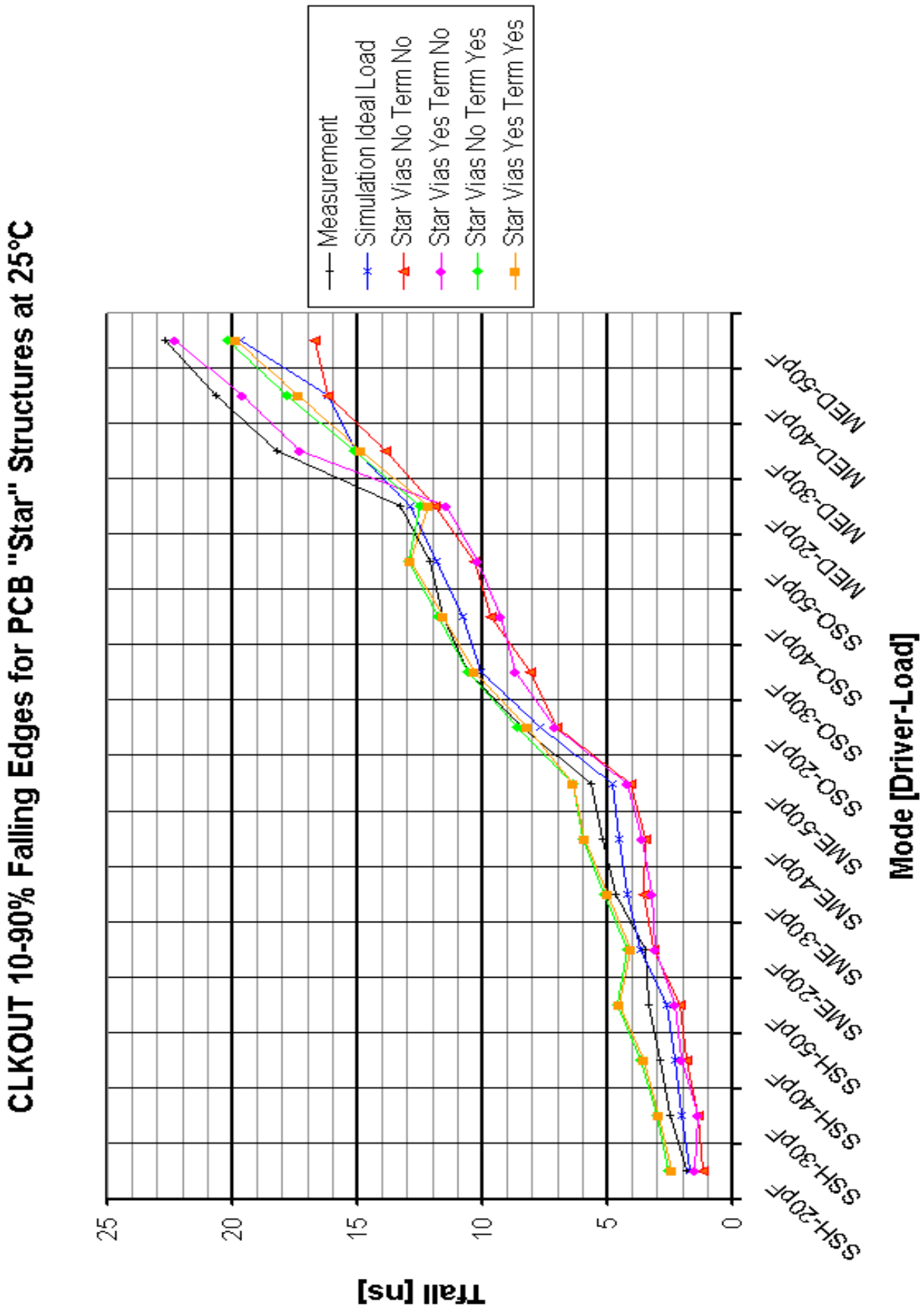


*Figure 32: CLKOUT fall times for “Star” layout at 25°C*

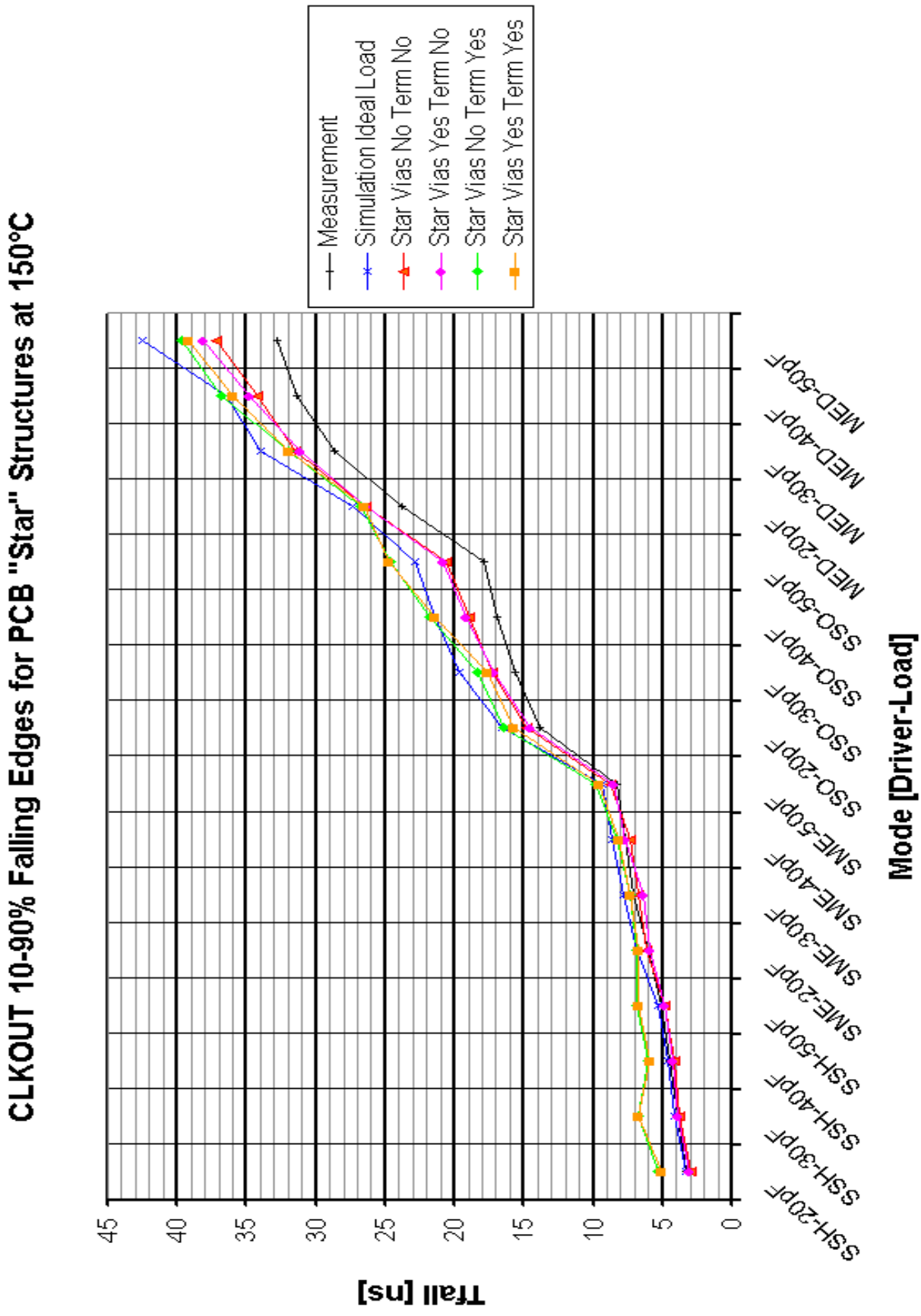


*Figure 33: CLKOUT fall times for “Star” layout at 150°C*

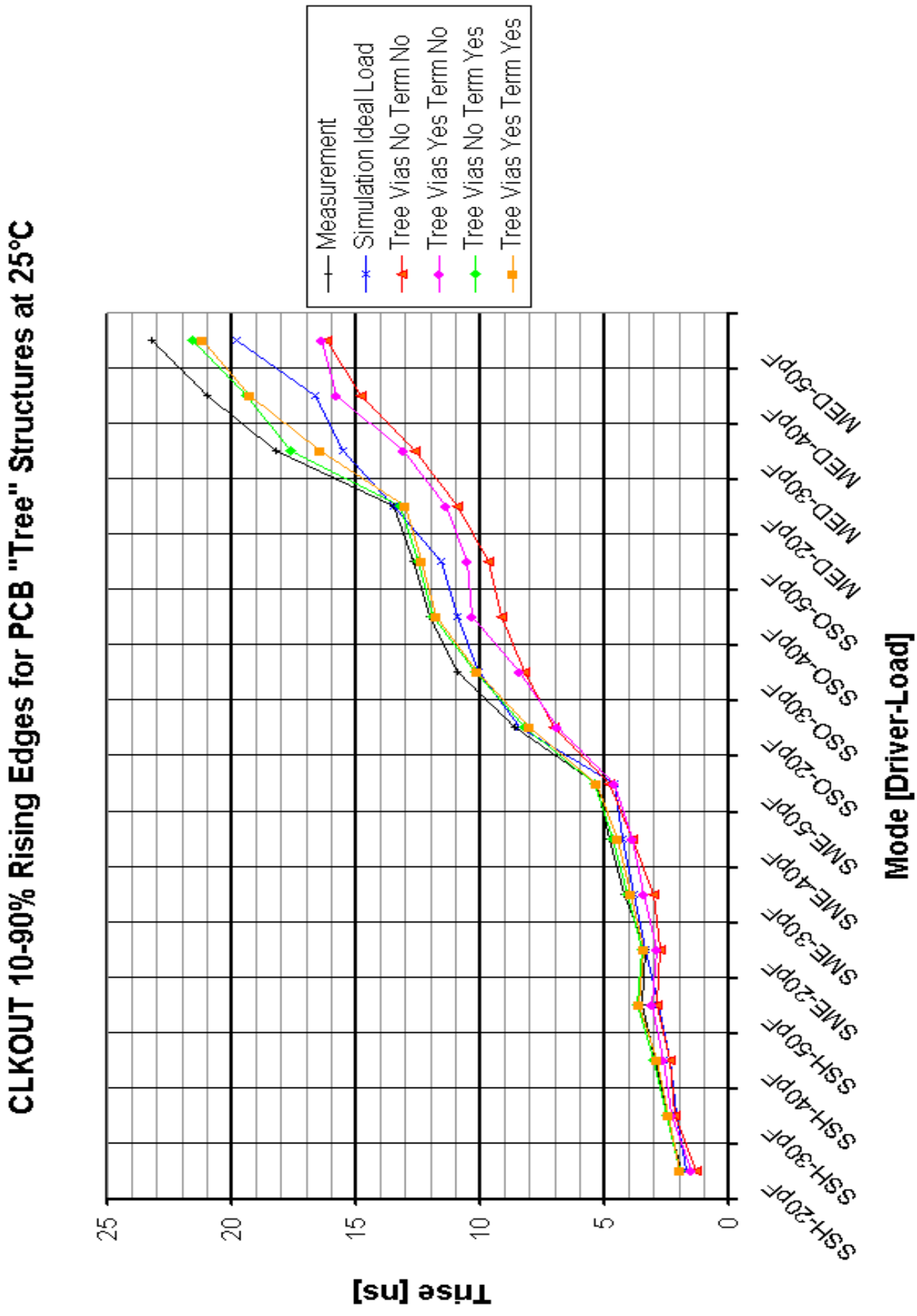


*Figure 34: CLKOUT rise times for “Tree” layout at 25°C*

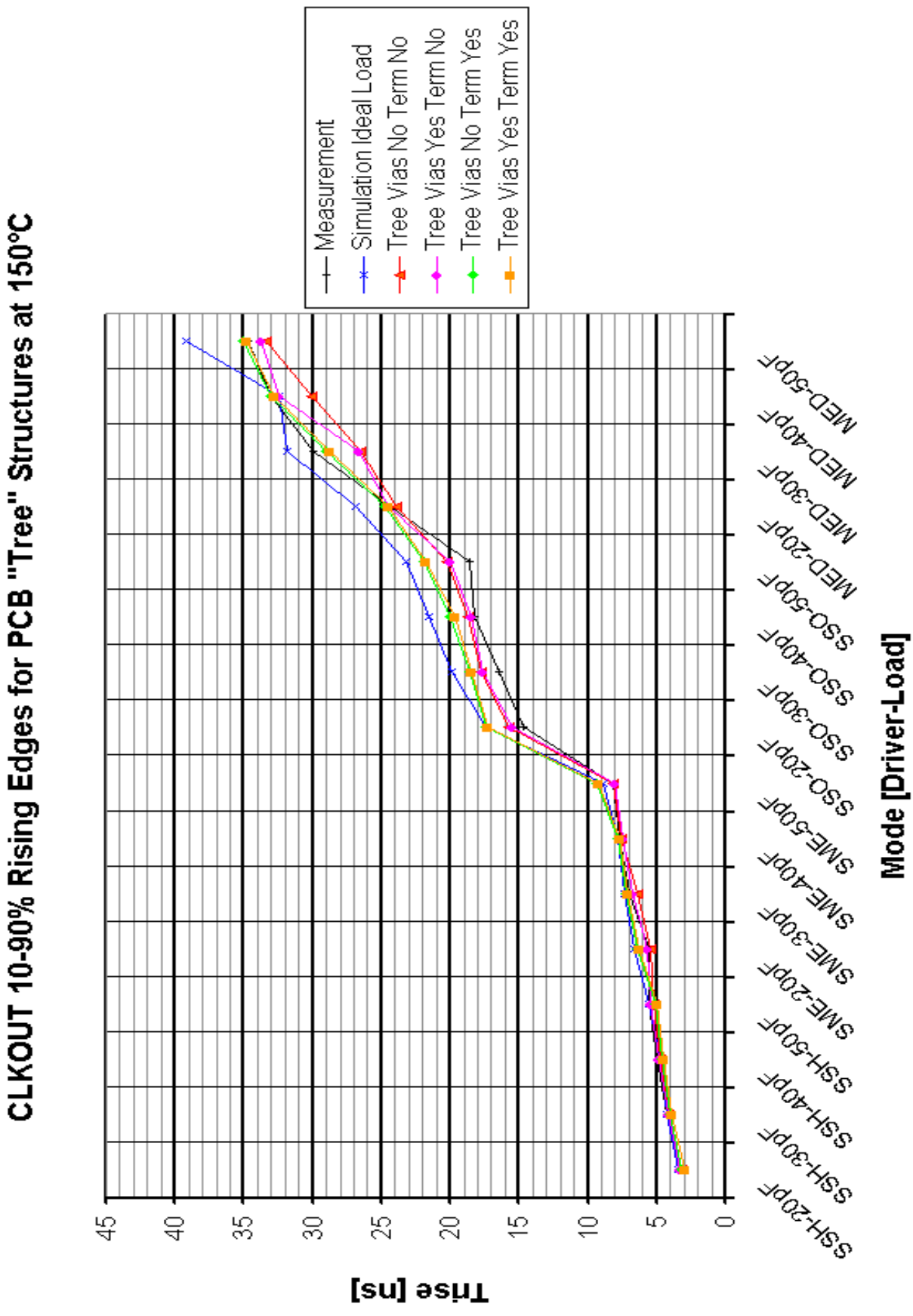


*Figure 35: CLKOUT rise times for “Tree” layout at 150°C*

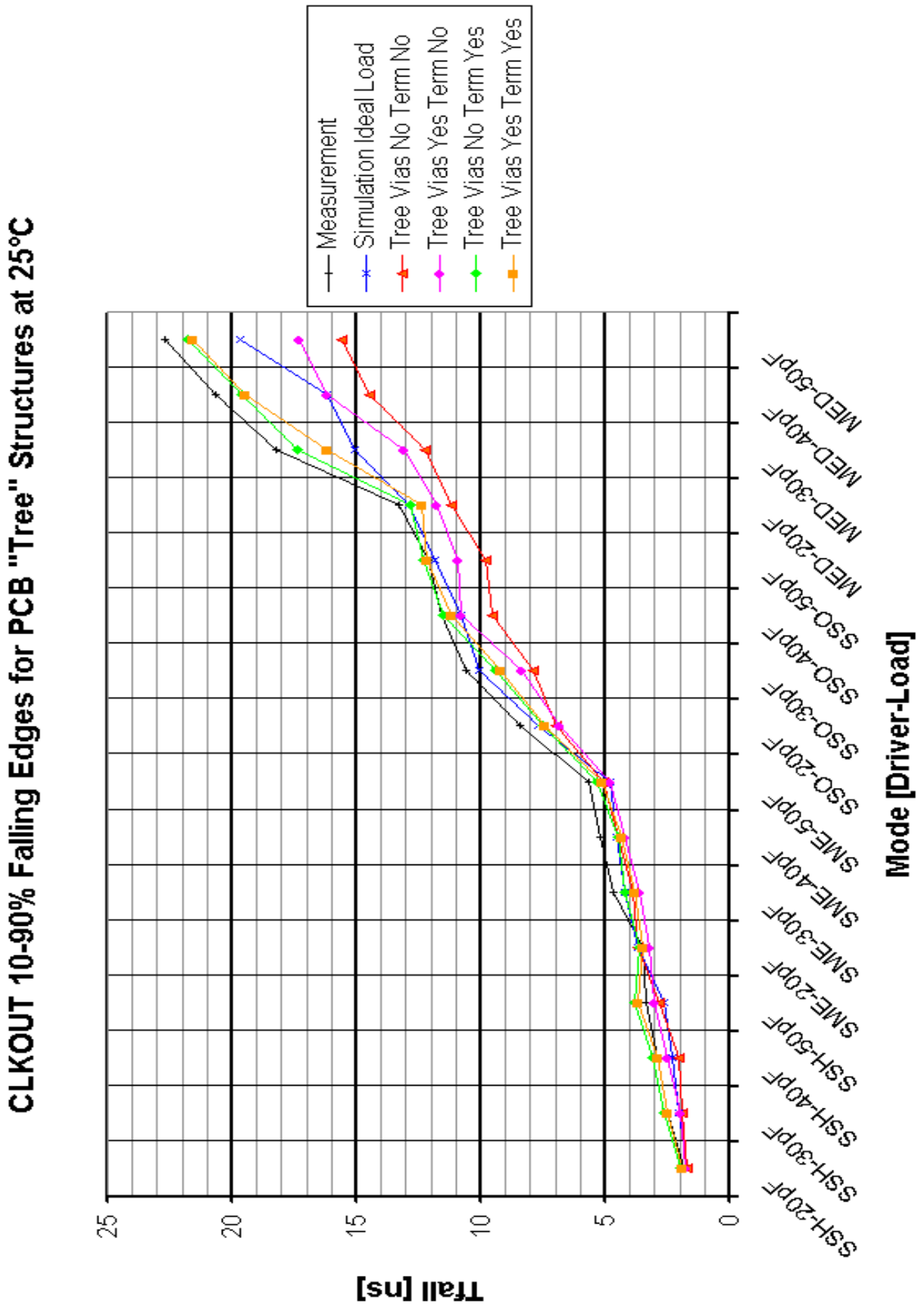


*Figure 36: CLKOUT fall times for “Tree” layout at 25°C*

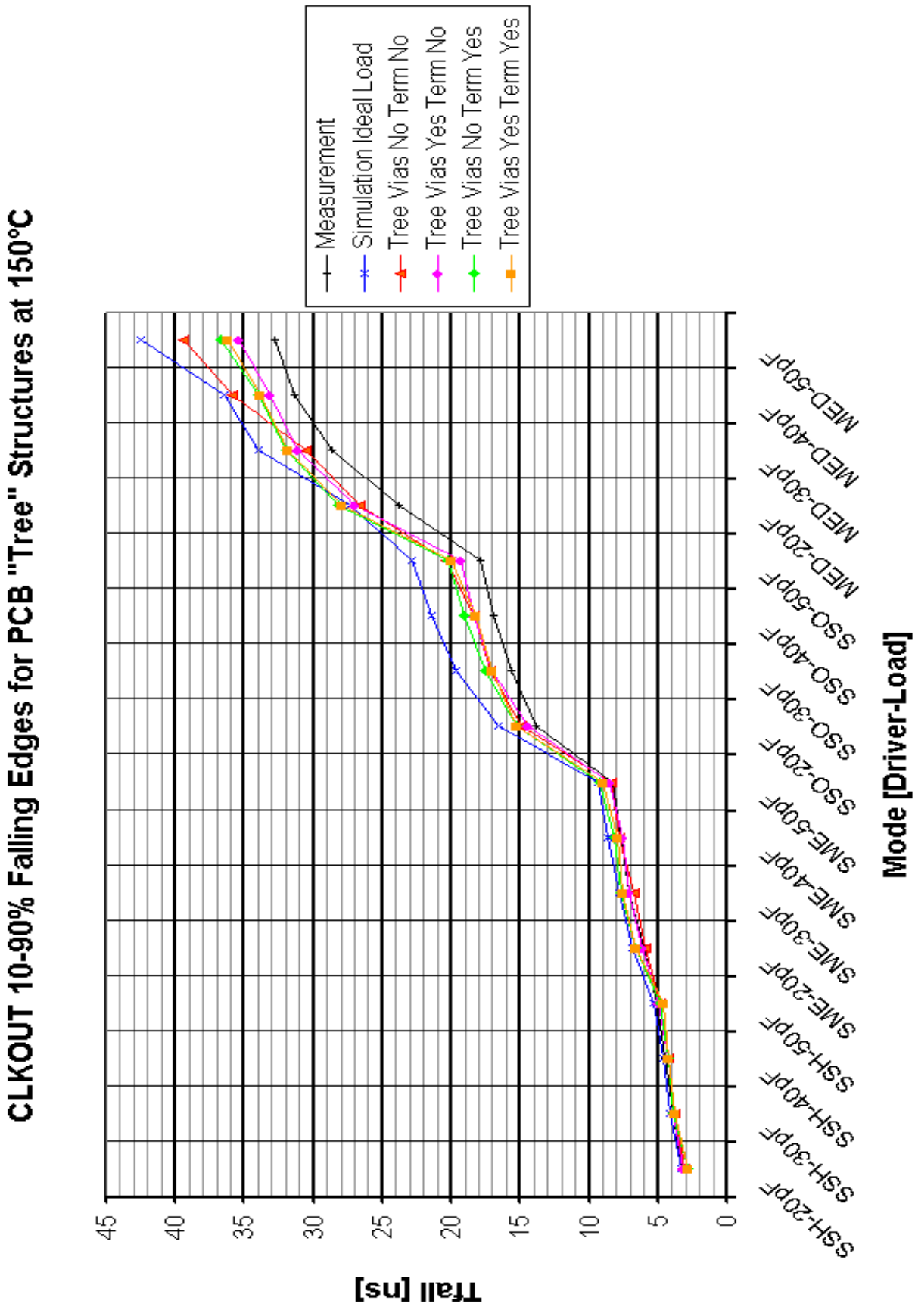


*Figure 37: CLKOUT fall times for “Tree” layout at 150°C*

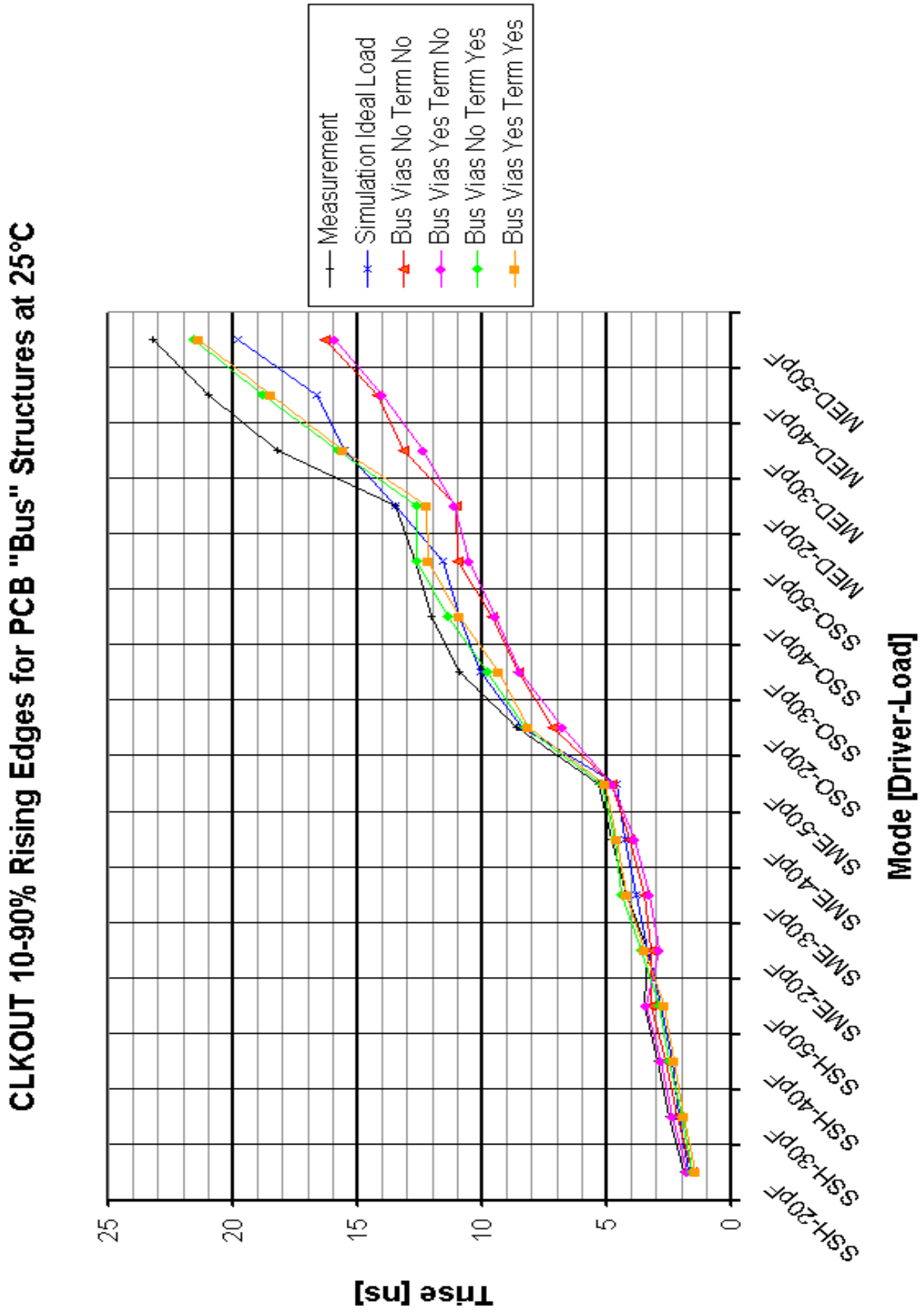


*Figure 38: CLKOUT rise times for “Bus” layout at 25°C*

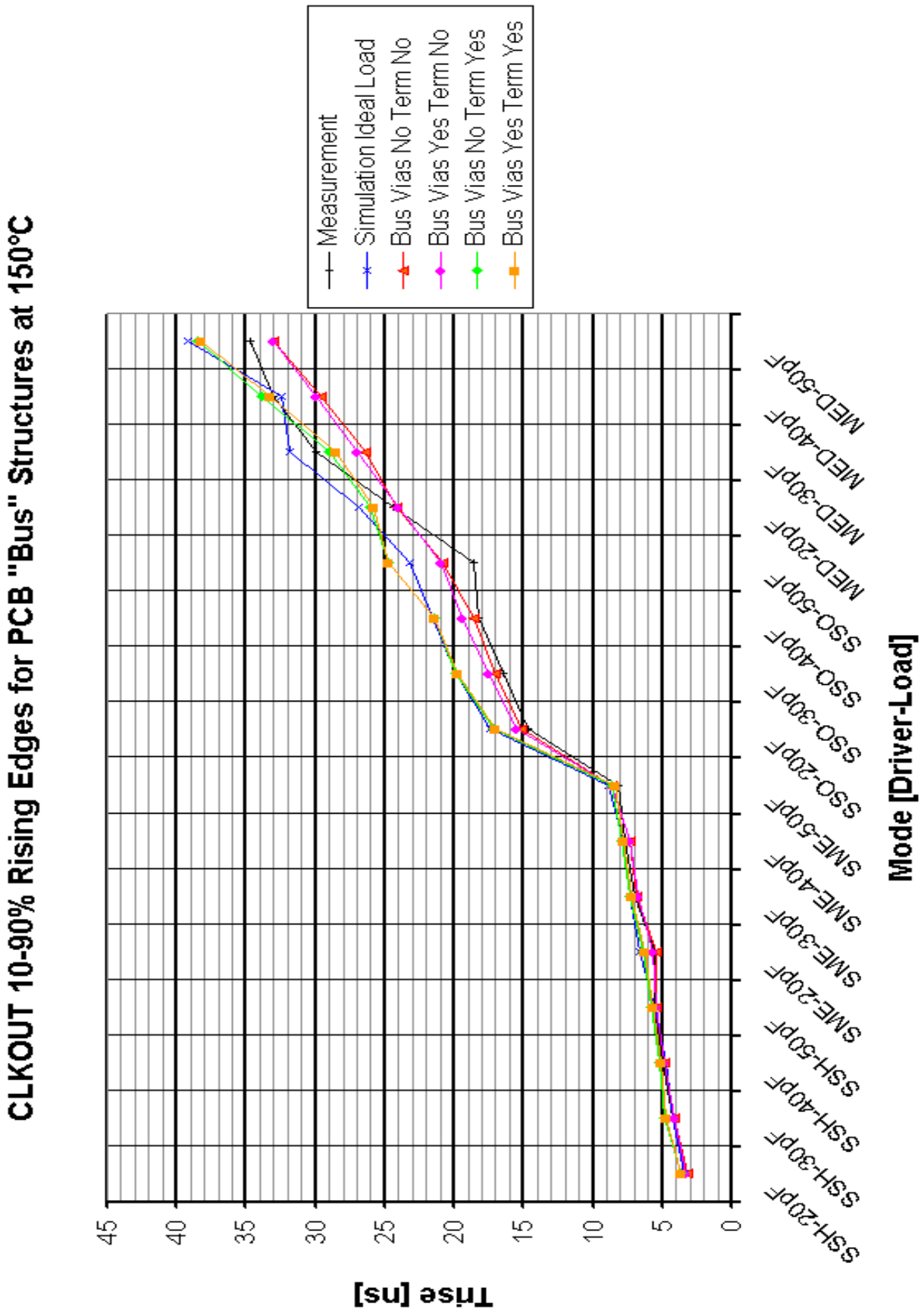


*Figure 39: CLKOUT rise times for “Bus” layout at 150°C*

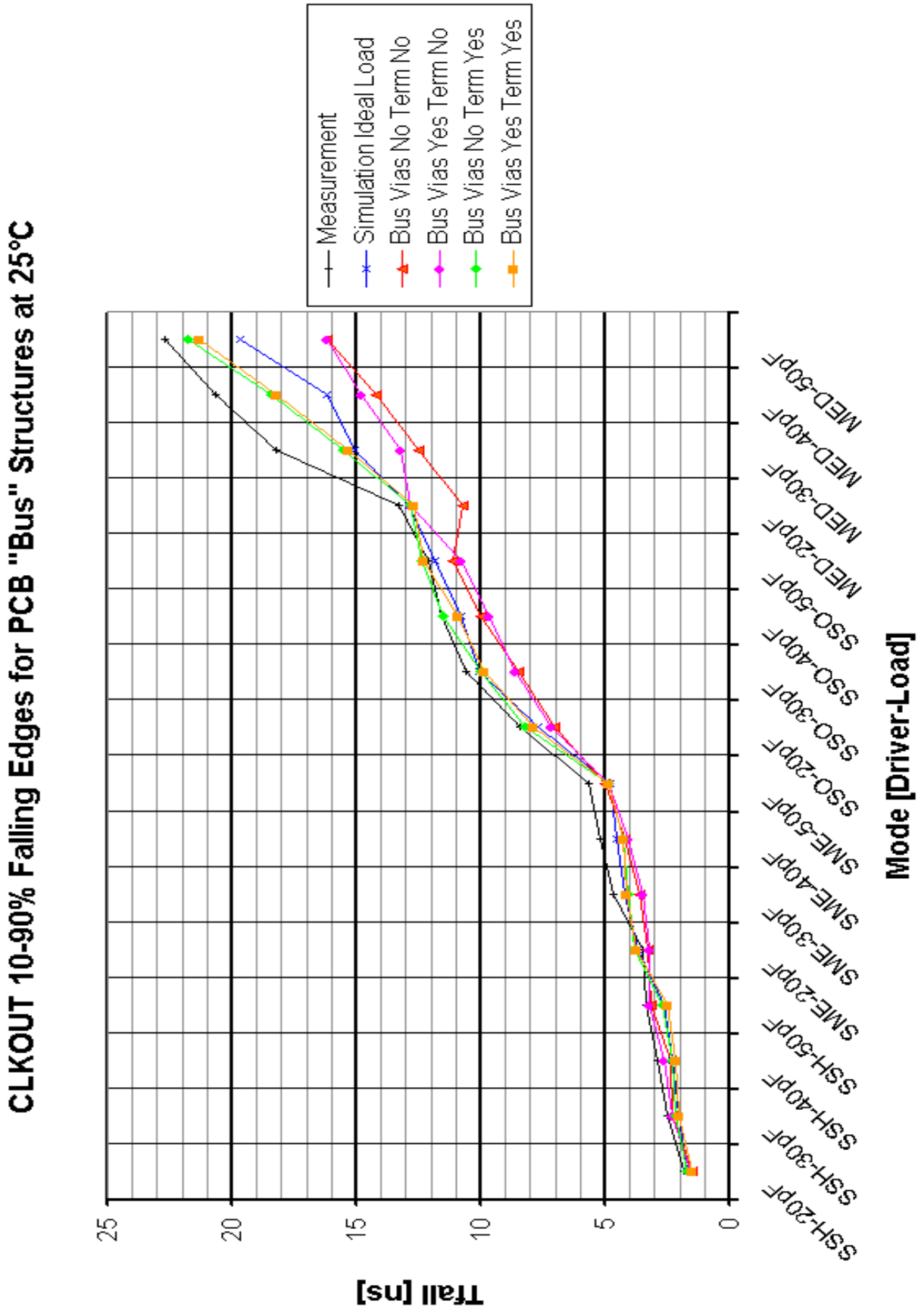


*Figure 40: CLKOUT fall times for “Bus” layout at 25°C*

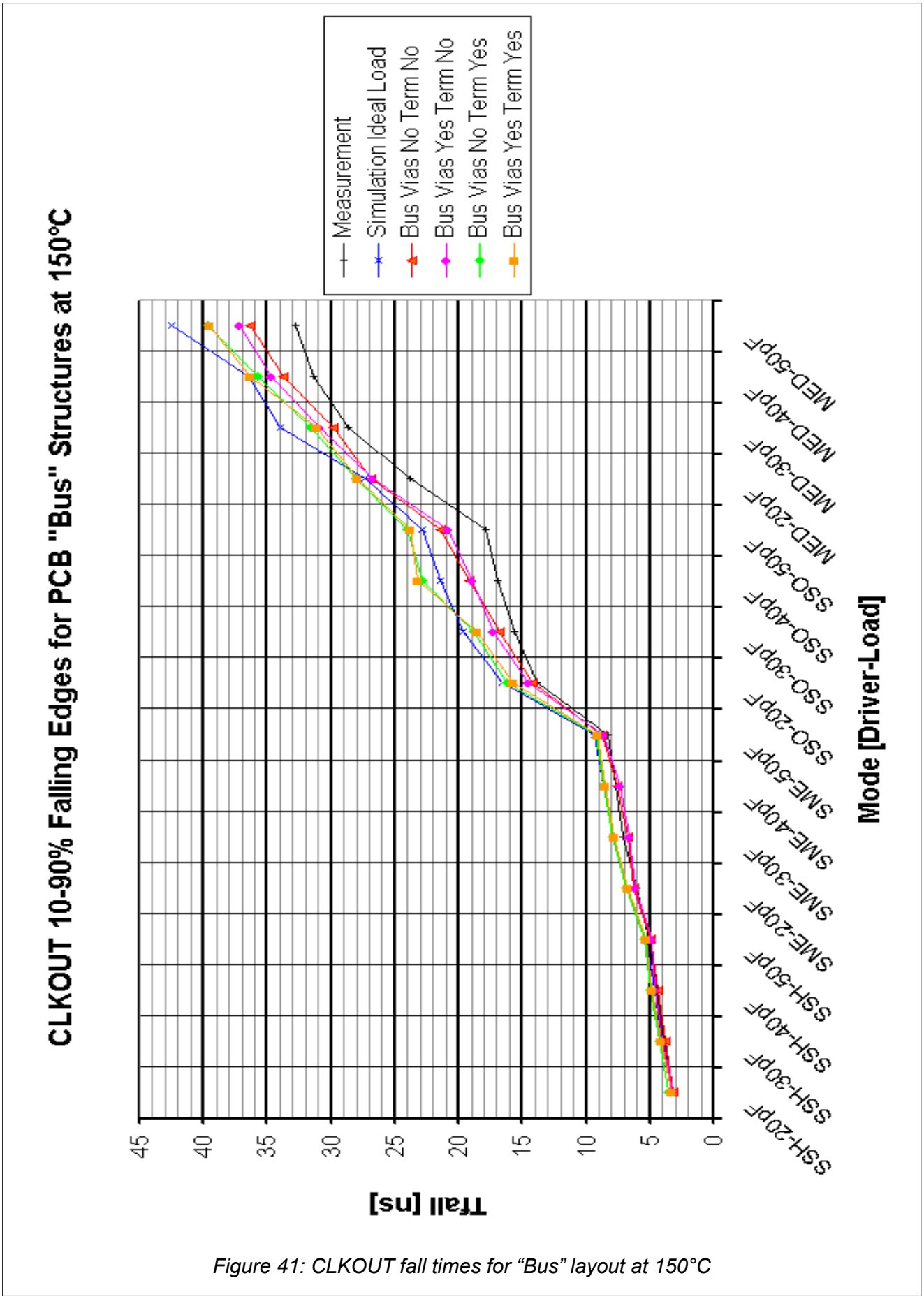


*Figure 41: CLKOUT fall times for “Bus” layout at 150°C*

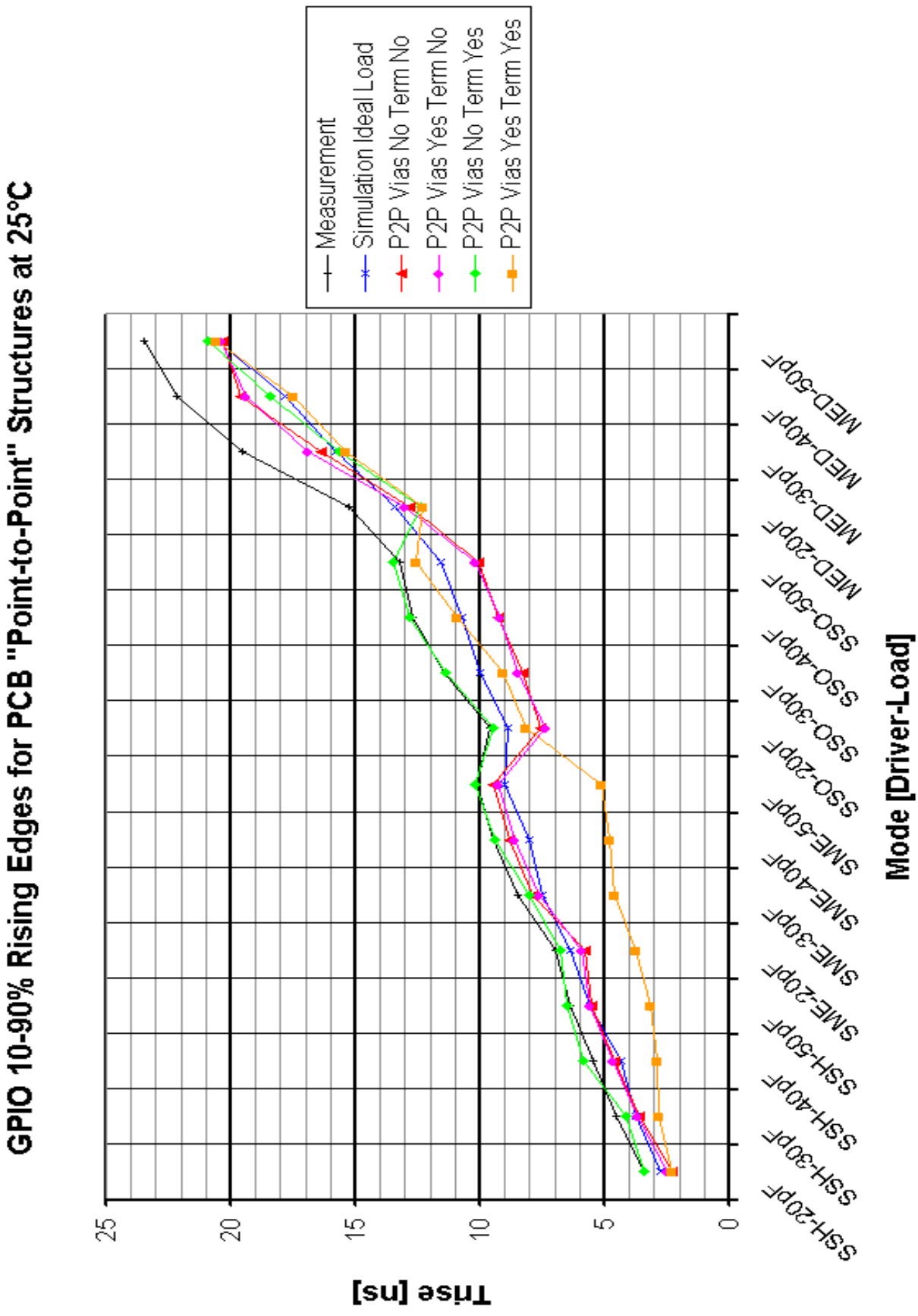


*Figure 42: GPIO rise times for “Point-to-Point” layout at 25°C*

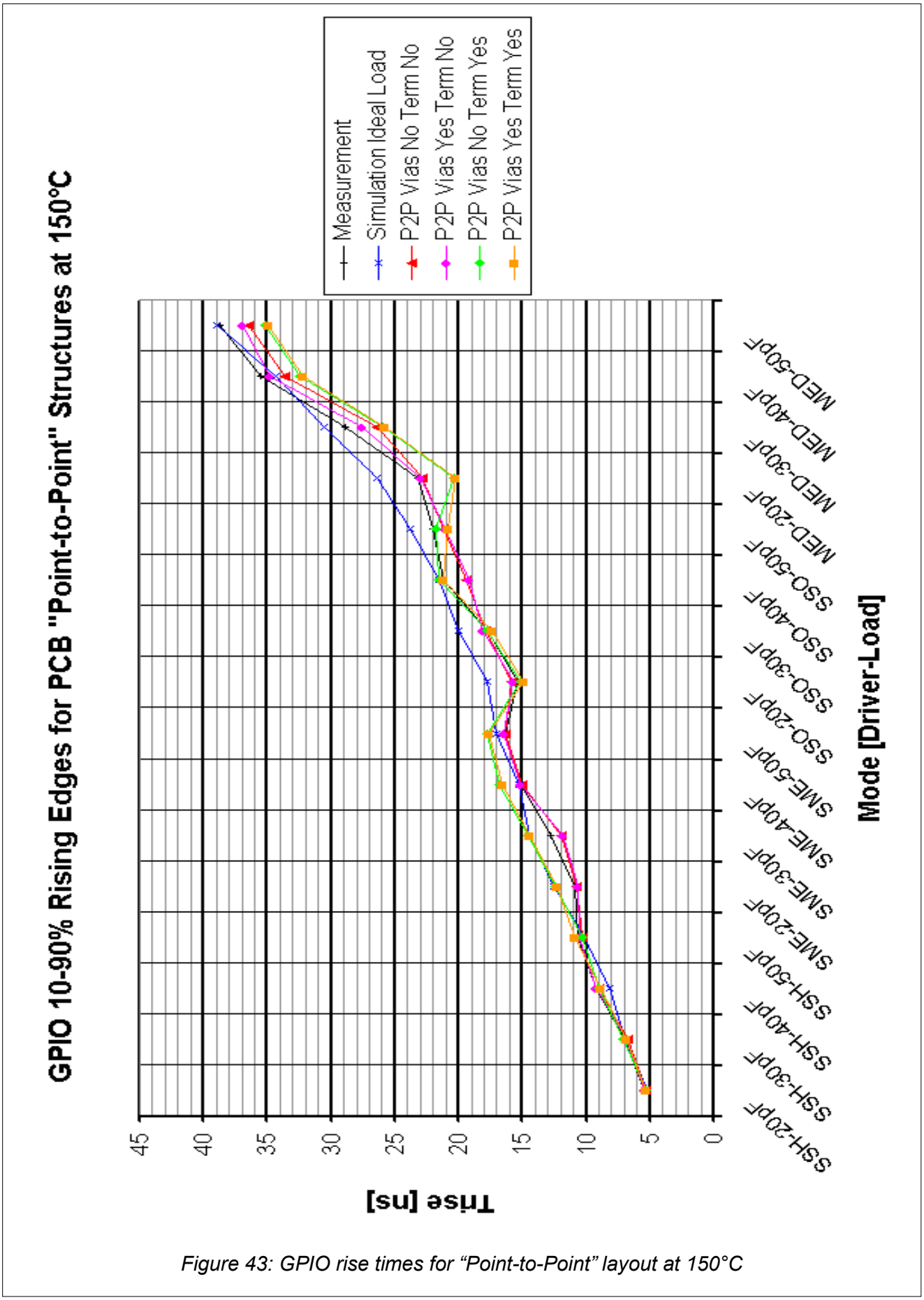


*Figure 43: GPIO rise times for “Point-to-Point” layout at 150°C*

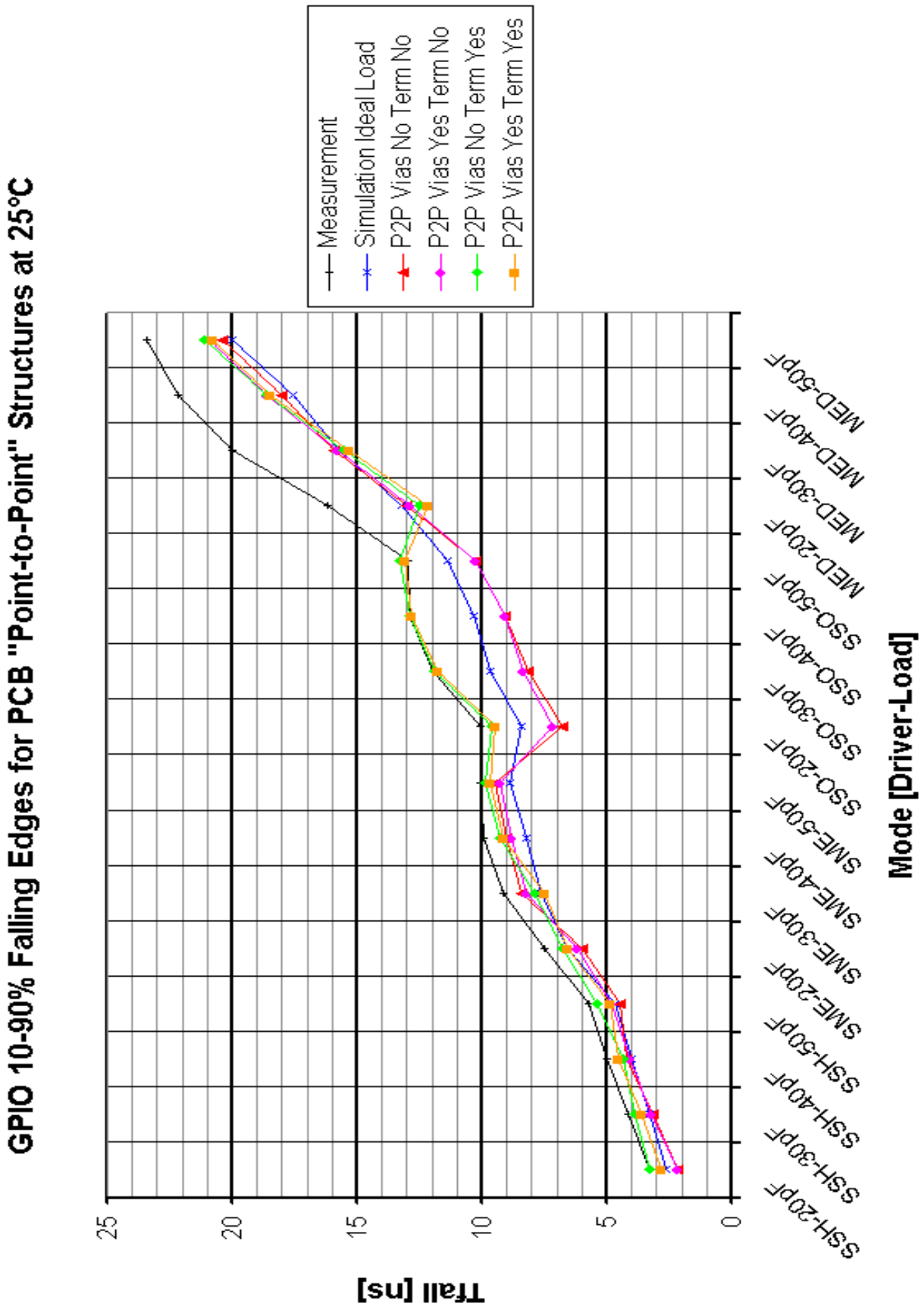


*Figure 44: GPIO fall times for “Point-to-Point” layout at 25°C*

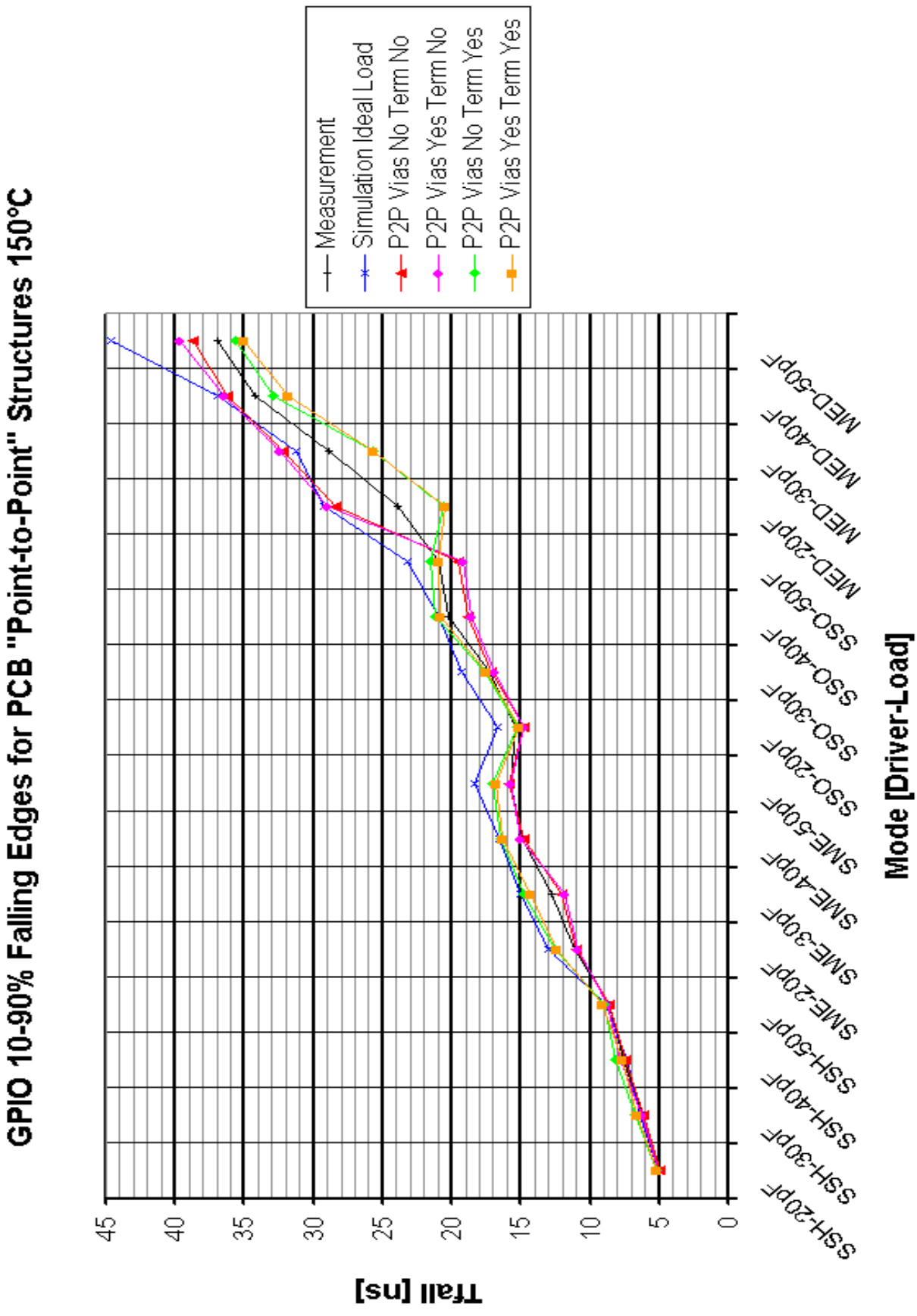


*Figure 45: GPIO fall times for “Point-to-Point” layout at 150°C*

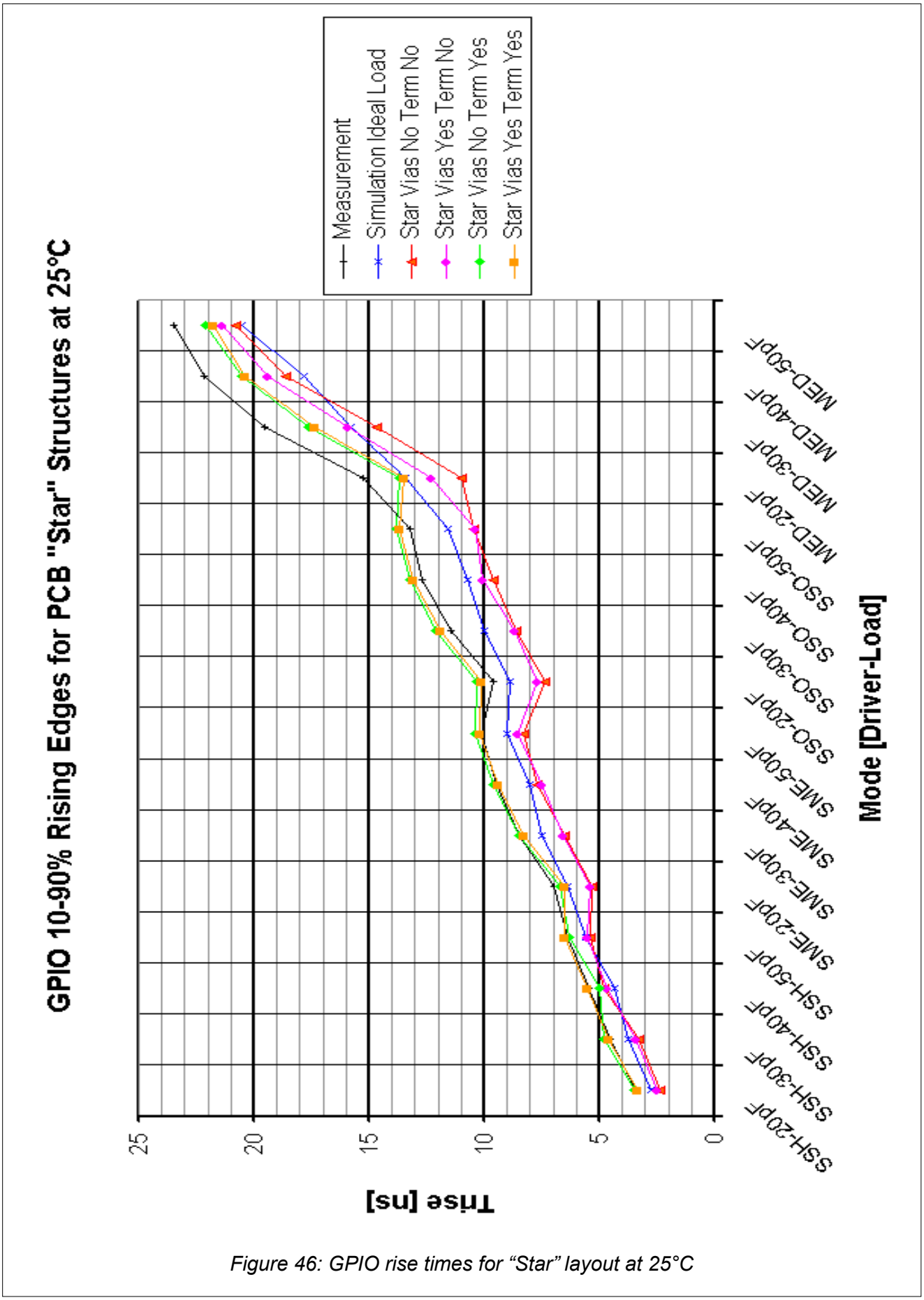


*Figure 46: GPIO rise times for "Star" layout at 25°C*

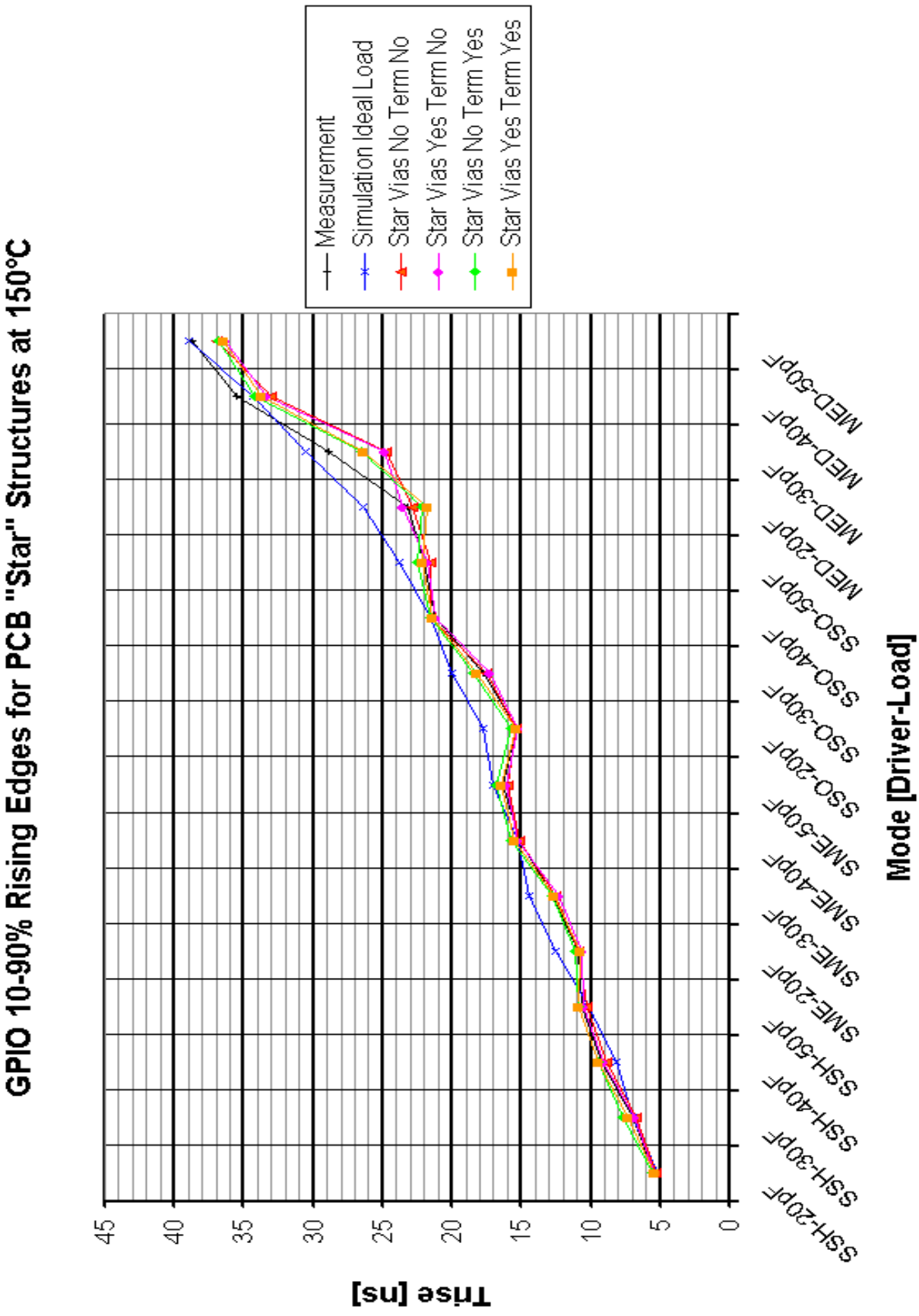


*Figure 47: GPIO rise times for “Star” layout at 150°C*

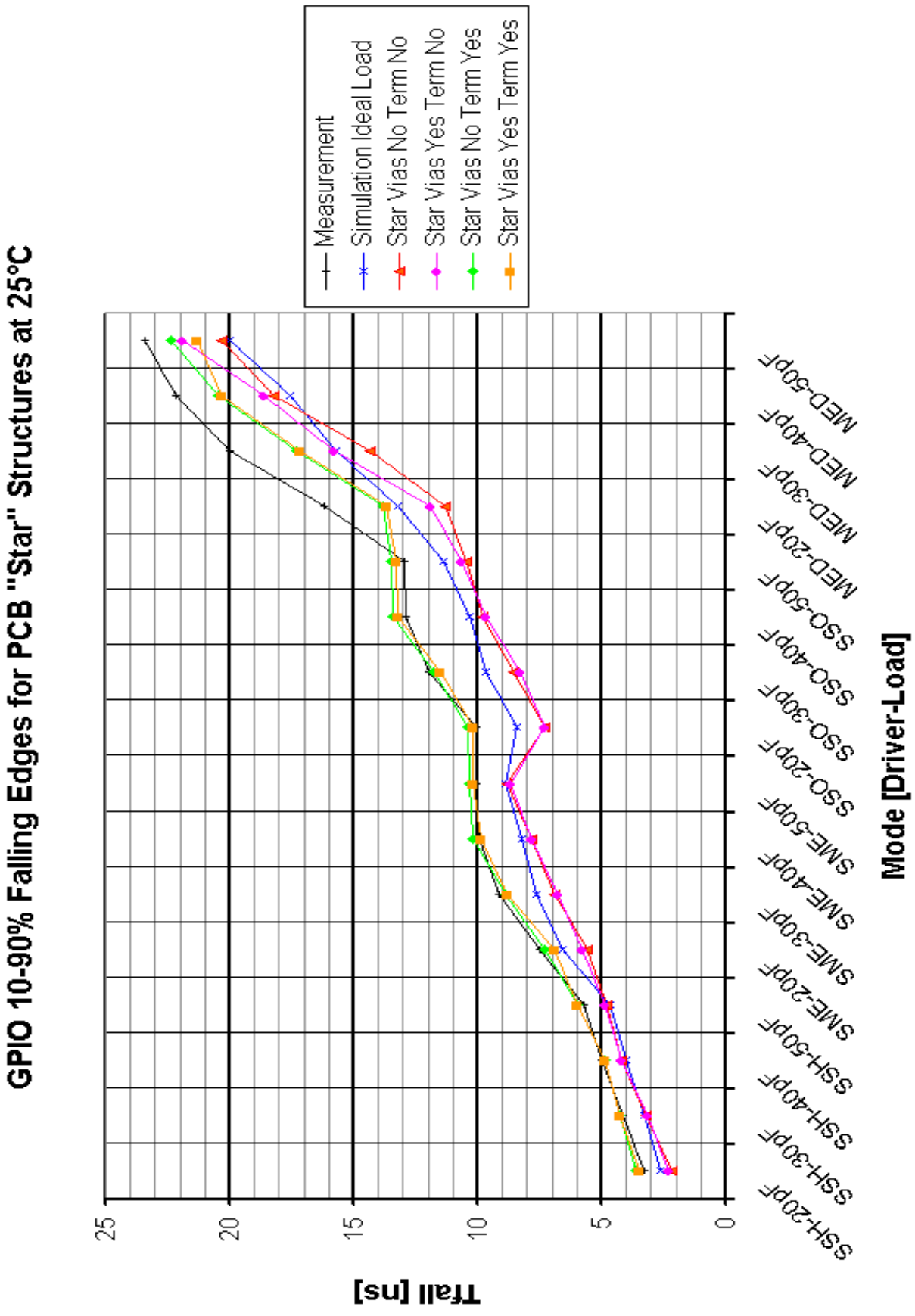


*Figure 48: GPIO fall times for “Star” layout at 25°C*

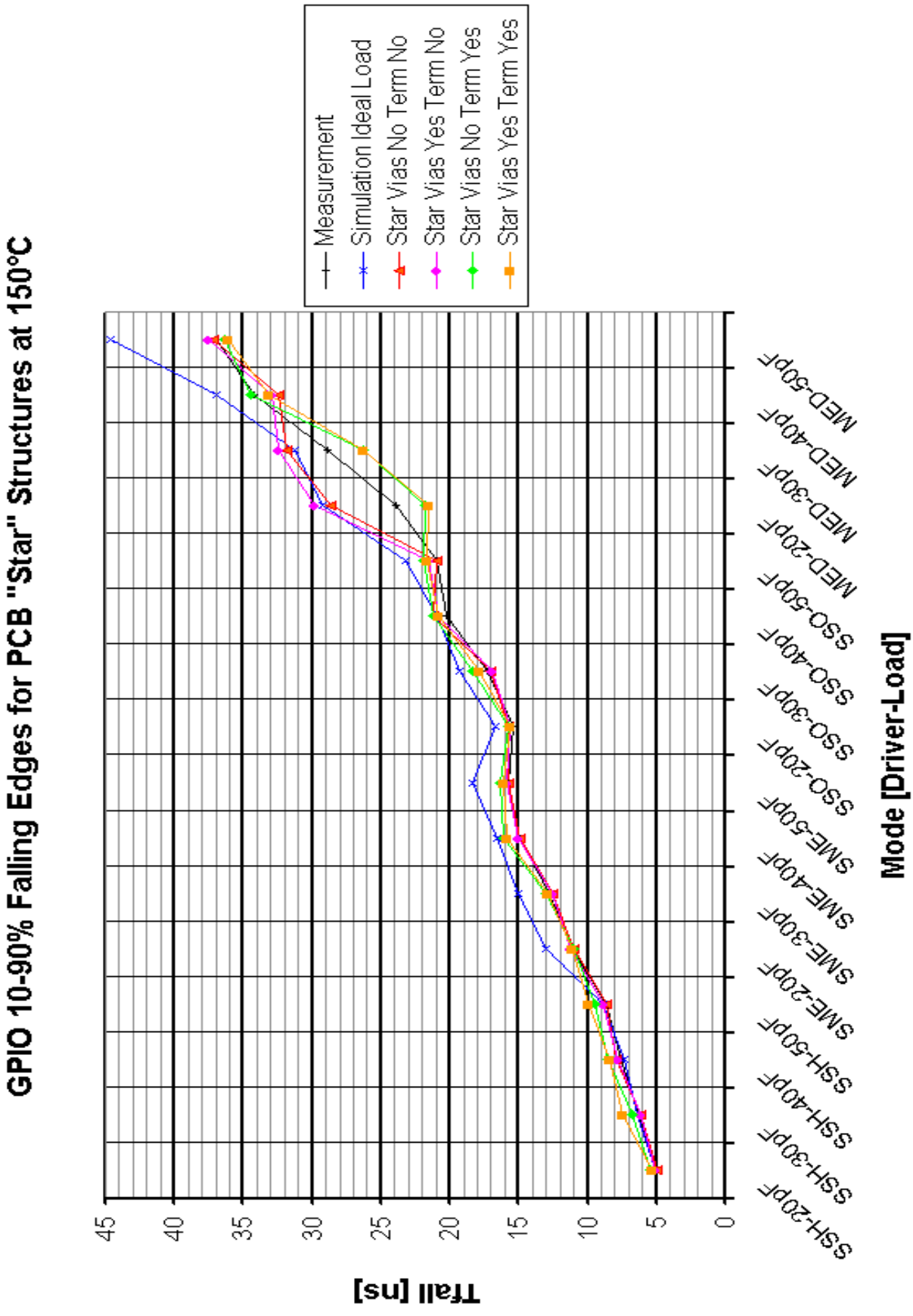


*Figure 49: GPIO fall times for “Star” layout at 150°C*

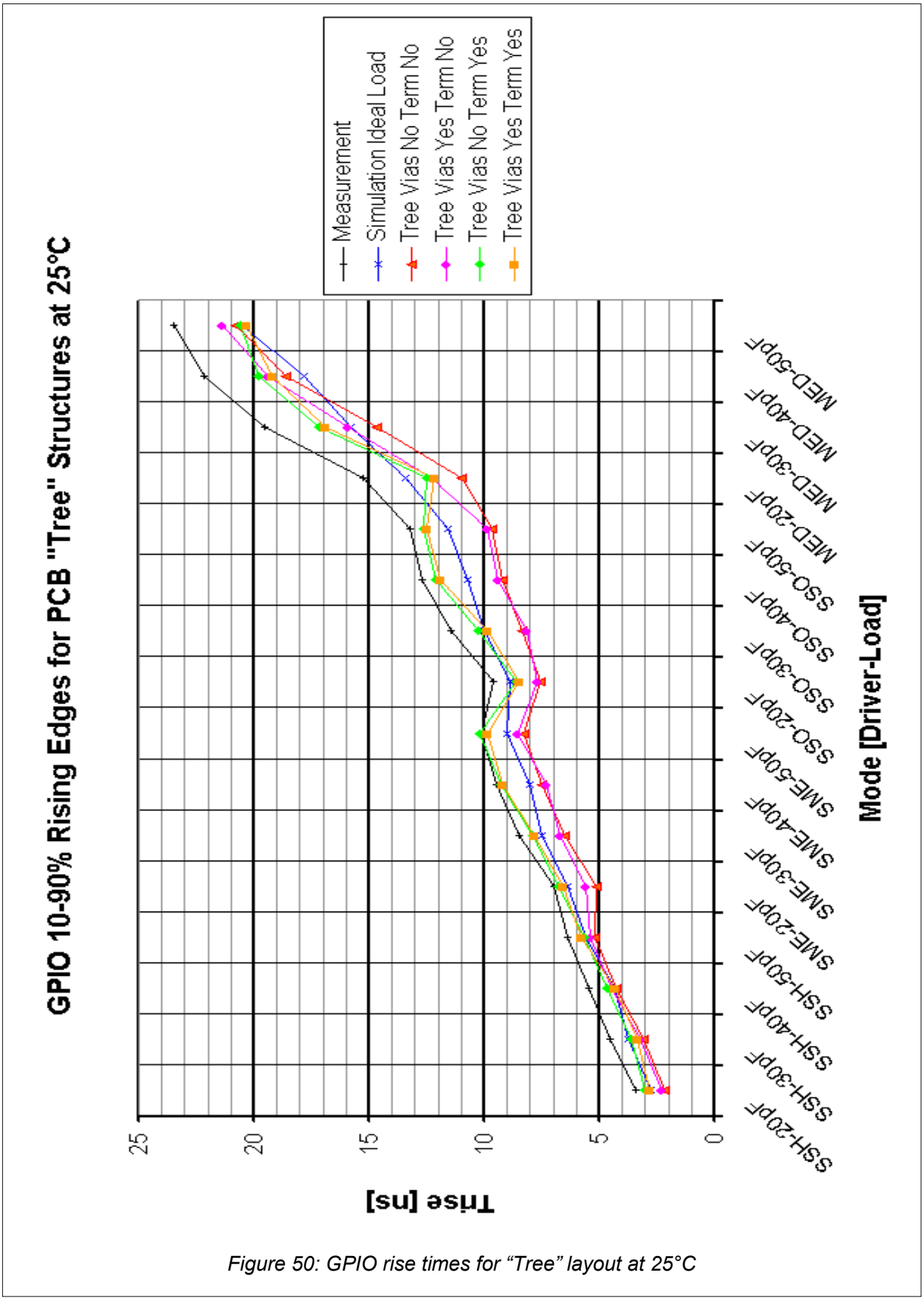


*Figure 50: GPIO rise times for “Tree” layout at 25°C*

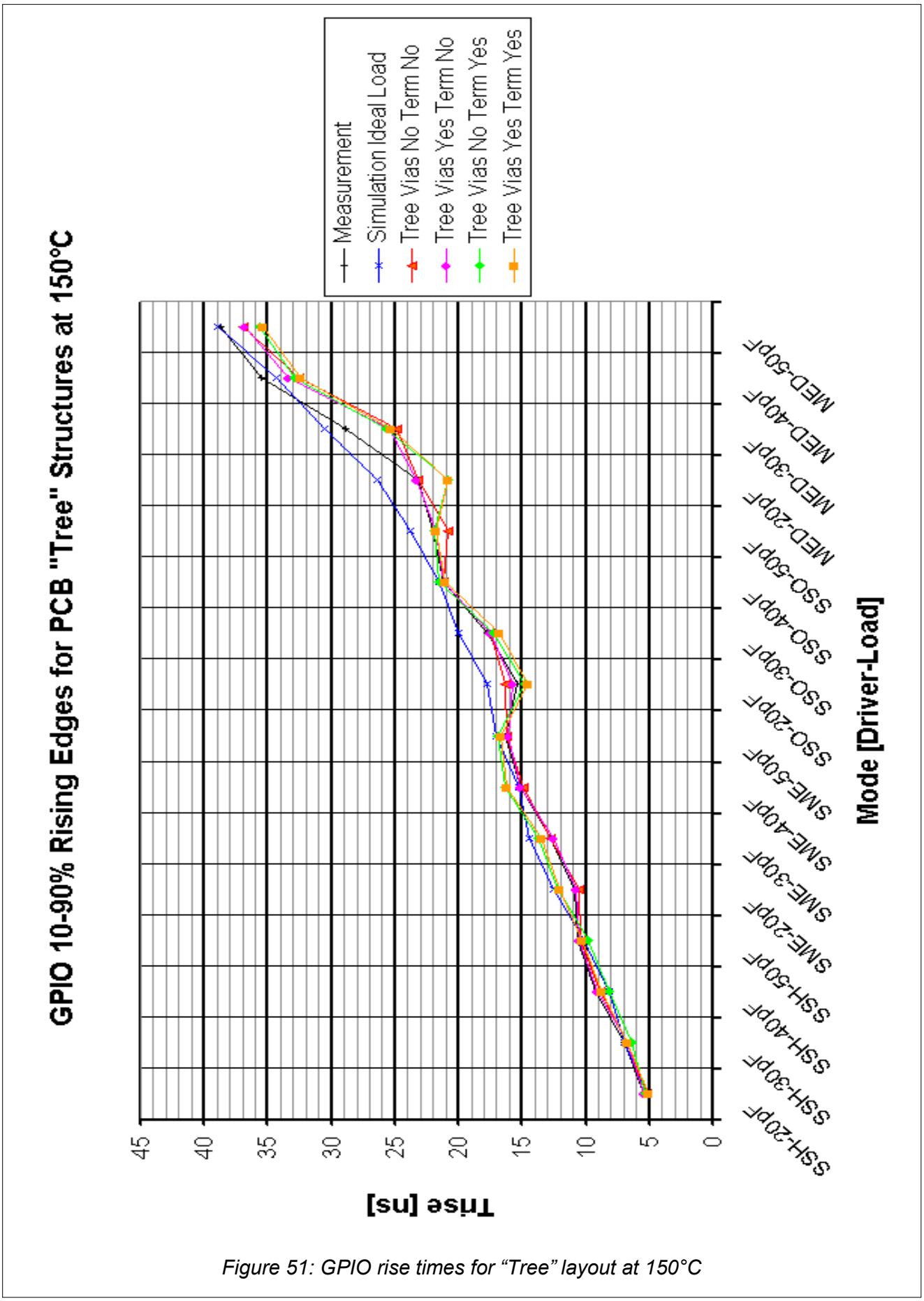


*Figure 51: GPIO rise times for “Tree” layout at 150°C*

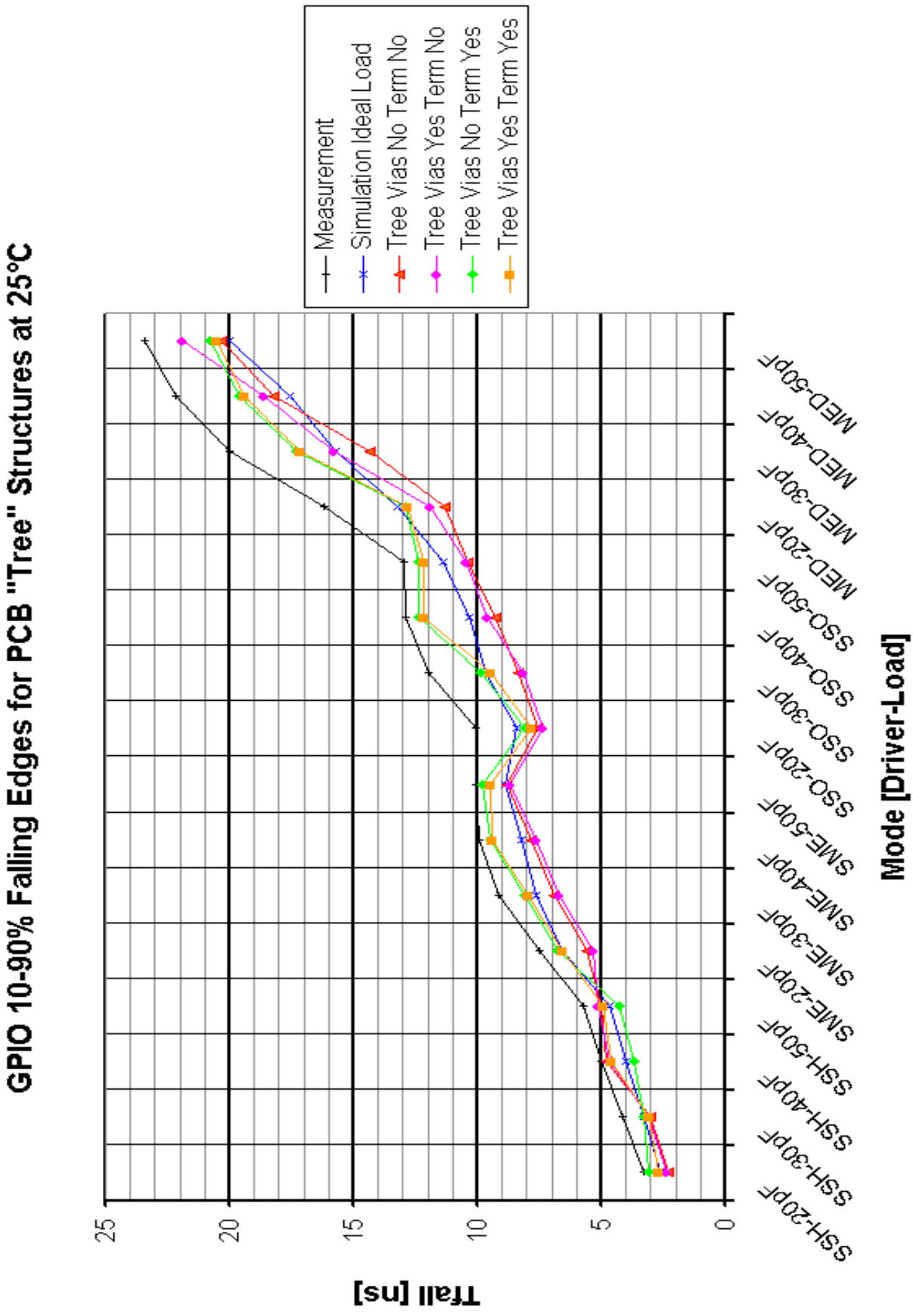


*Figure 52: GPIO fall times for “Tree” layout at 25°C*

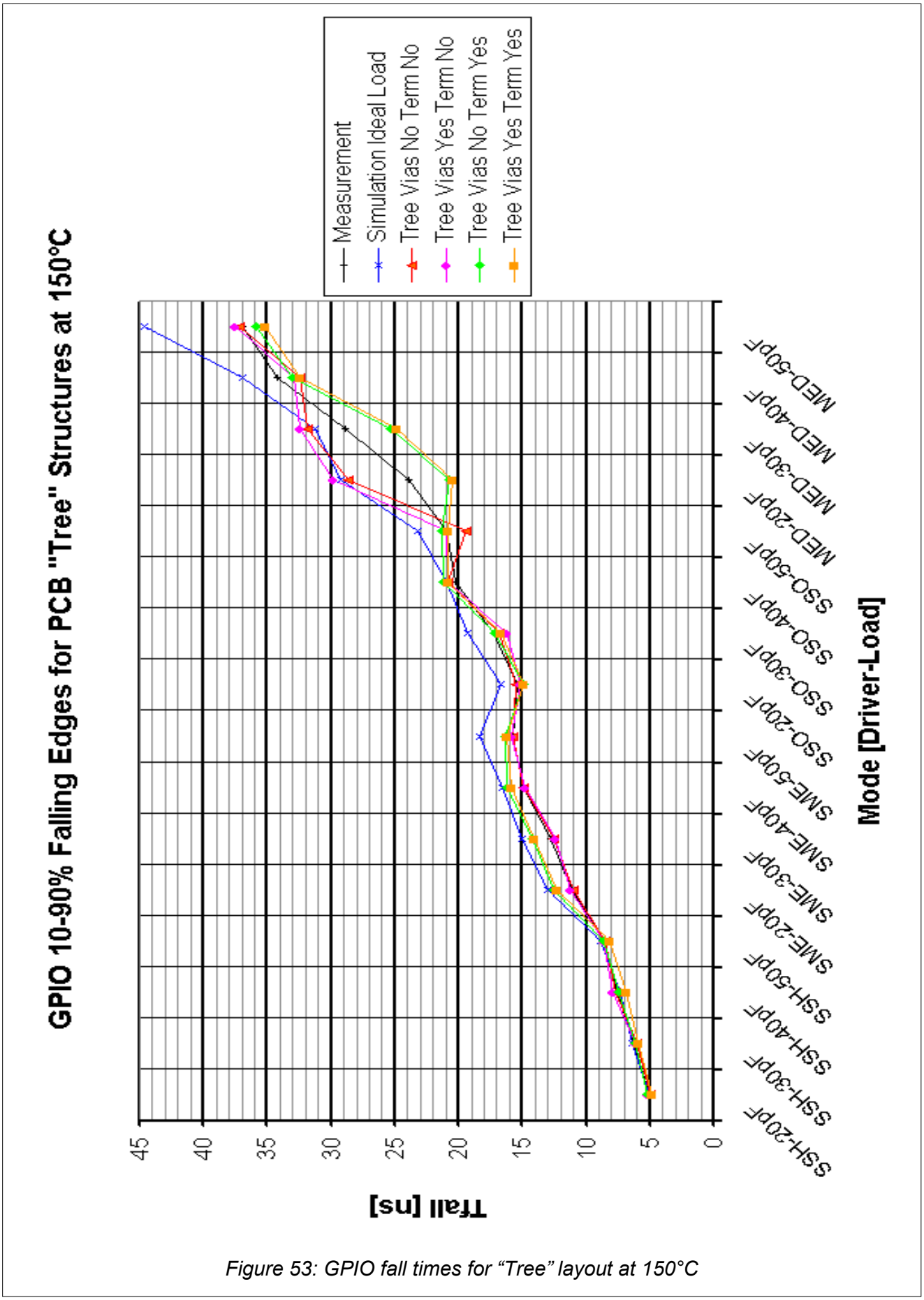


*Figure 53: GPIO fall times for "Tree" layout at 150°C*

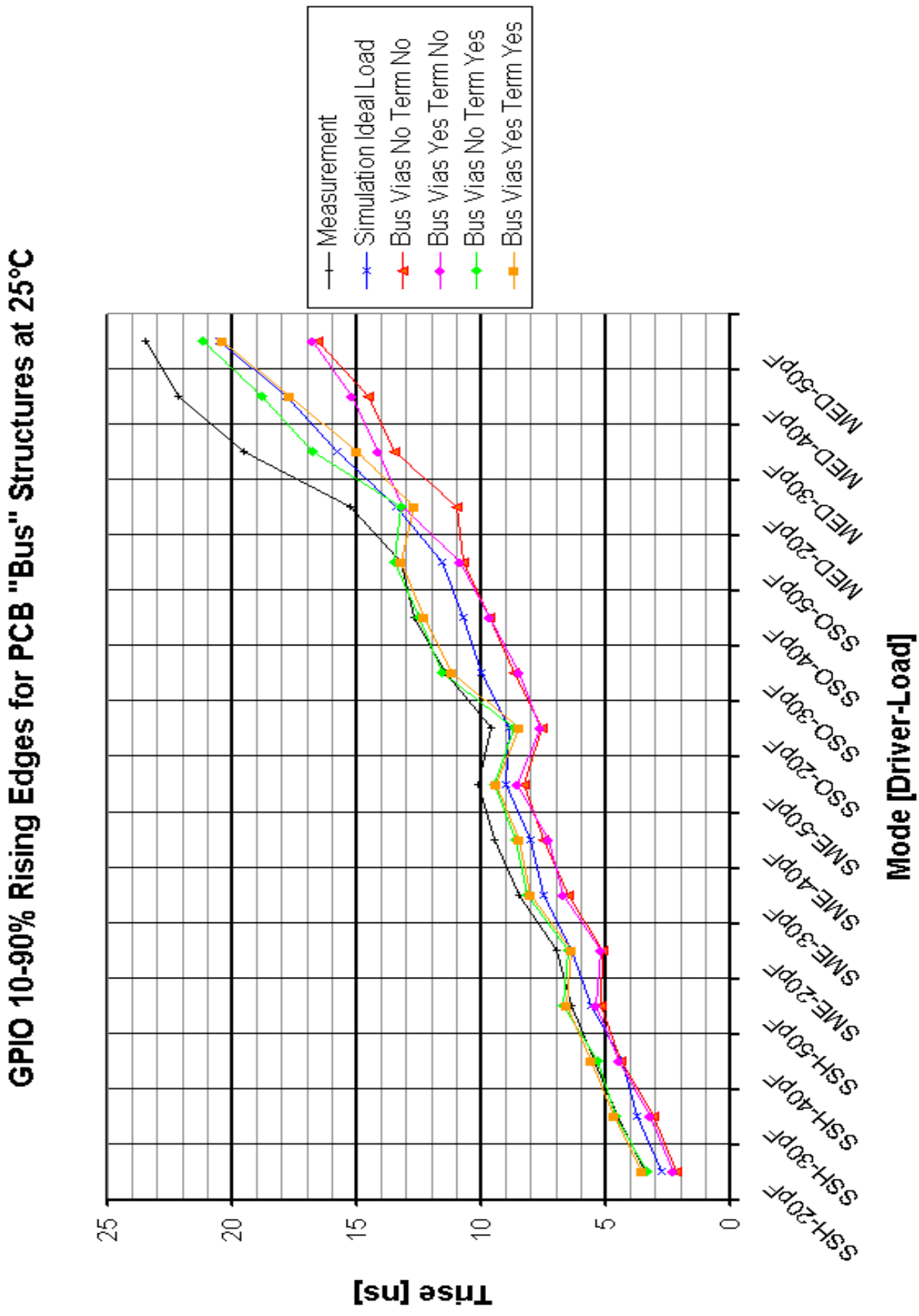


*Figure 54: GPIO rise times for “Bus” layout at 25°C*

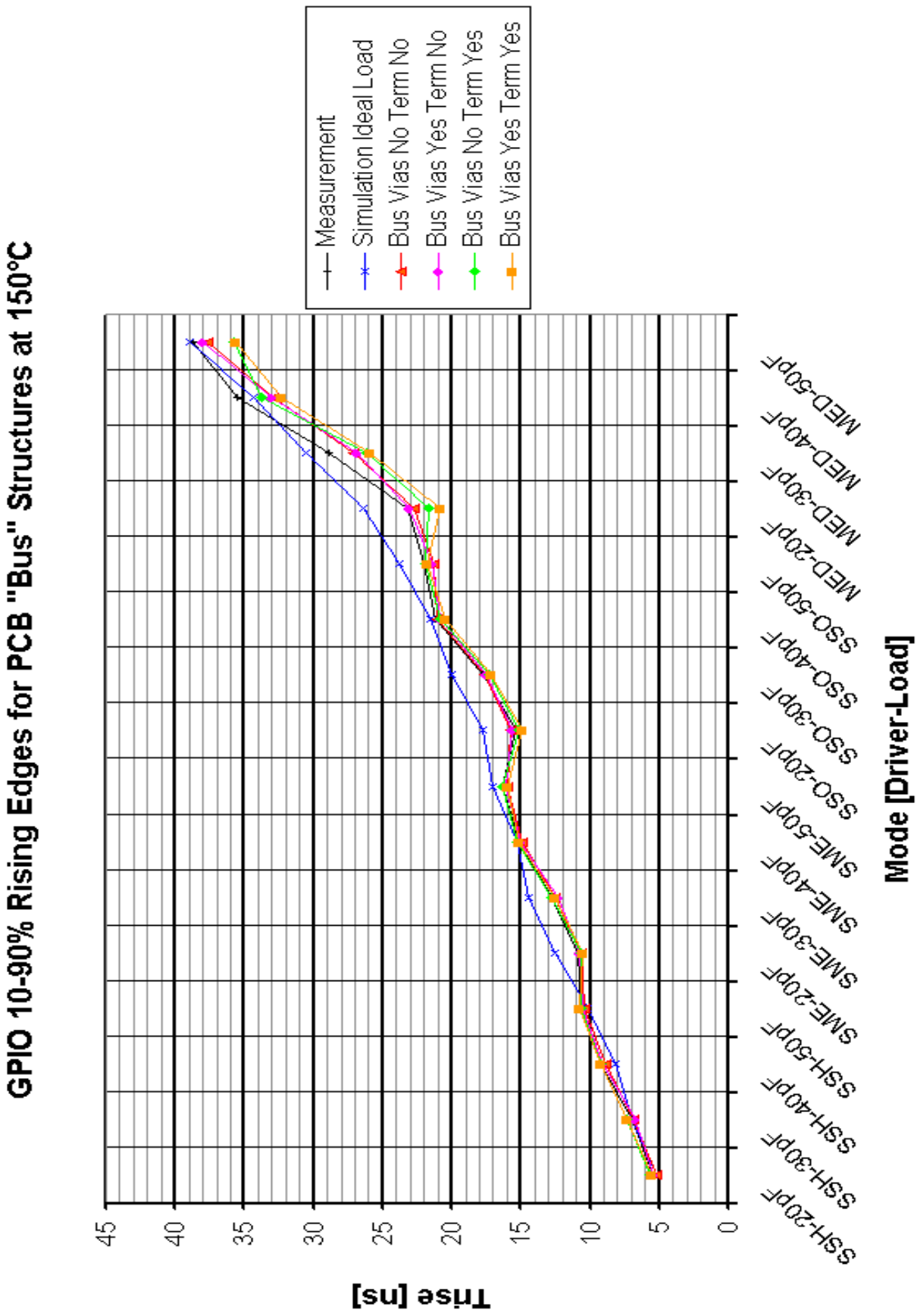


*Figure 55: GPIO rise times for “Bus” layout at 150°C*

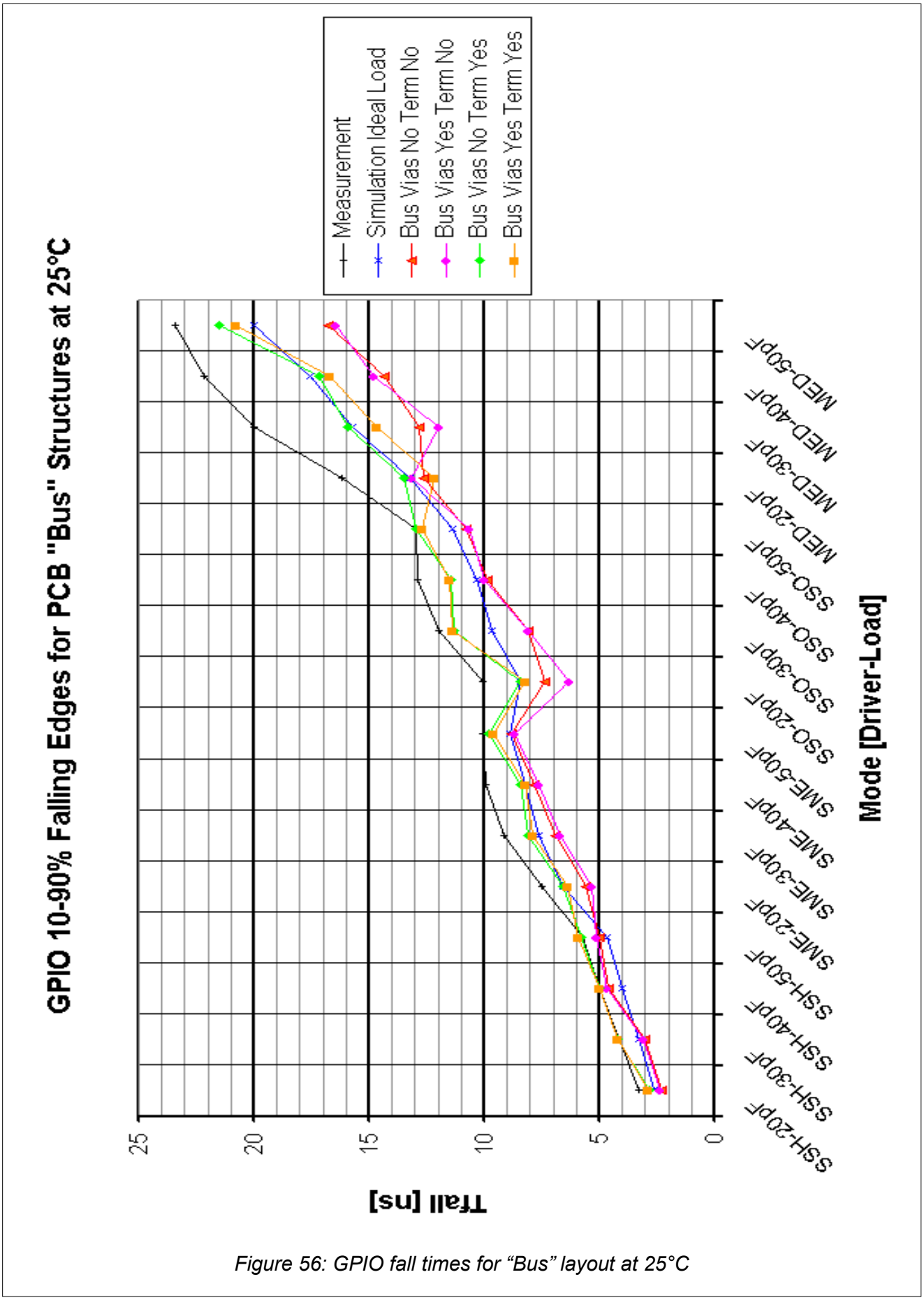


*Figure 56: GPIO fall times for “Bus” layout at 25°C*

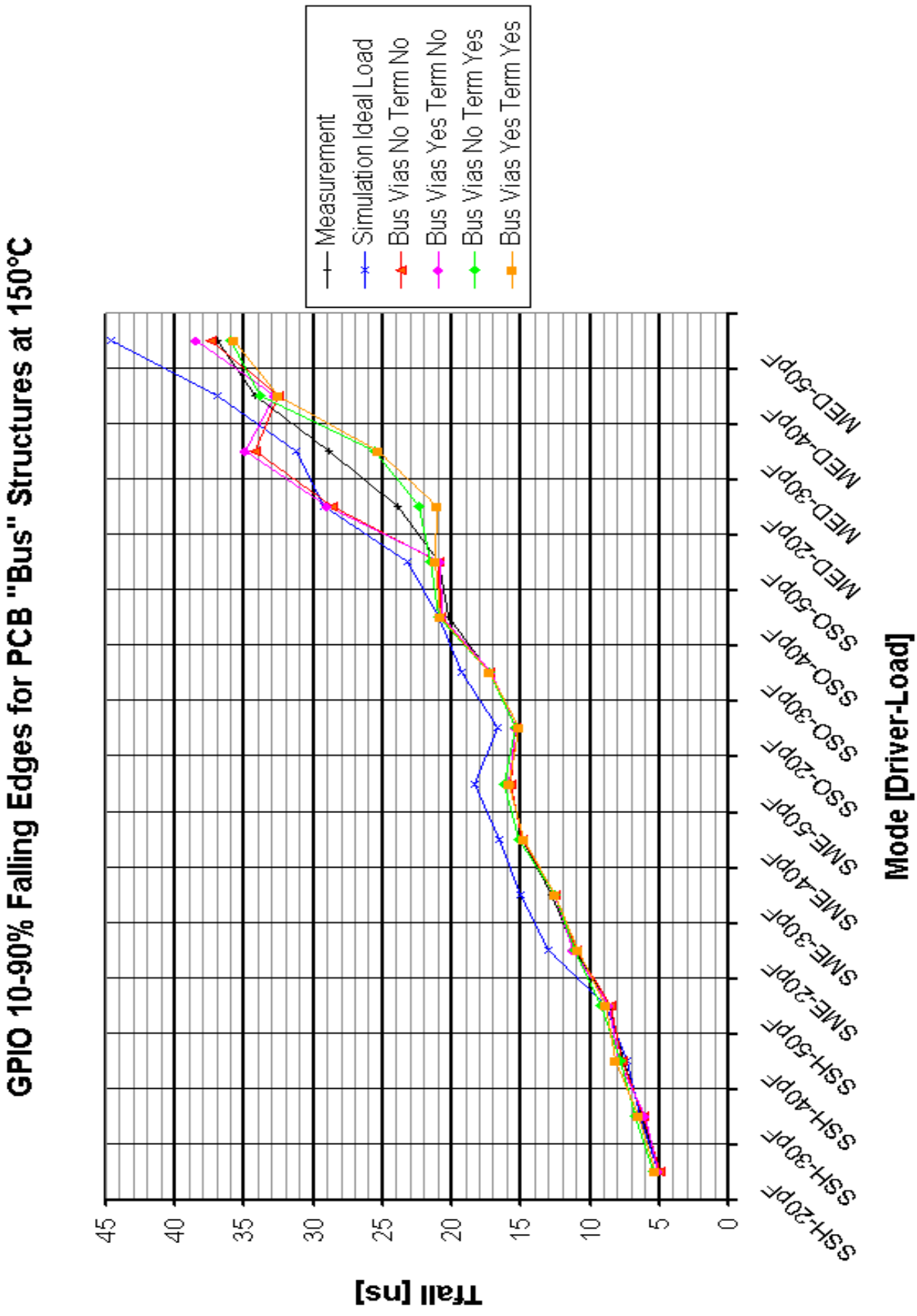


*Figure 57: GPIO fall times for “Bus” layout at 150°C*

### 4.1.3 Rise/fall waveforms

The following waveforms result from Speed2000™ timing simulations of the PCB structures described in chapter 4.1.1. Since the waveforms of the different structures are very similar, only “point-to-point” and “bus” structures are presented here with loads of 20pF and 40pF. However, the influence of via contacts and termination resistors is visible from the waveforms.

Each of Fig. 59-90 contains 4 waveforms for a given pad type (CLKOUT or GPOI), a given ambient temperature (25°C or 150°C) and a given driver strength. Depending on these settings, certain clock frequencies can be driven or not. The waveforms show one of 3 frequencies: 10MHz, 5MHz or 2.5MHz – whatever is the highest frequency for a given setting which shows an acceptable signal integrity (i.e. high and low voltage levels of 5.0V and 0.0V are reached during switching).

The 4 configurations shown in one figure are distributed as follows:

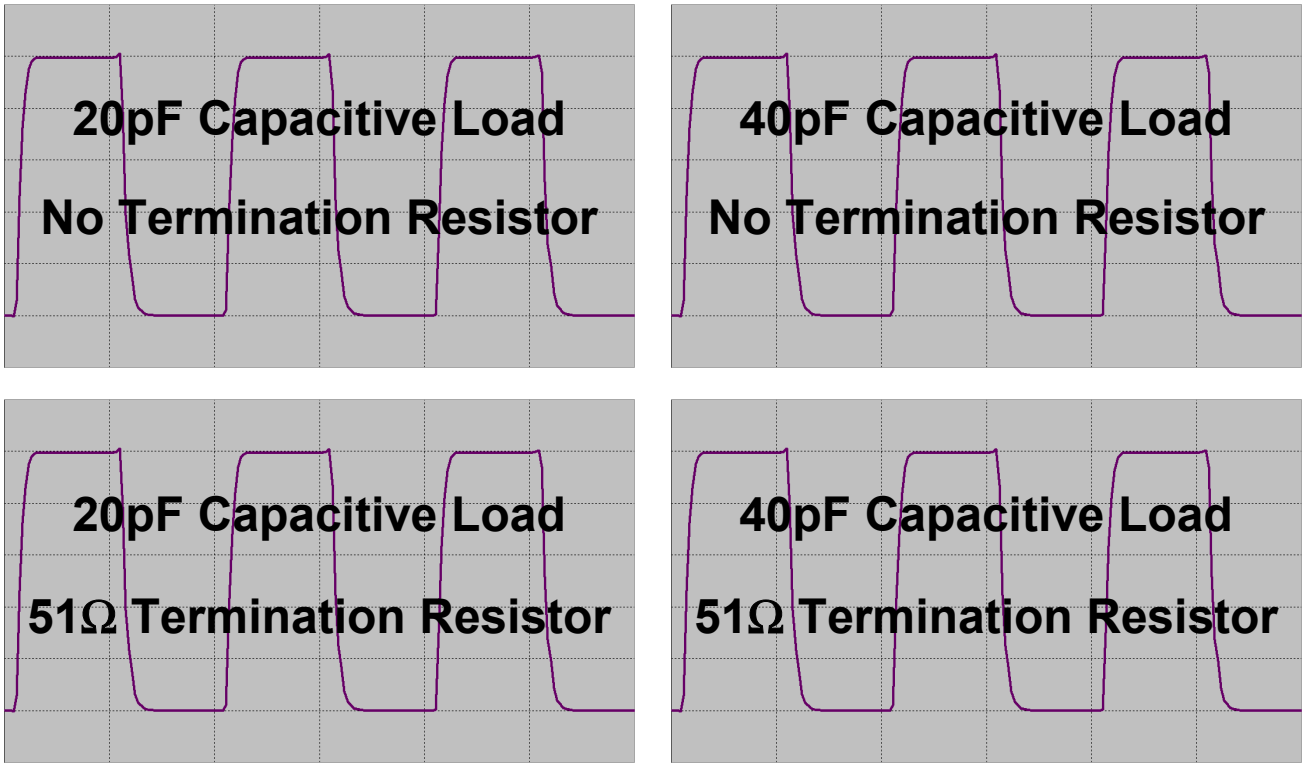


*Figure 58: General grouping of waveform configurations*

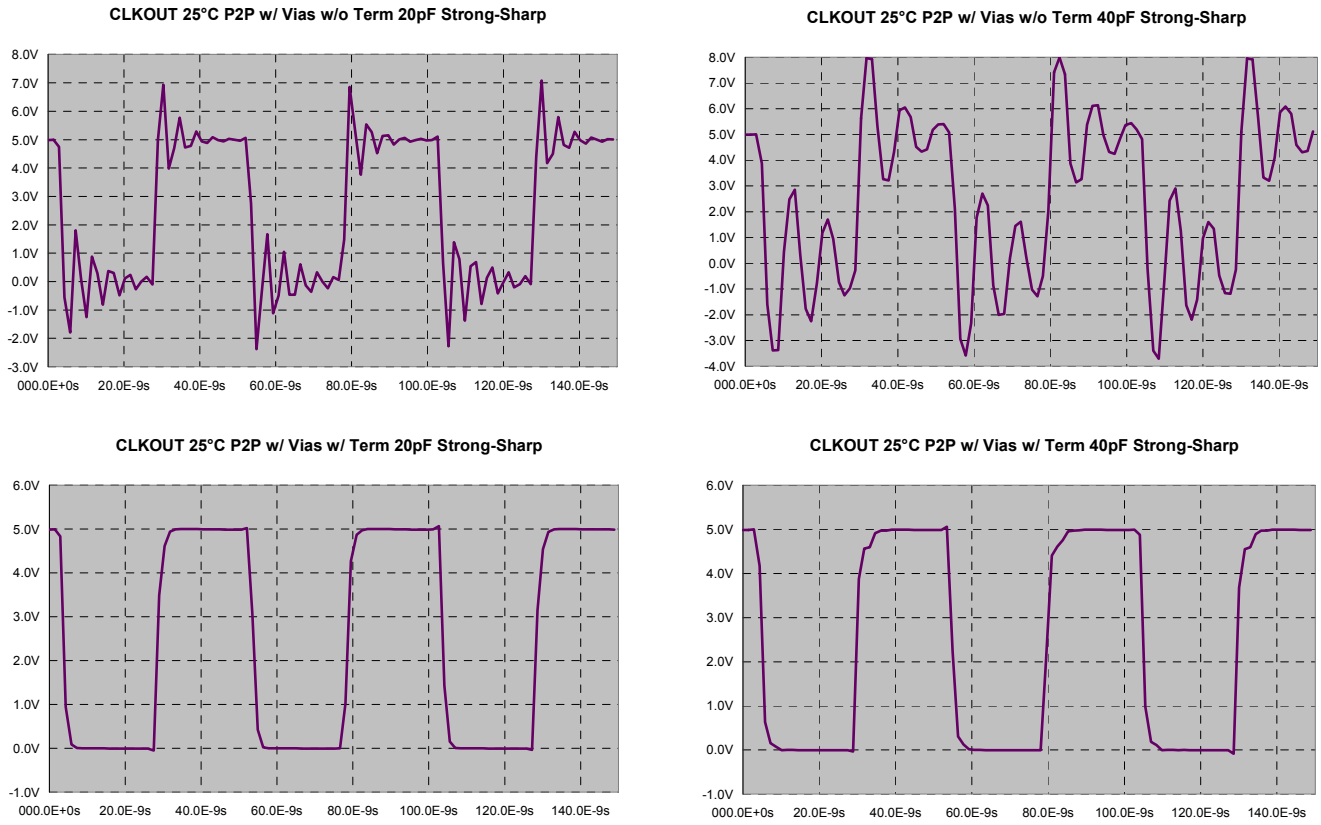


*Figure 59: Waveforms CLKOUT 20 MHz "Strong-Sharp" / "Point-to-Point" at 25°C ambient temperature*

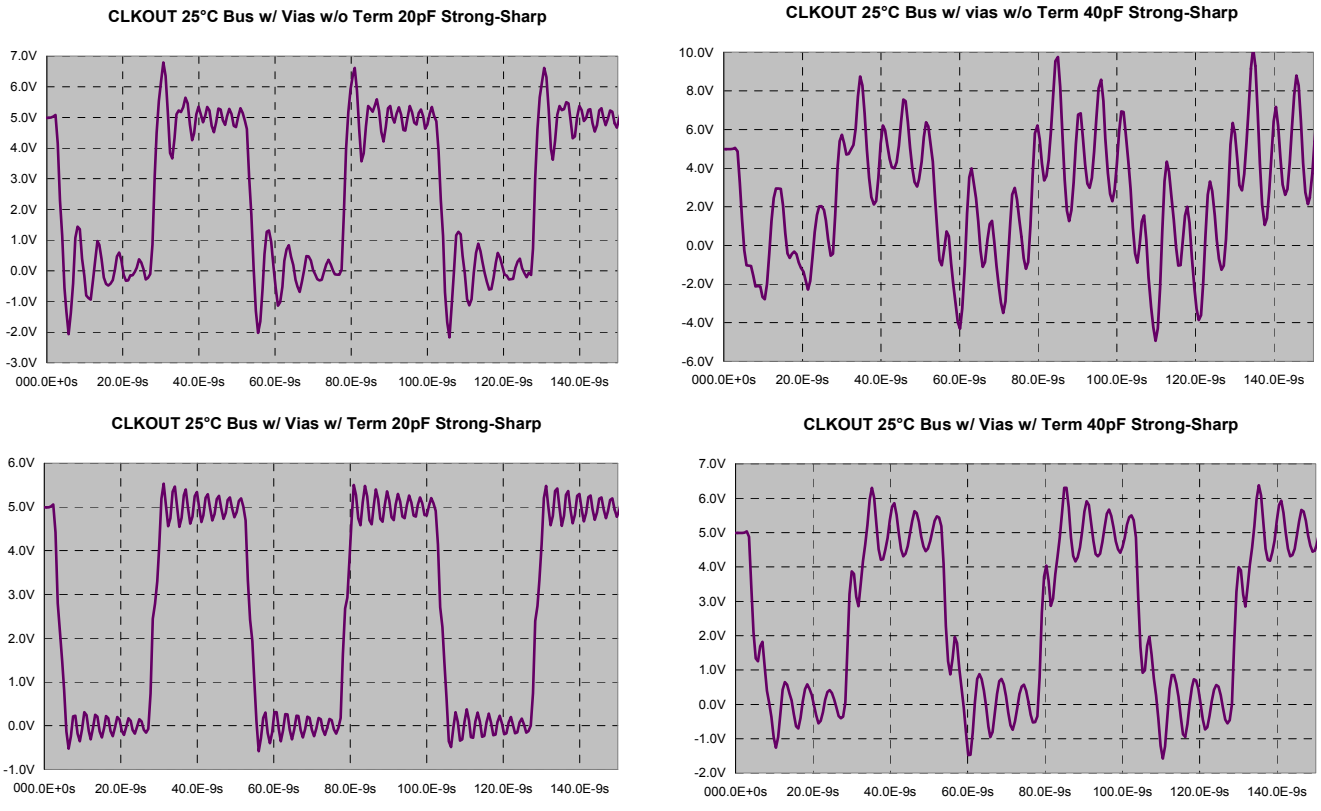


*Figure 60: Waveforms CLKOUT 20 MHz "Strong-Sharp" / "Bus" at 25°C ambient temperature*

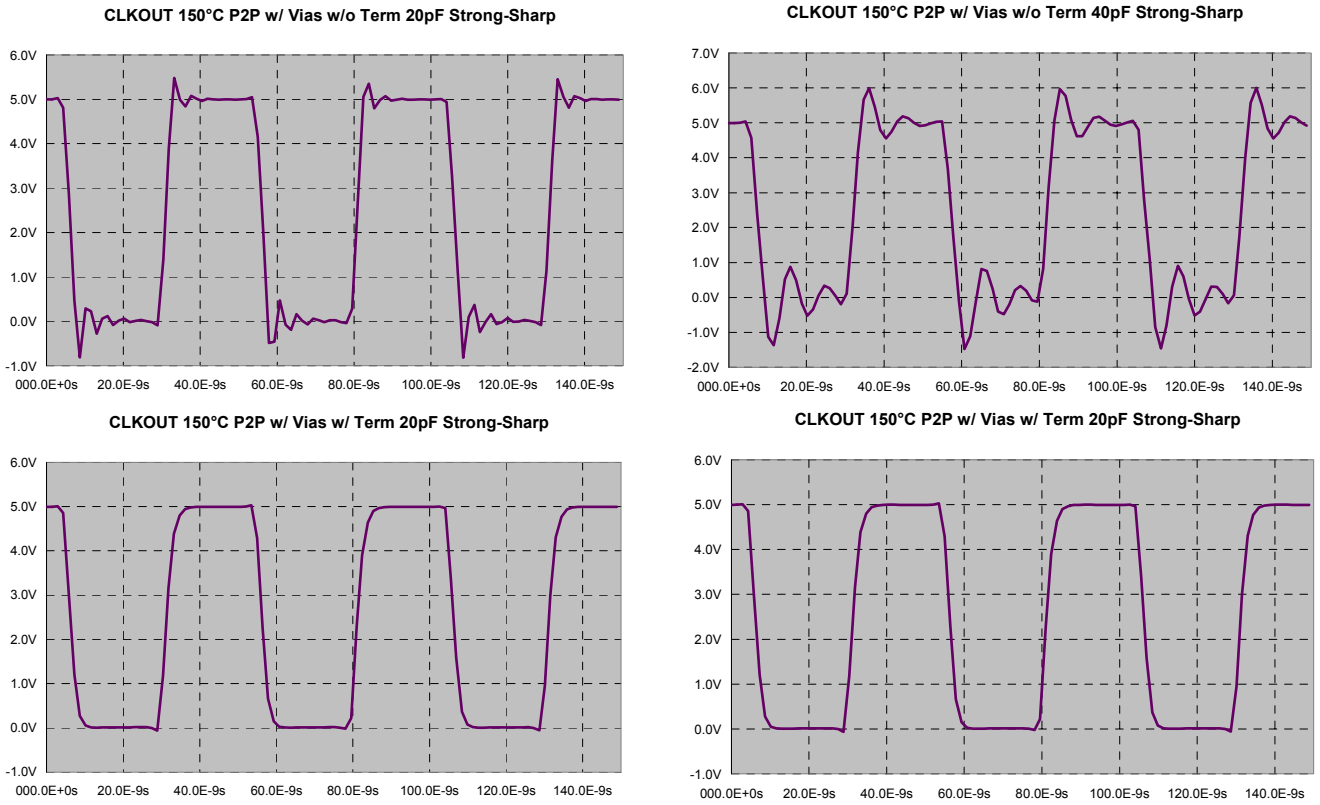


*Figure 61: Waveforms CLKOUT 20 MHz "Strong-Sharp" / "Point-to-Point" at 150°C ambient temperat.*

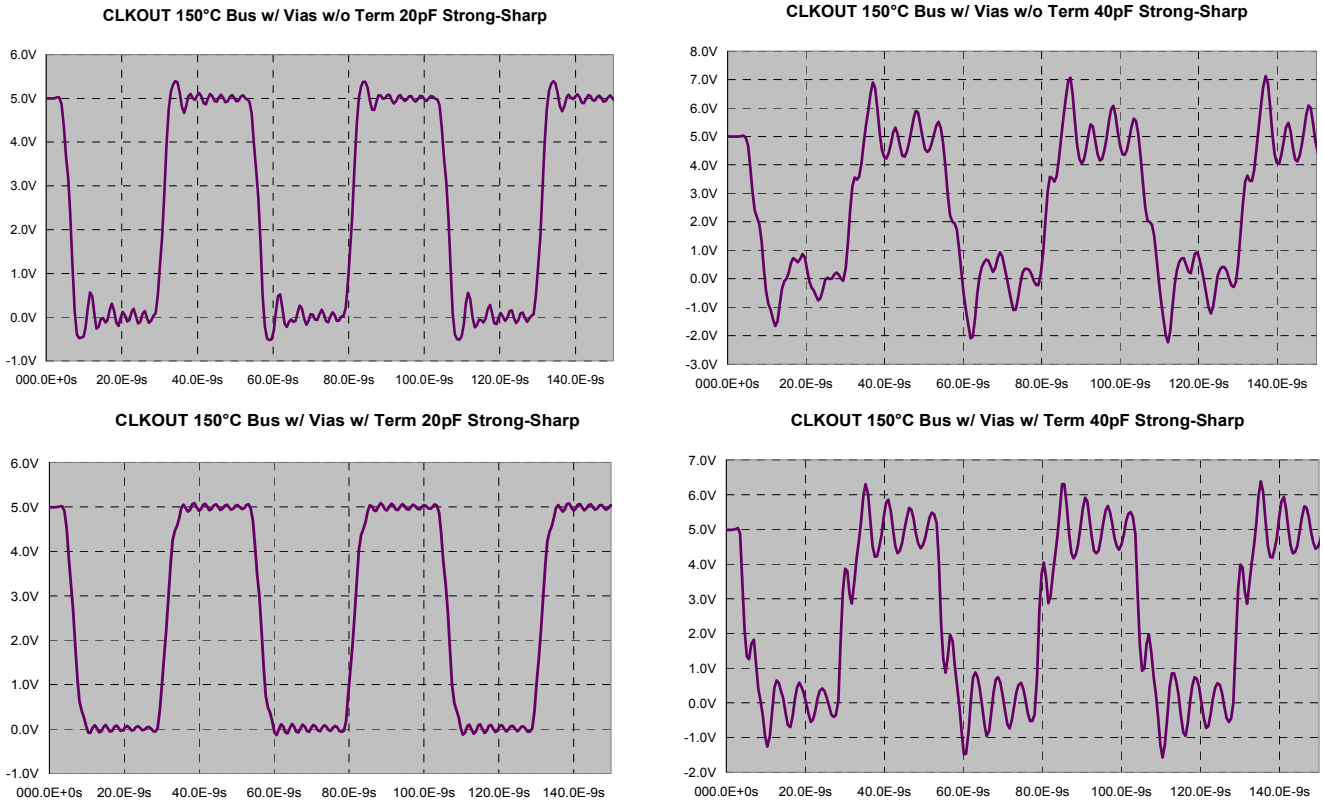


*Figure 62: Waveforms CLKOUT 20 MHz "Strong-Sharp" / "Bus" at 150°C ambient temperature*

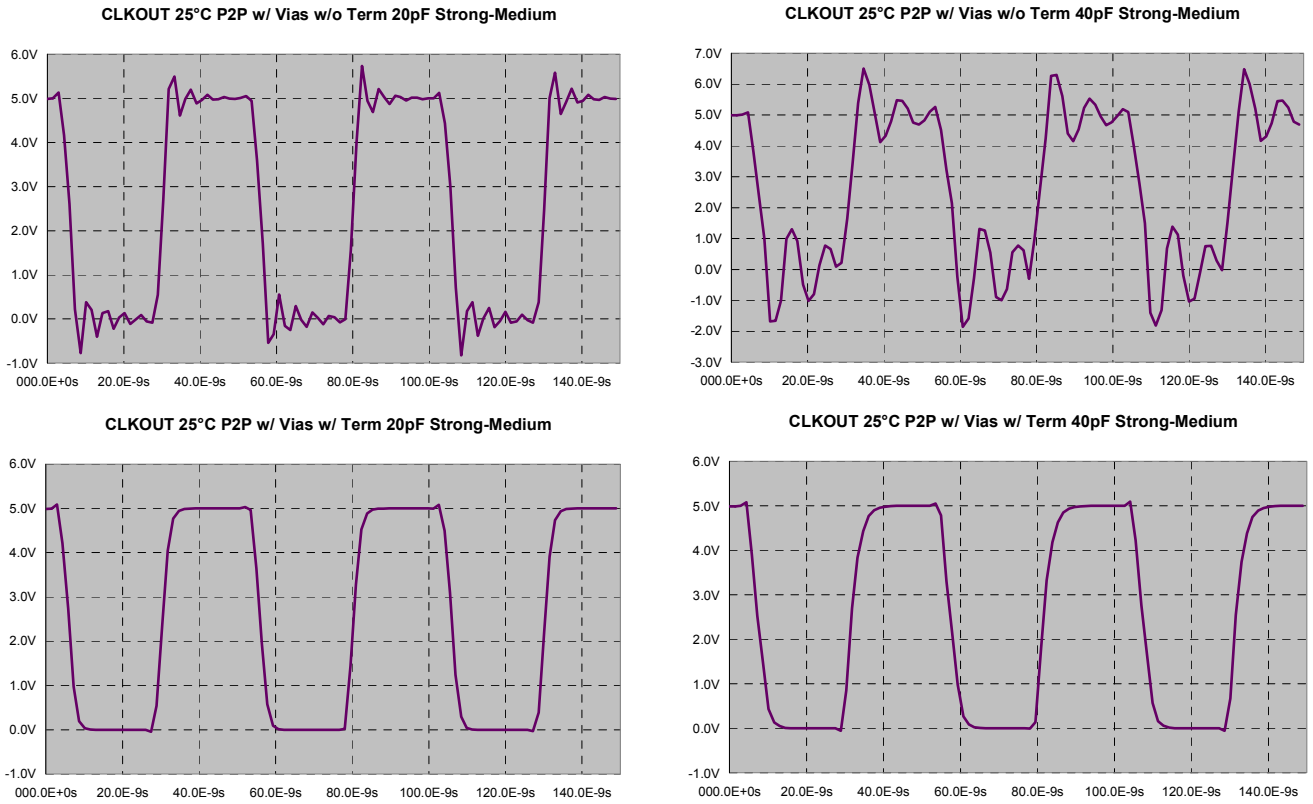


*Figure 63: Waveforms CLKOUT 20 MHz "Strong-Medium" / "Point-to-Point" 25°C ambient temperature*

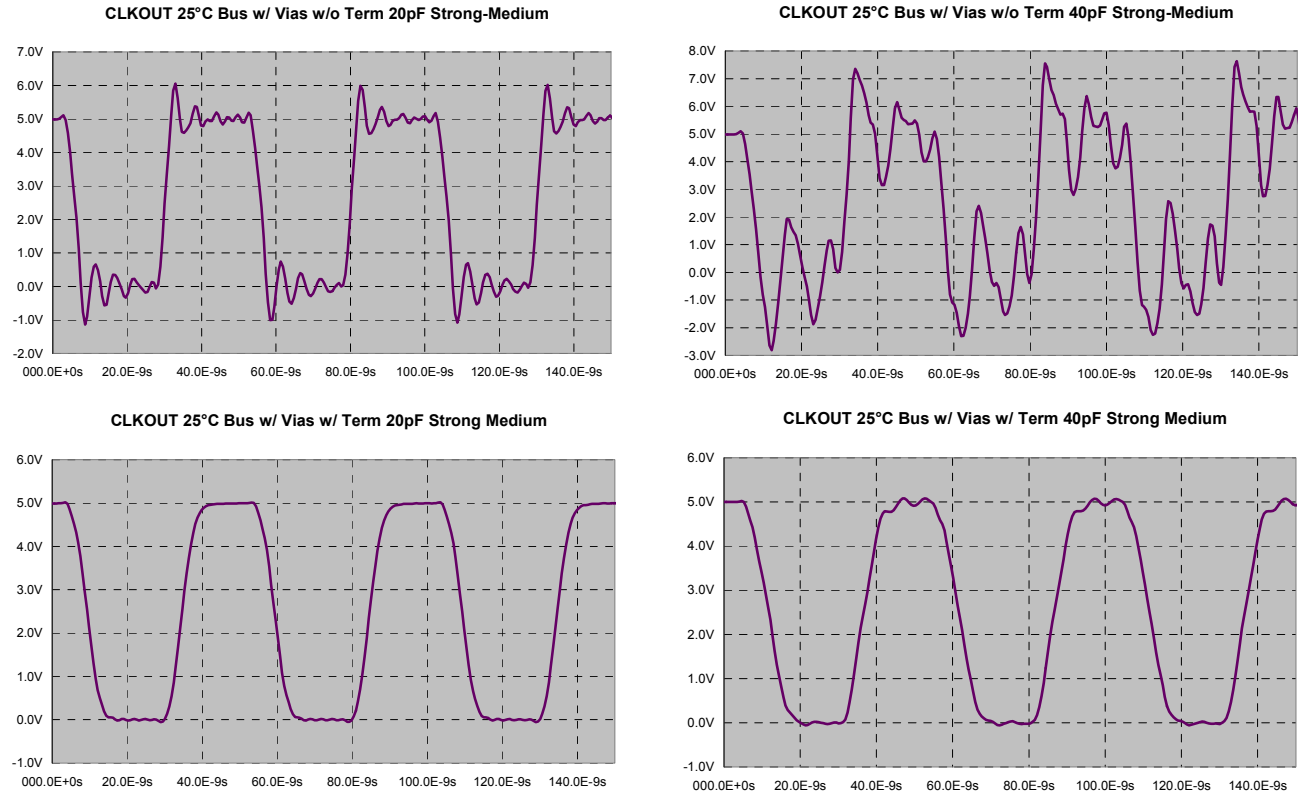


*Figure 64: Waveforms CLKOUT 20 MHz "Strong-Medium" / "Bus" at 25°C ambient temperature*

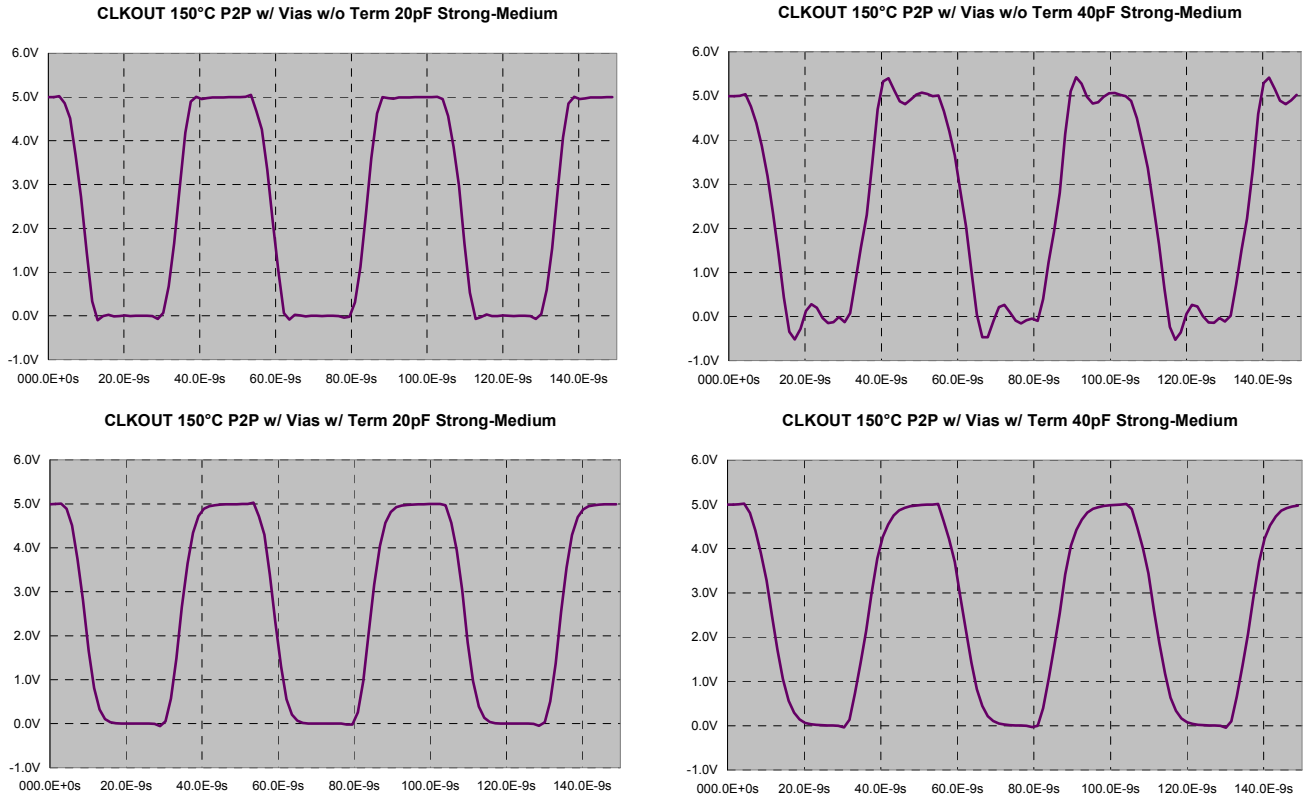


*Figure 65: Waveforms CLKOUT 20 MHz "Strong-Medium" / "Point-to-Point" at 150°C ambient temper.*

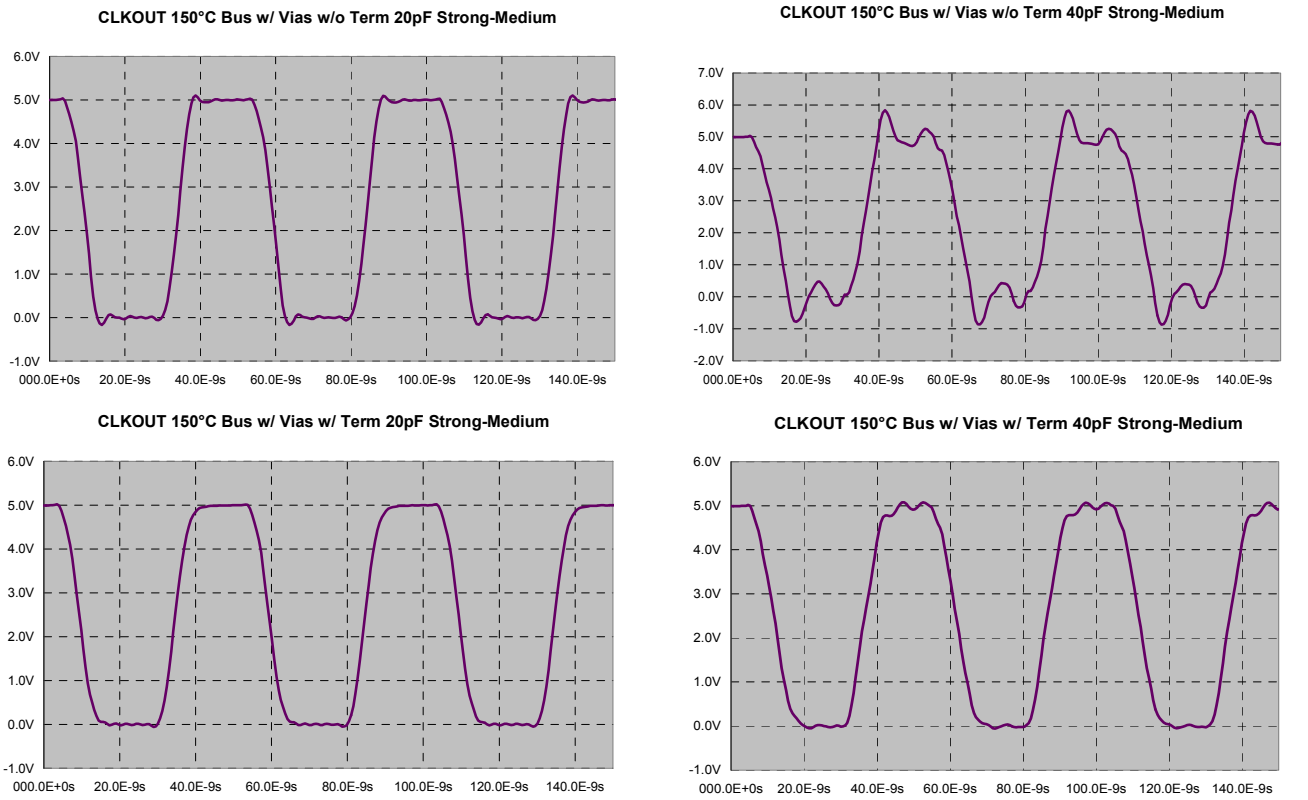


*Figure 66: Waveforms CLKOUT 20 MHz "Strong-Medium" / "Bus" at 150°C ambient temperature*

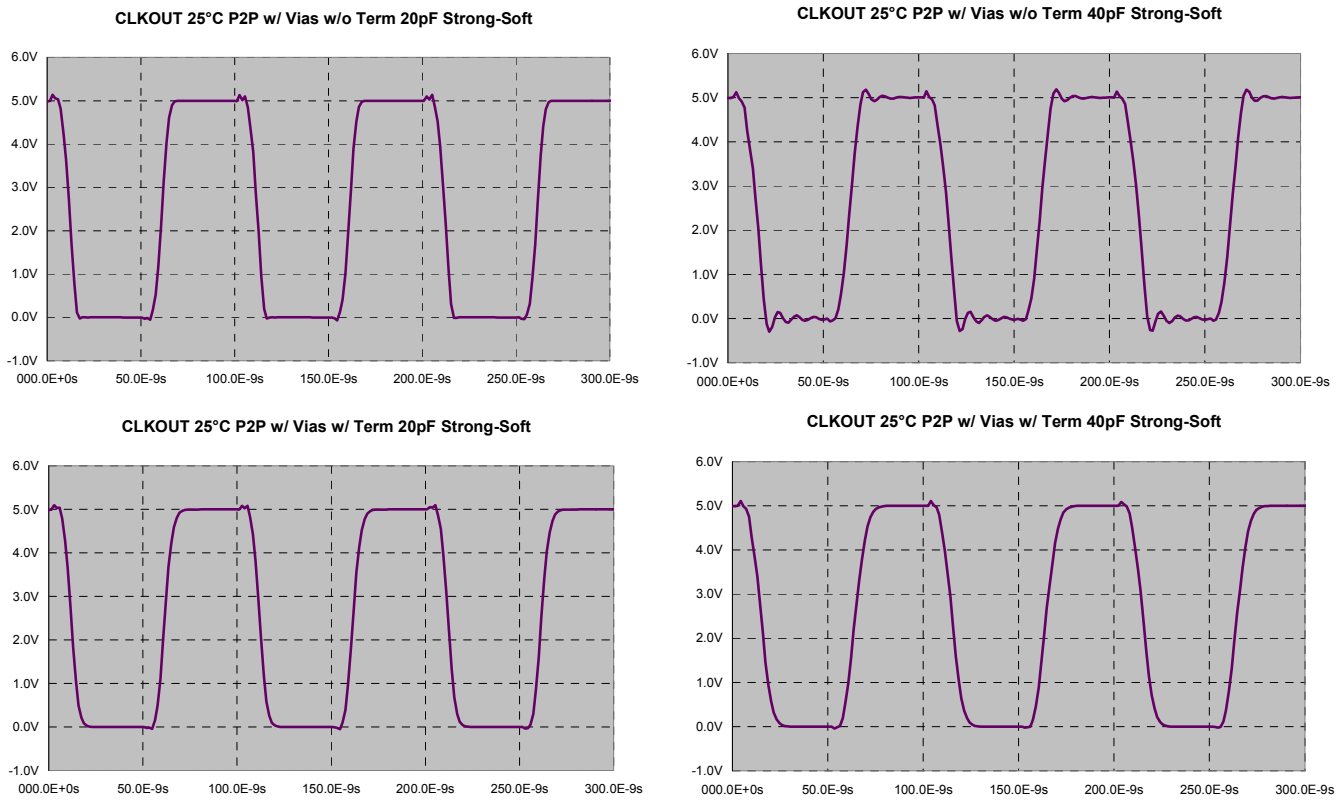


*Figure 67: Waveforms CLKOUT 10 MHz "Strong-Soft" / "Point-to-Point" at 25°C ambient temperature*

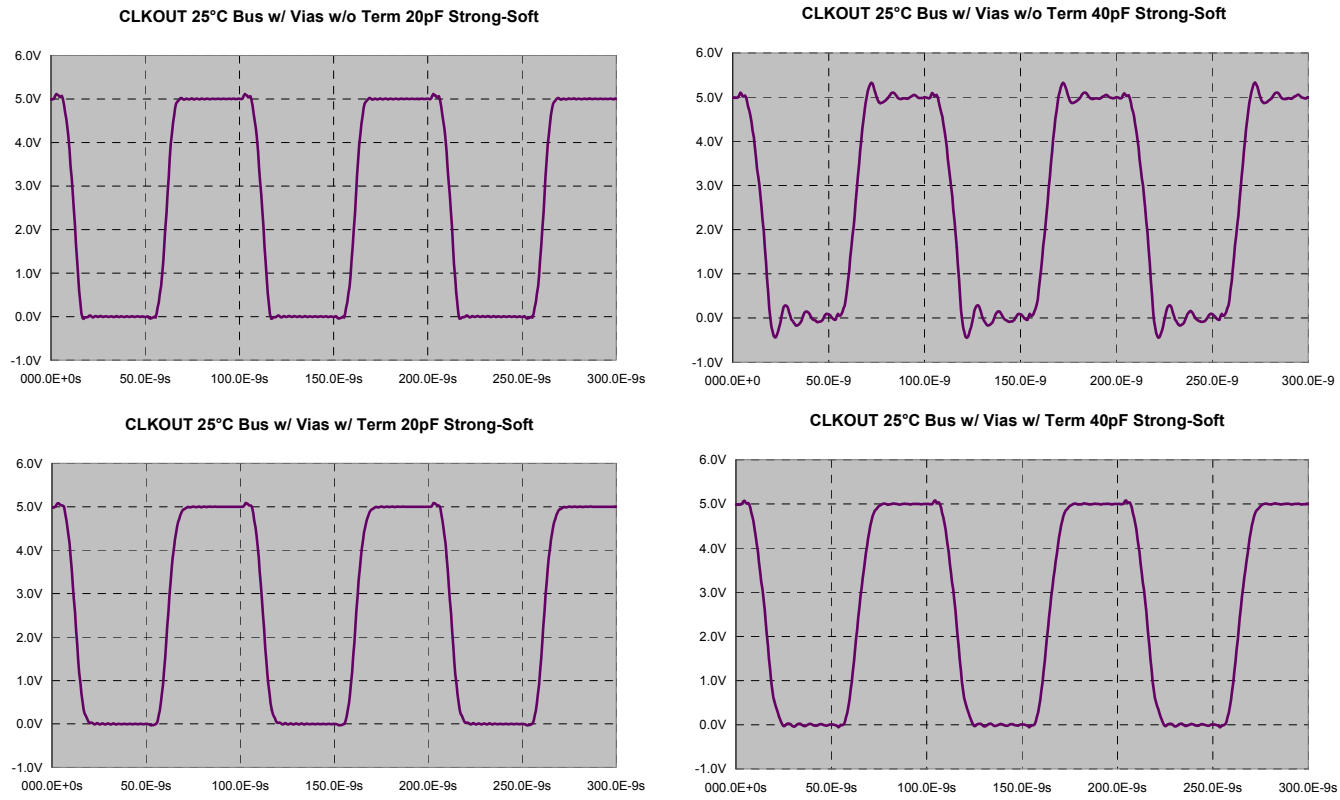


*Figure 68: Waveforms CLKOUT 10 MHz "Strong-Soft" / "Bus" at 25°C ambient temperature*

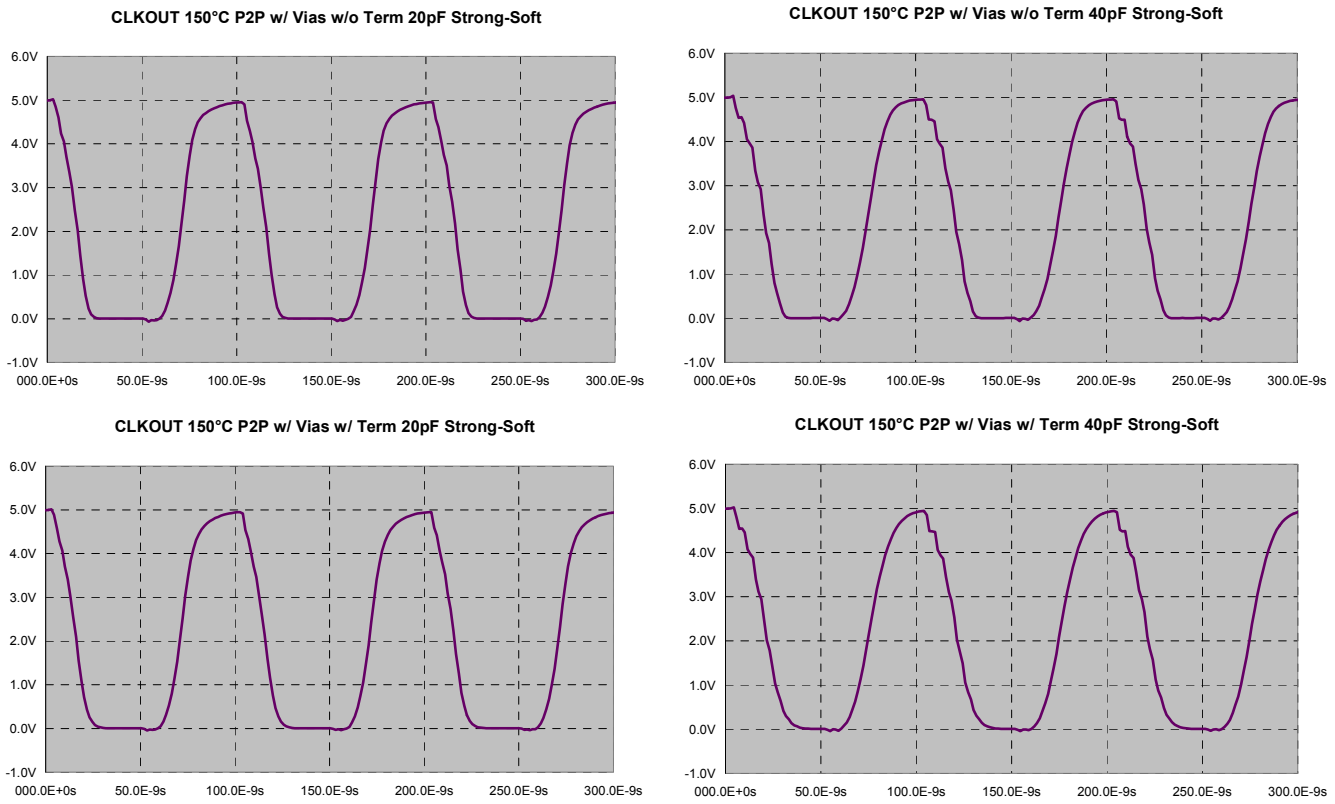


*Figure 69: Waveforms CLKOUT 10 MHz "Strong-Soft" / "Point-to-Point" at 150°C ambient temperature*

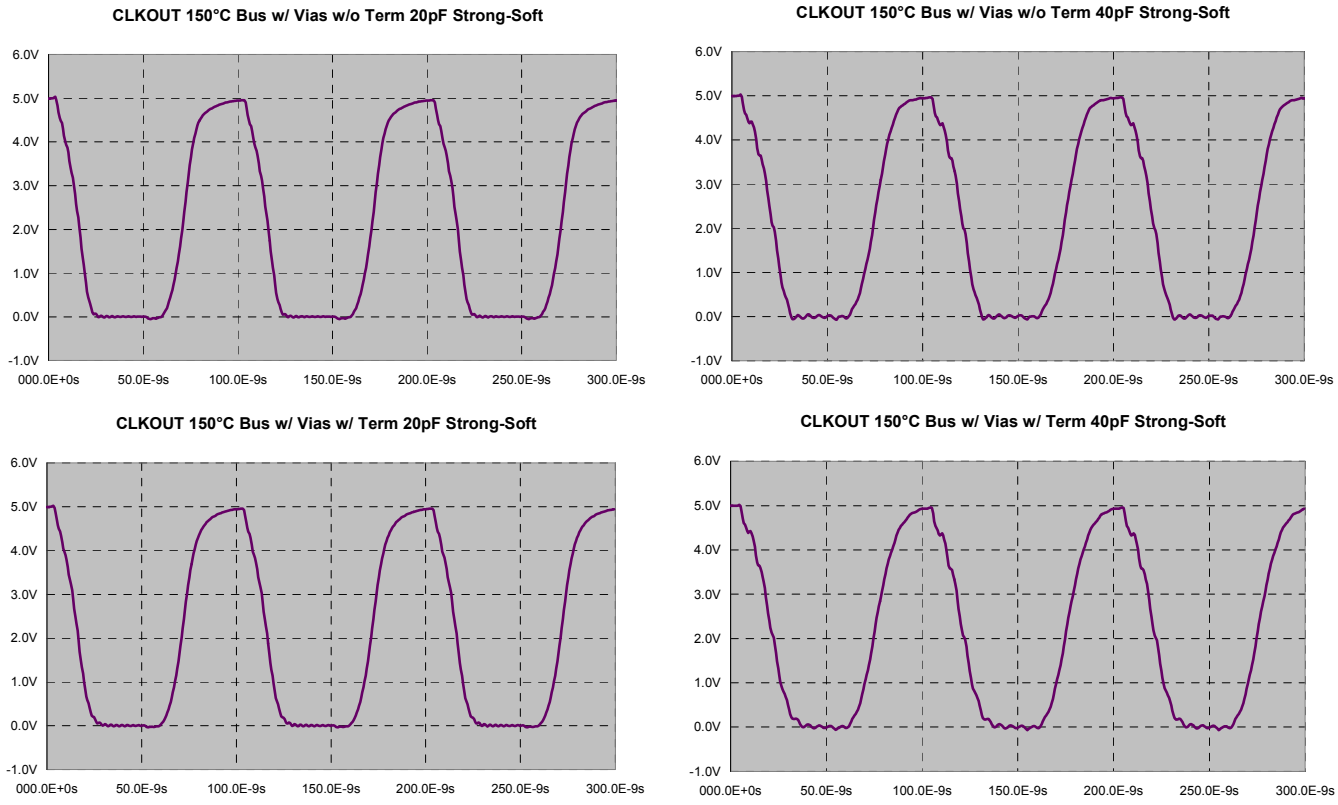


*Figure 70: Waveforms CLKOUT 10 MHz "Strong-Soft" / "Bus" at 150°C ambient temperature*

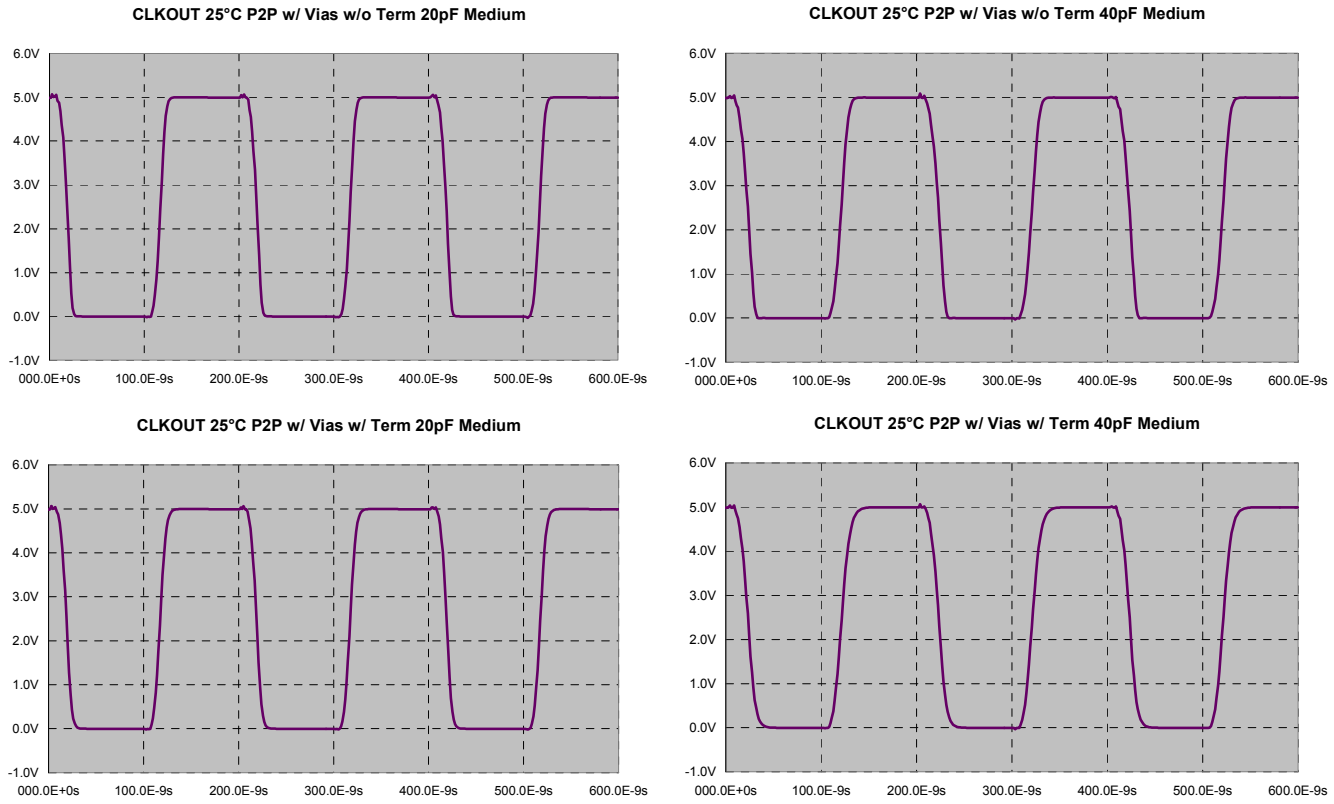


*Figure 71: Waveforms CLKOUT 5 MHz "Medium" / "Point-to-Point" at 25°C ambient temperature*

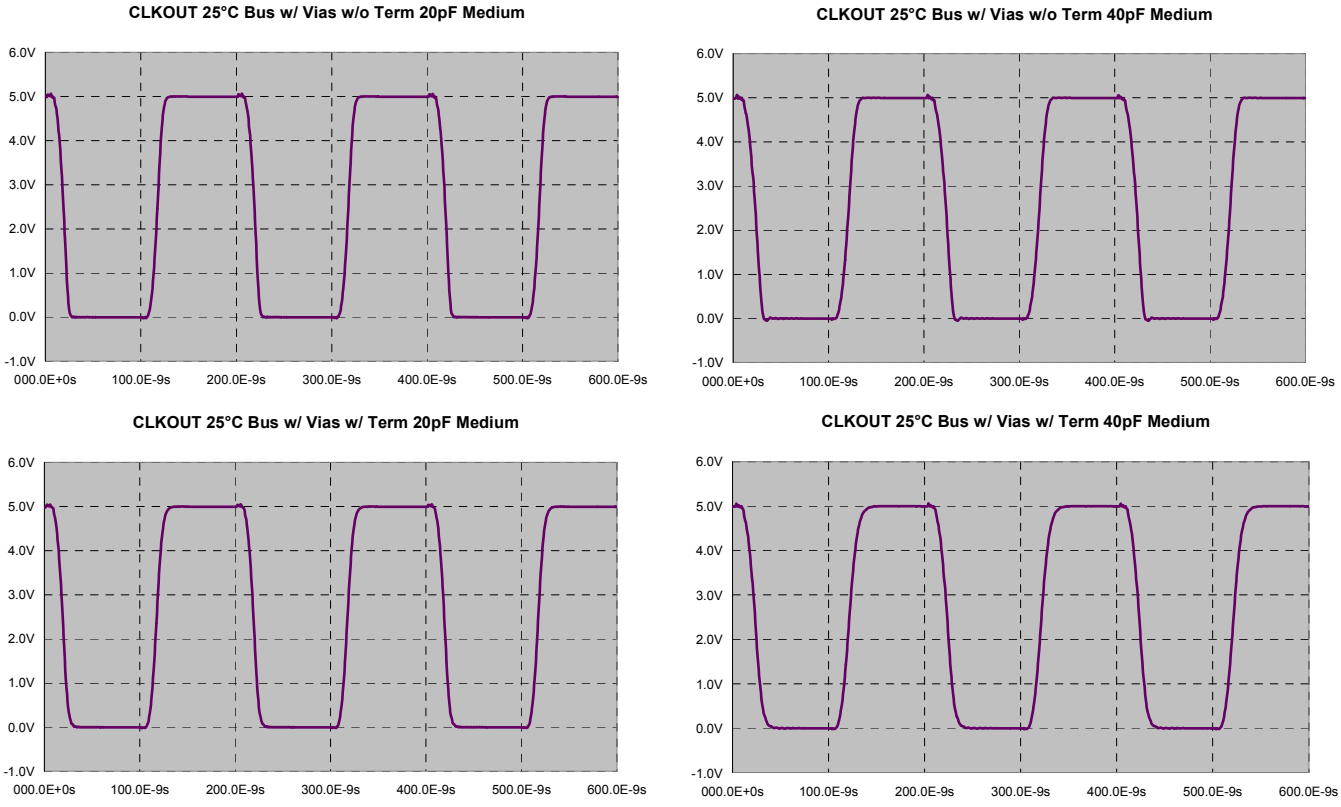


*Figure 72: Waveforms CLKOUT 5 MHz "Medium" / "Bus" at 25°C ambient temperature*

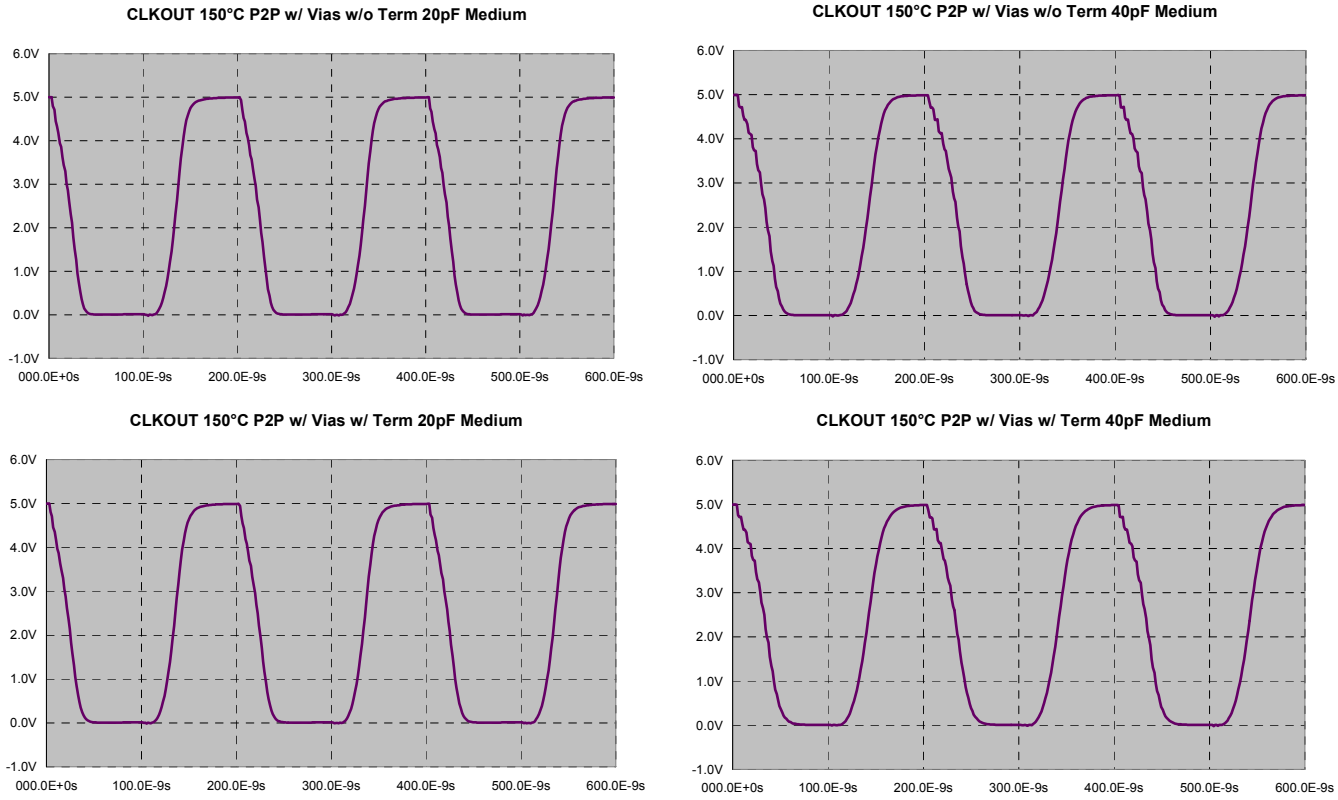


*Figure 73: Waveforms CLKOUT 5 MHz "Medium" / "Point-to-Point" at 150°C ambient temperature*

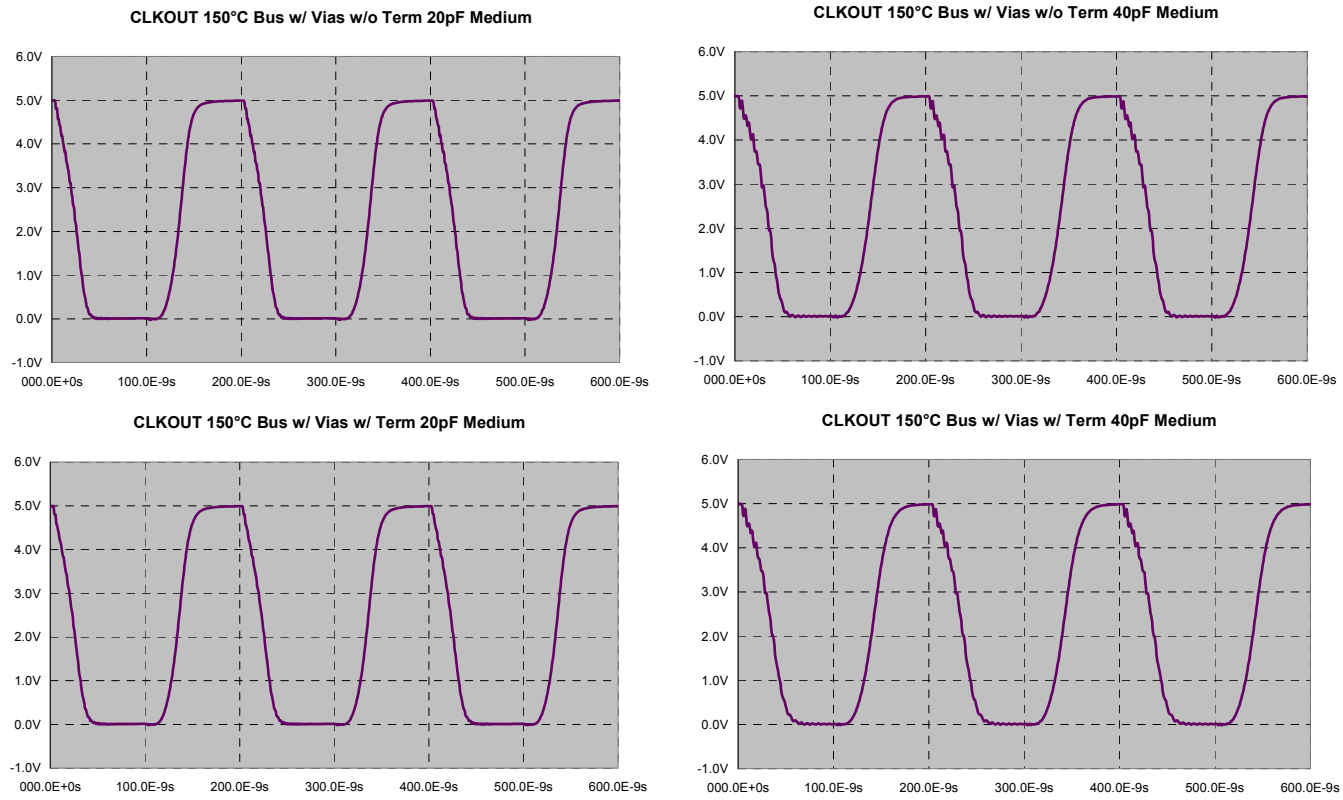


*Figure 74: Waveforms CLKOUT 5 MHz "Medium" / "Bus" at 150°C ambient temperature*

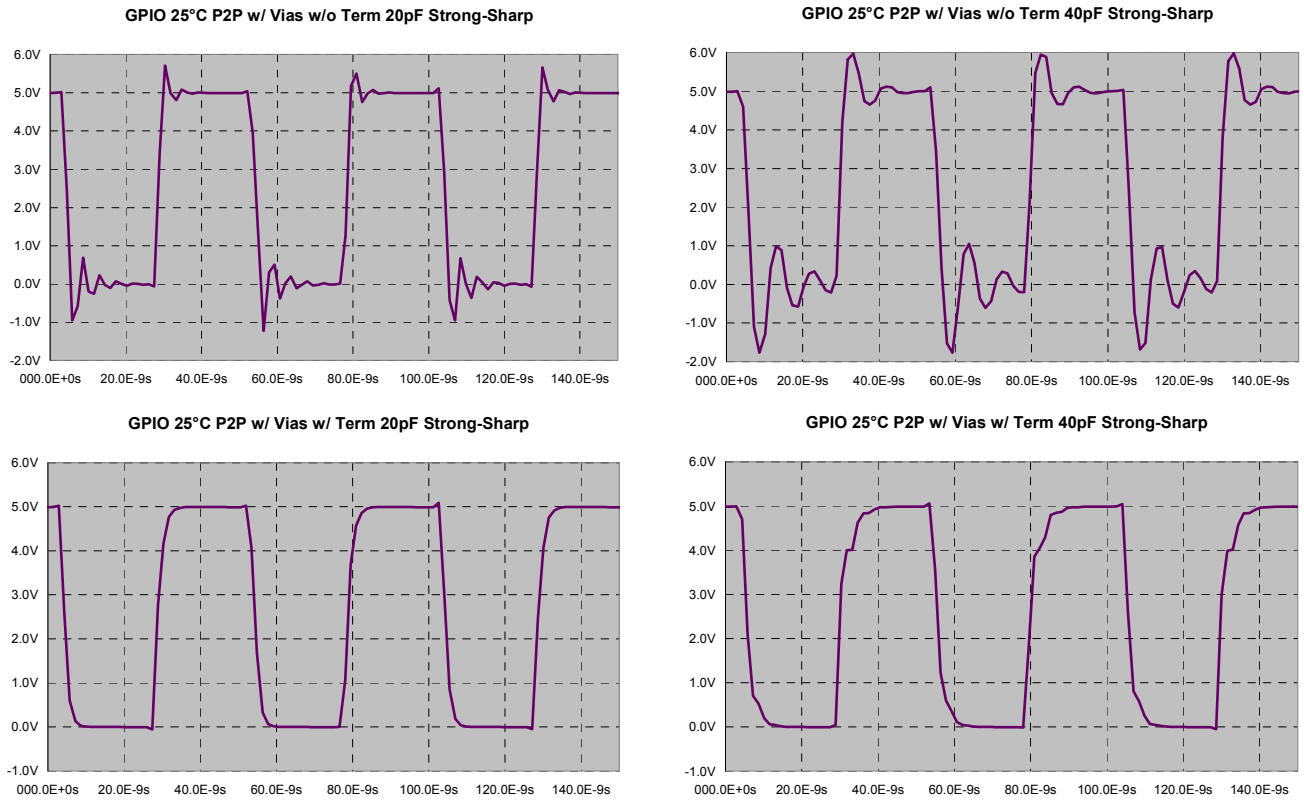


*Figure 75: Waveforms GPIO 20 MHz "Strong-Sharp" / "Point-to-Point" at 25°C ambient temperature*

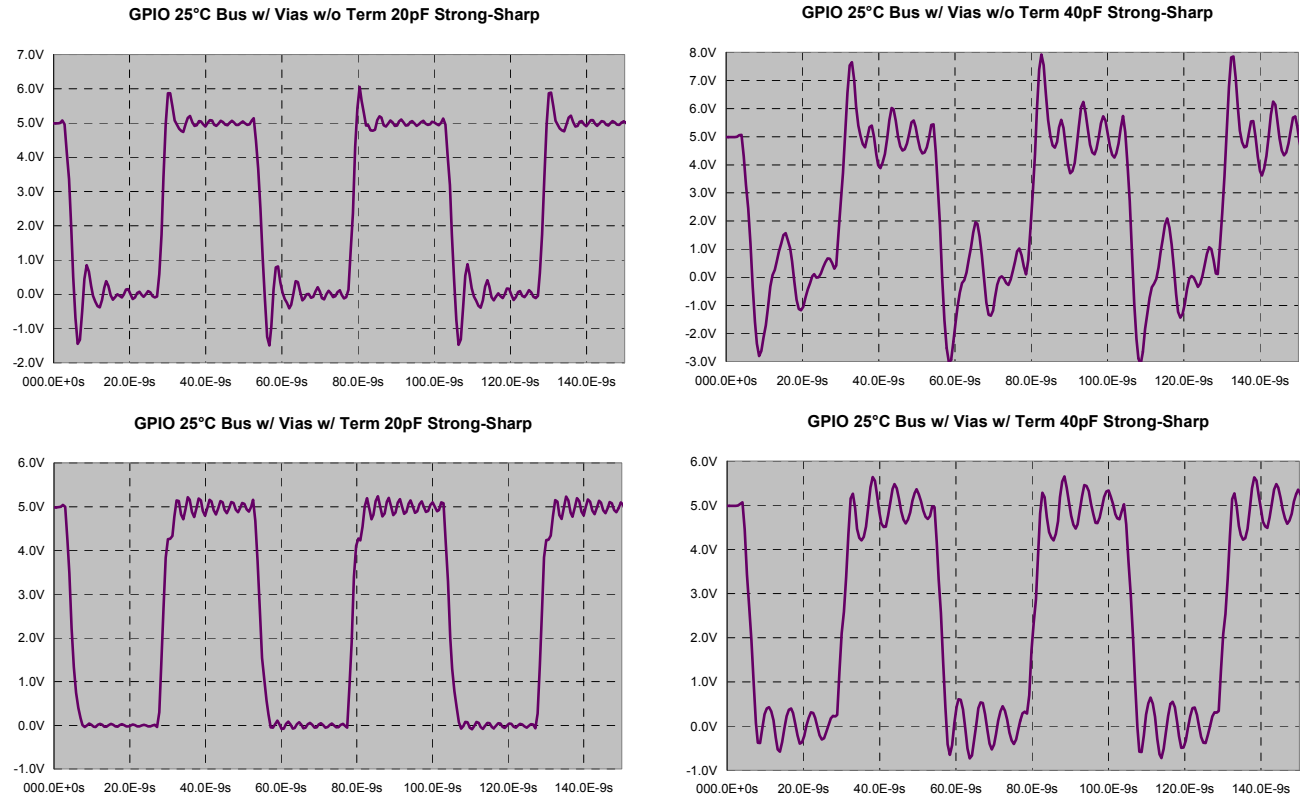


*Figure 76: Waveforms GPIO 20 MHz "Strong-Sharp" / "Bus" at 25°C ambient temperature*

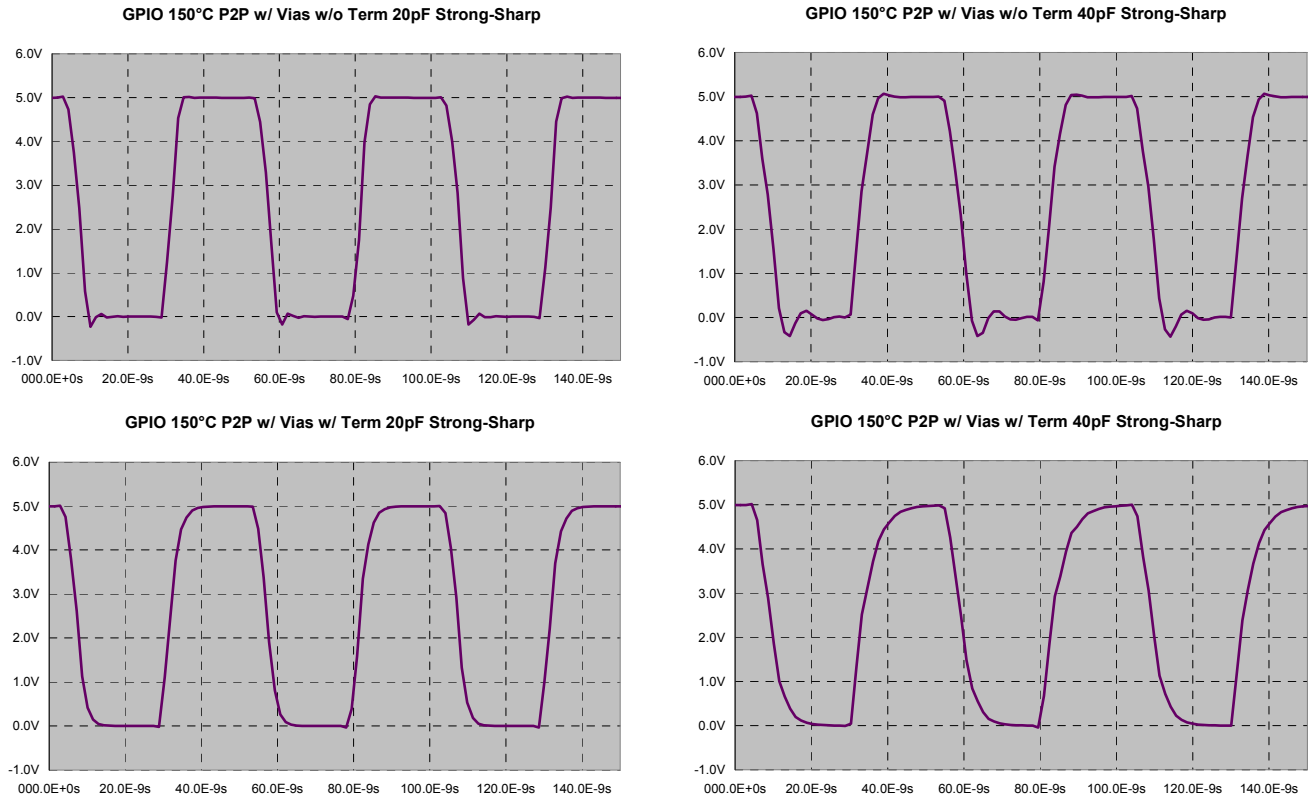


*Figure 77: Waveforms GPIO 20 MHz "Strong-Sharp" / "Point-to-Point" at 150°C ambient temperature*

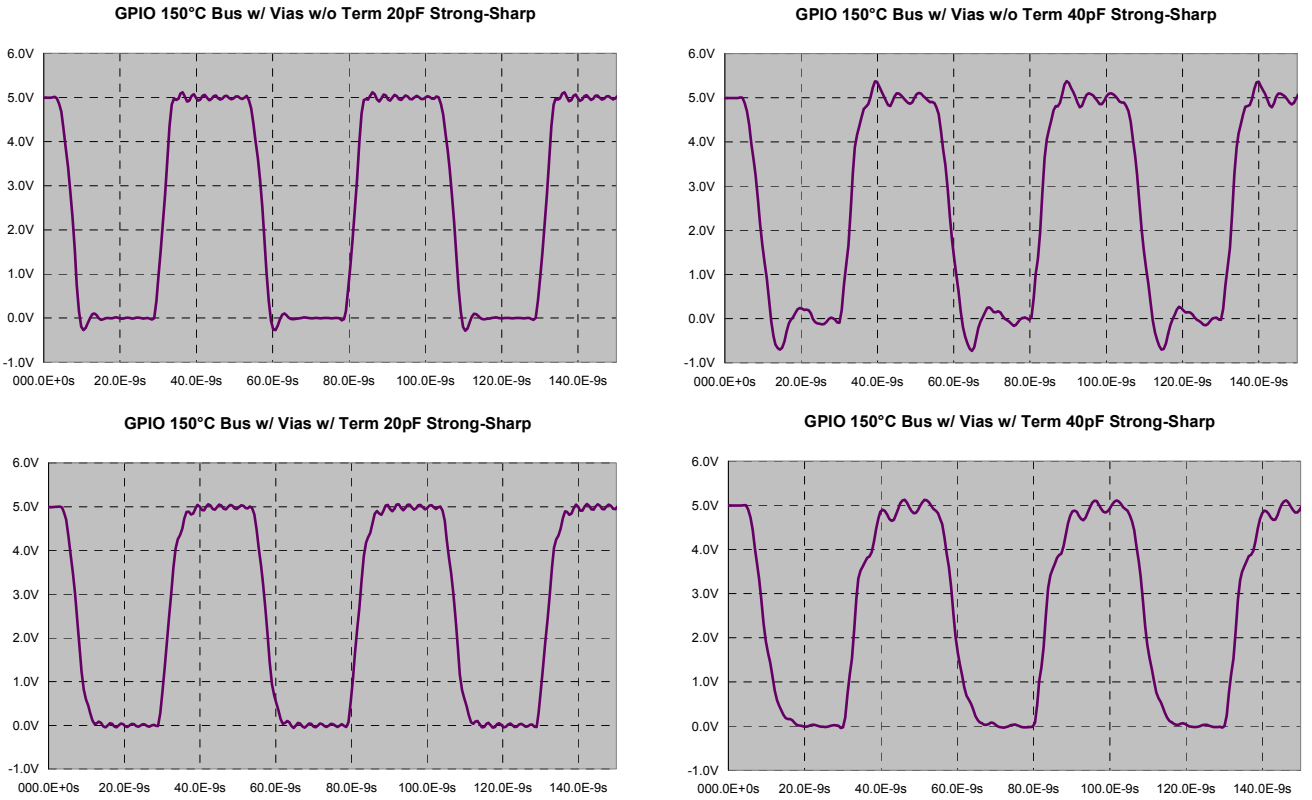


*Figure 78: Waveforms GPIO 20 MHz "Strong-Sharp" / "Bus" at 150°C ambient temperature*

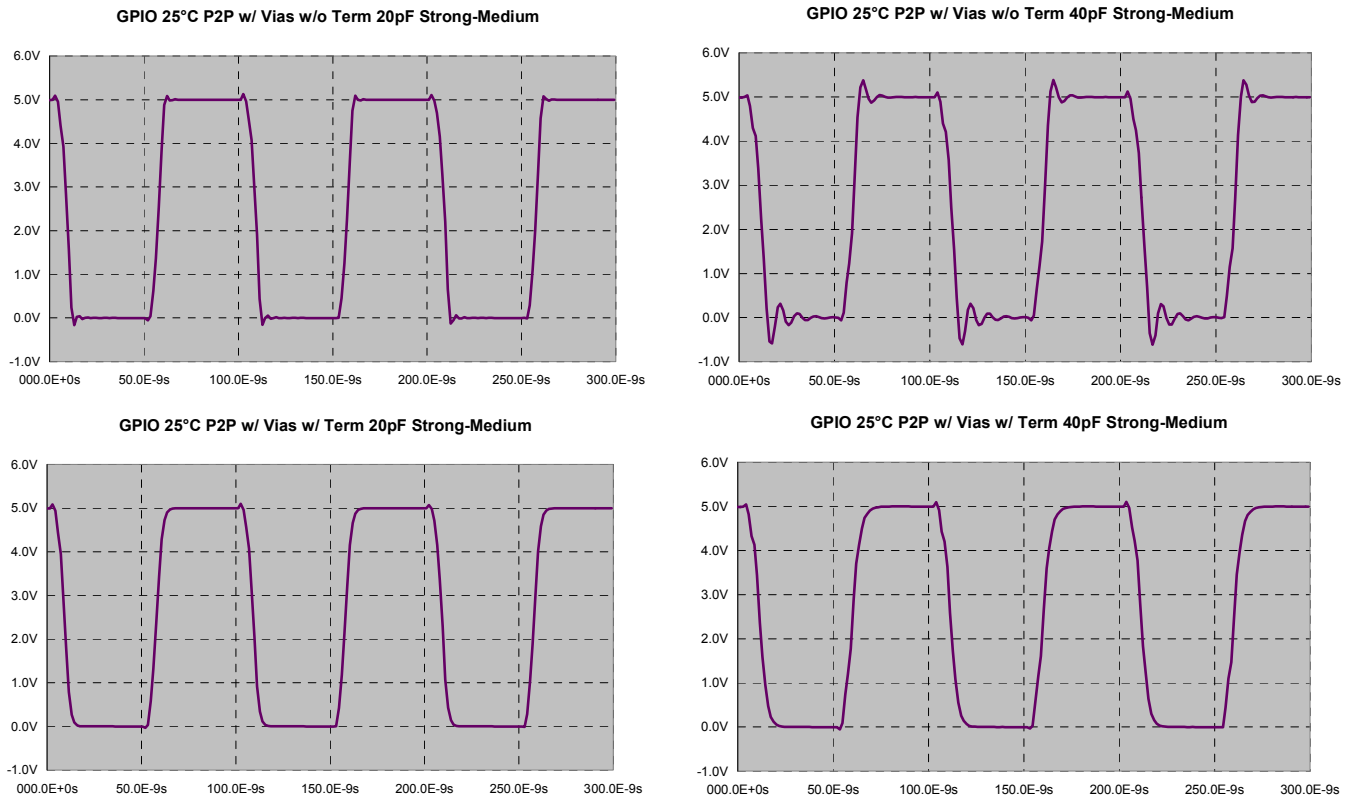


*Figure 79: Waveforms GPIO 10 MHz "Strong-Medium" / "Point-to-Point" at 25°C ambient temperature*

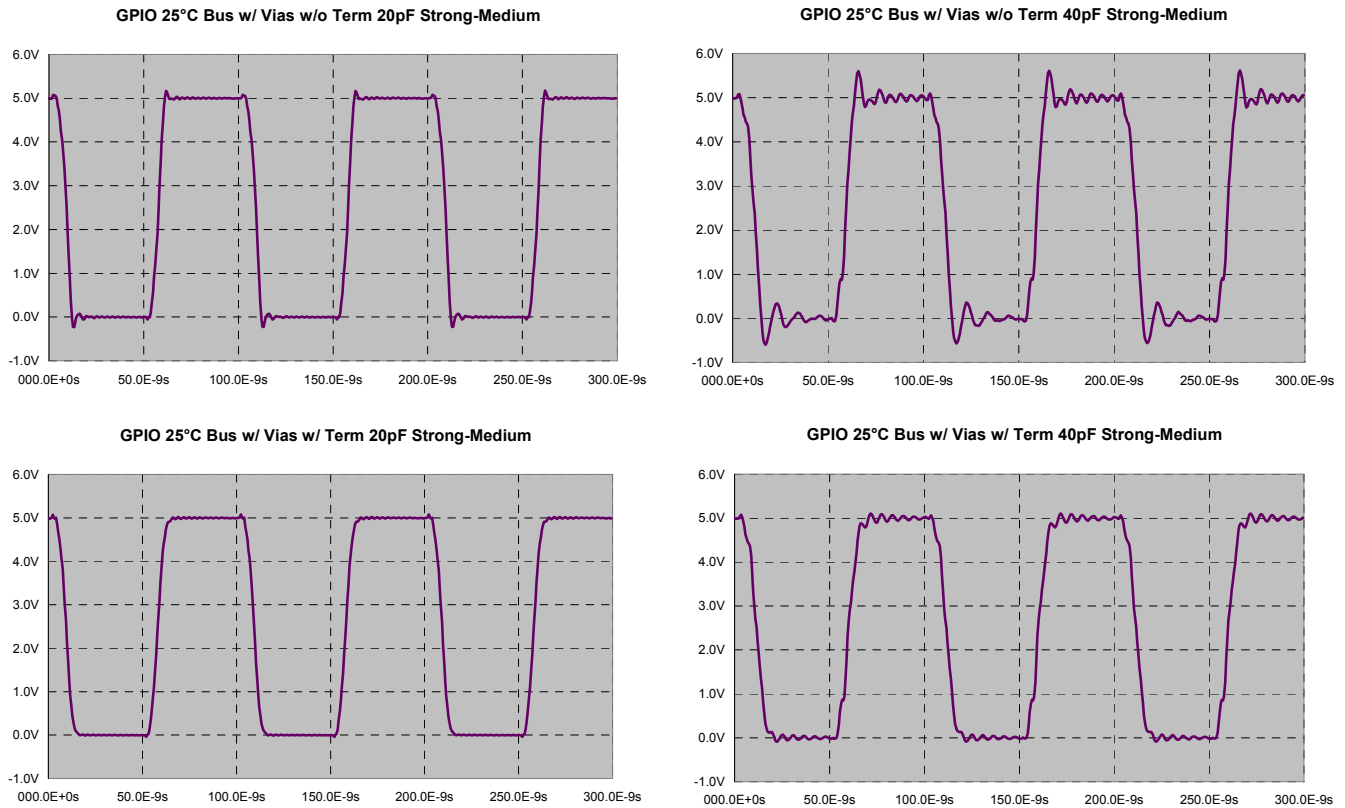


*Figure 80: Waveforms GPIO 10 MHz "Strong-Medium" / "Bus" at 25°C ambient temperature*

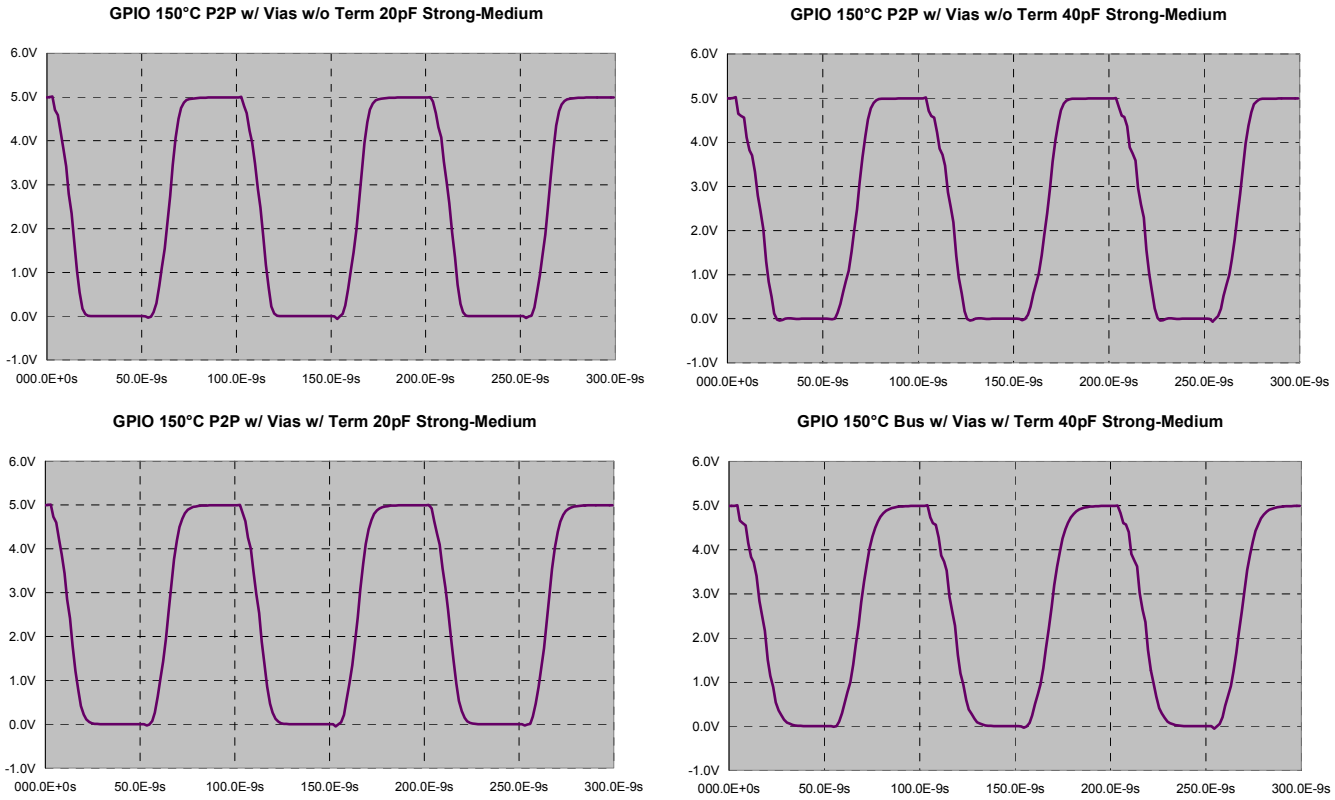


*Figure 81: Waveforms GPIO 10 MHz "Strong-Medium" / "Point-to-Point" at 150°C ambient temperature*

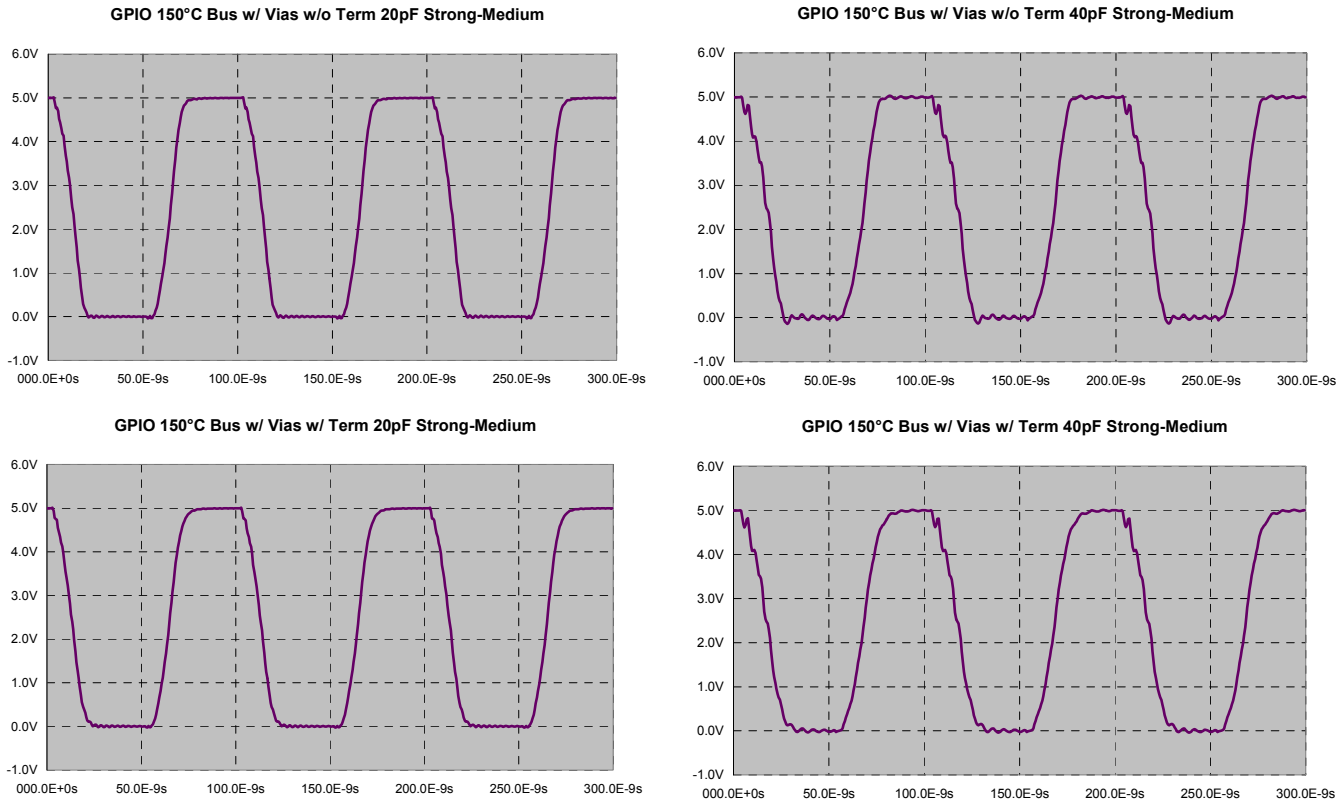


*Figure 82: Waveforms GPIO 10 MHz "Strong-Medium" / "Bus" at 150°C ambient temperature*

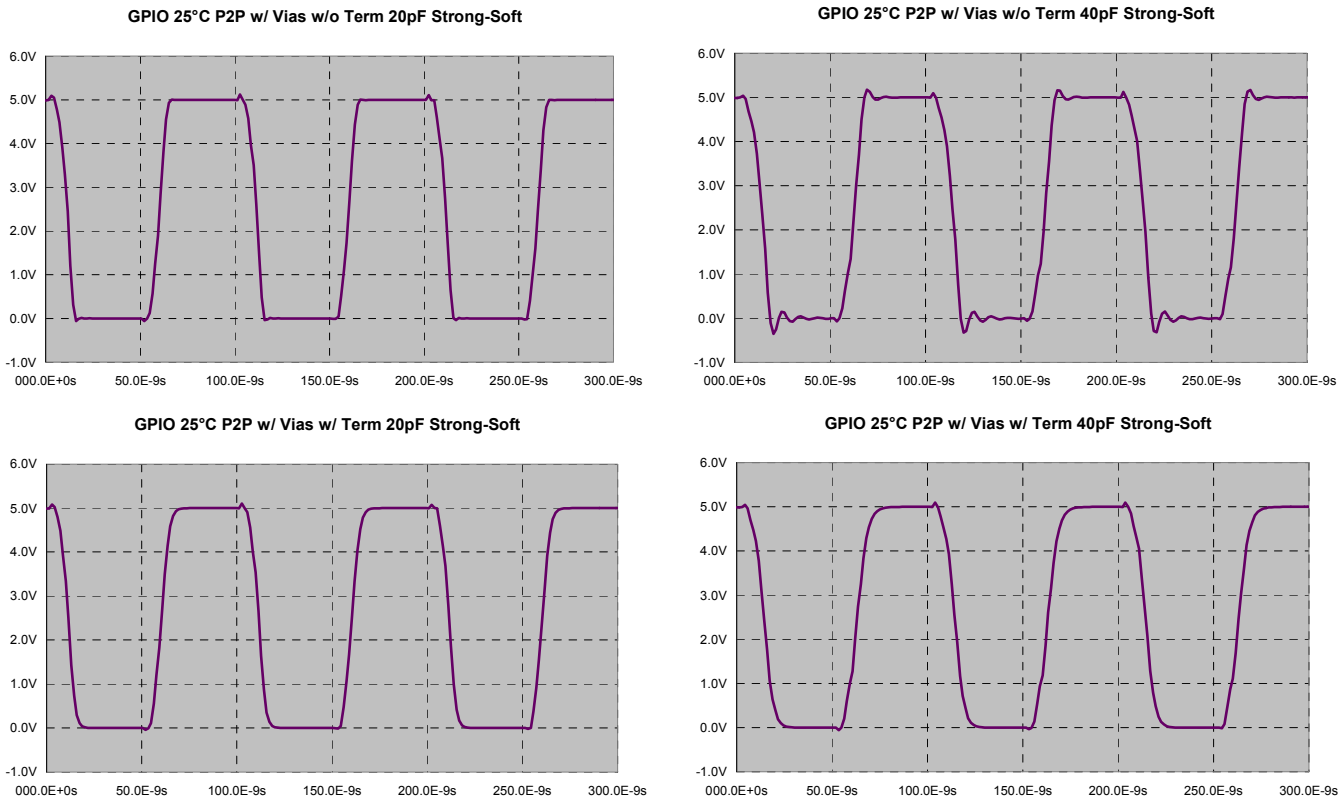


*Figure 83: Waveforms GPIO 10 MHz "Strong-Soft" / "Point-to-Point" at 25°C ambient temperature*

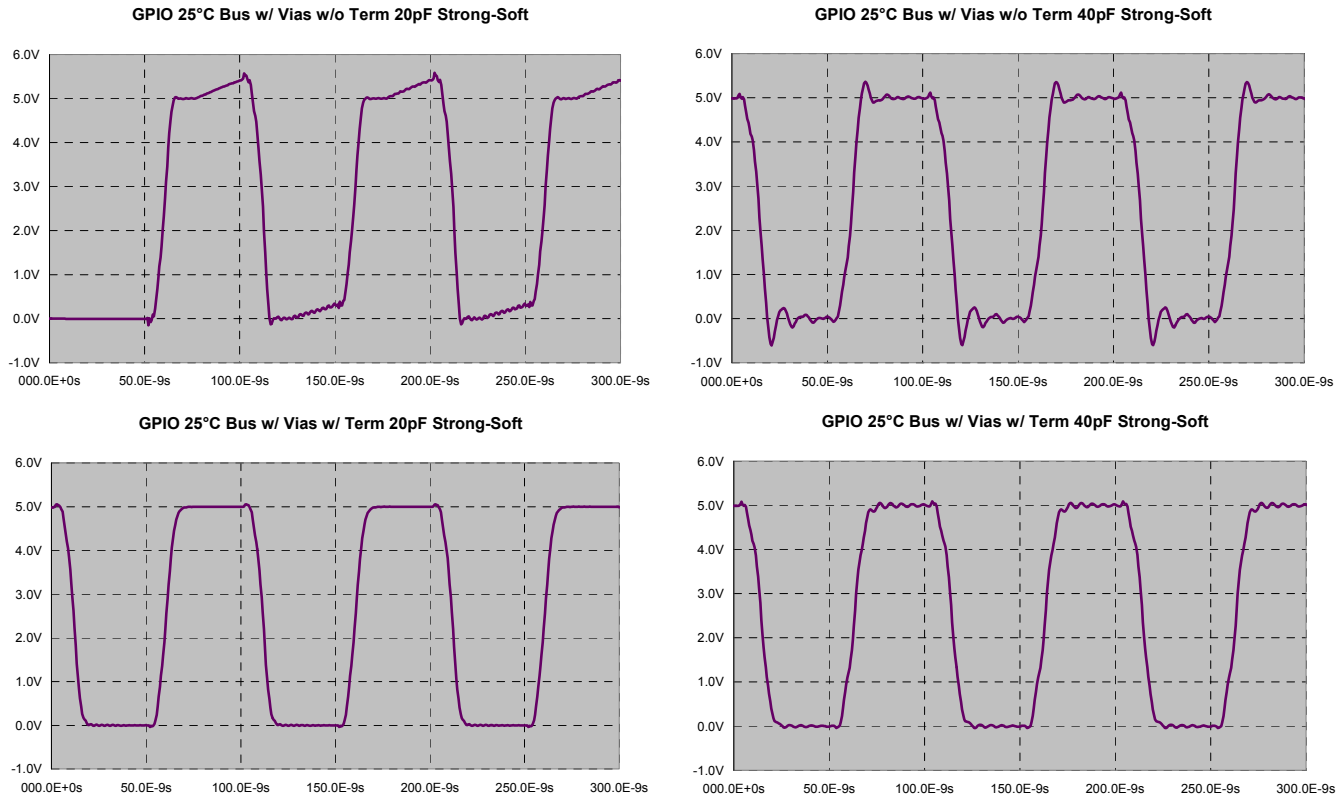


*Figure 84: Waveforms GPIO 10 MHz "Strong-Soft" / "Bus" at 25°C ambient temperature*

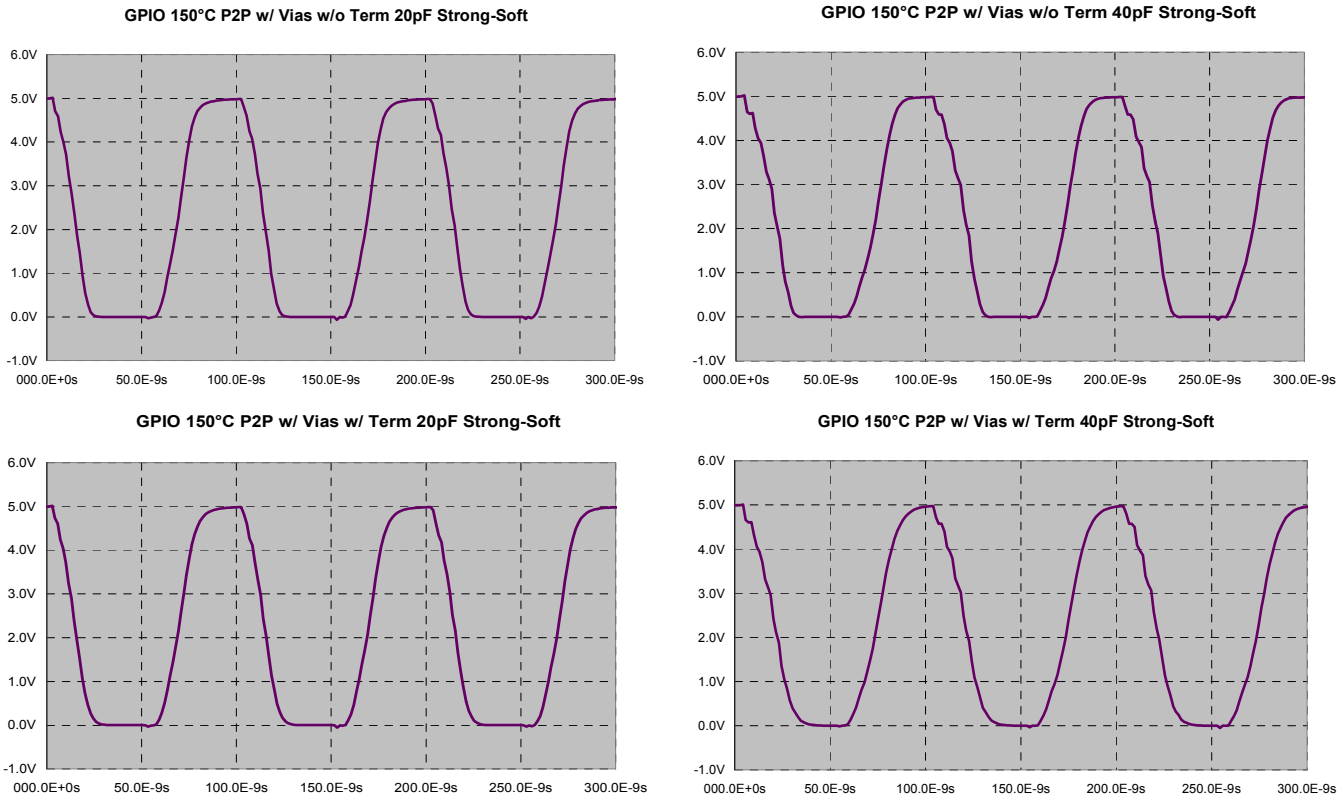


*Figure 85: Waveforms GPIO 10 MHz "Strong-Soft" / "Point-to-Point" at 150°C ambient temperature*

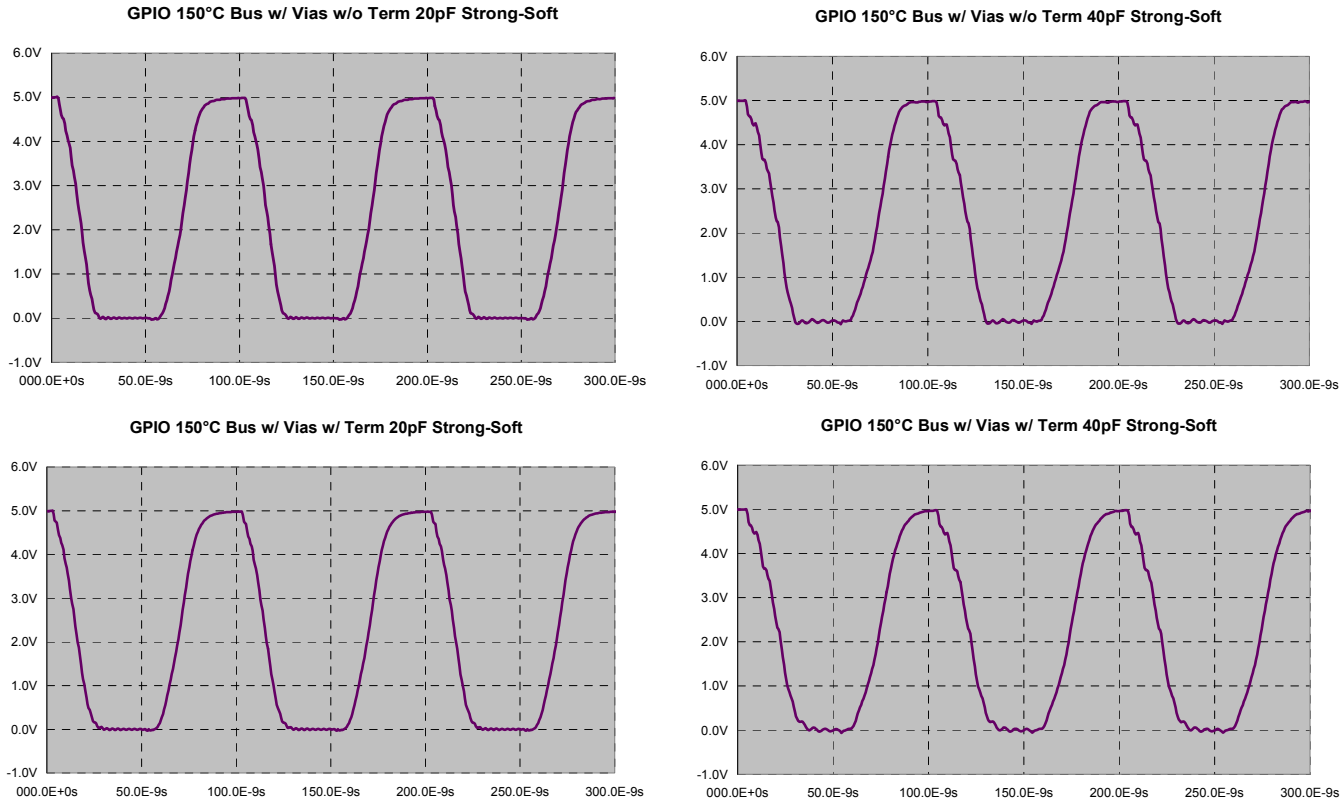


*Figure 86: Waveforms GPIO 10 MHz "Strong- Soft" / "Bus" at 150°C ambient temperature*

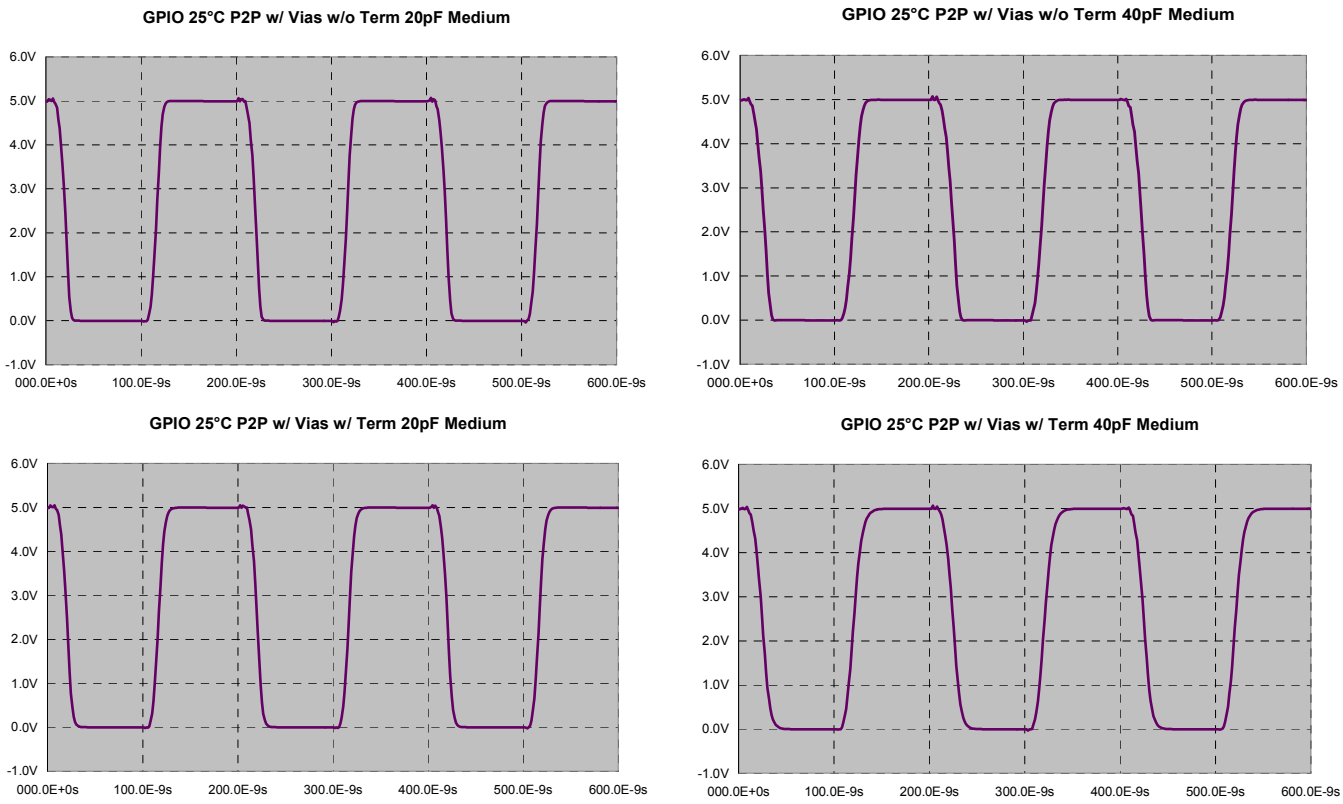


*Figure 87: Waveforms GPIO 5 MHz "Medium" / "Point-to-Point" at 25°C ambient temperature*

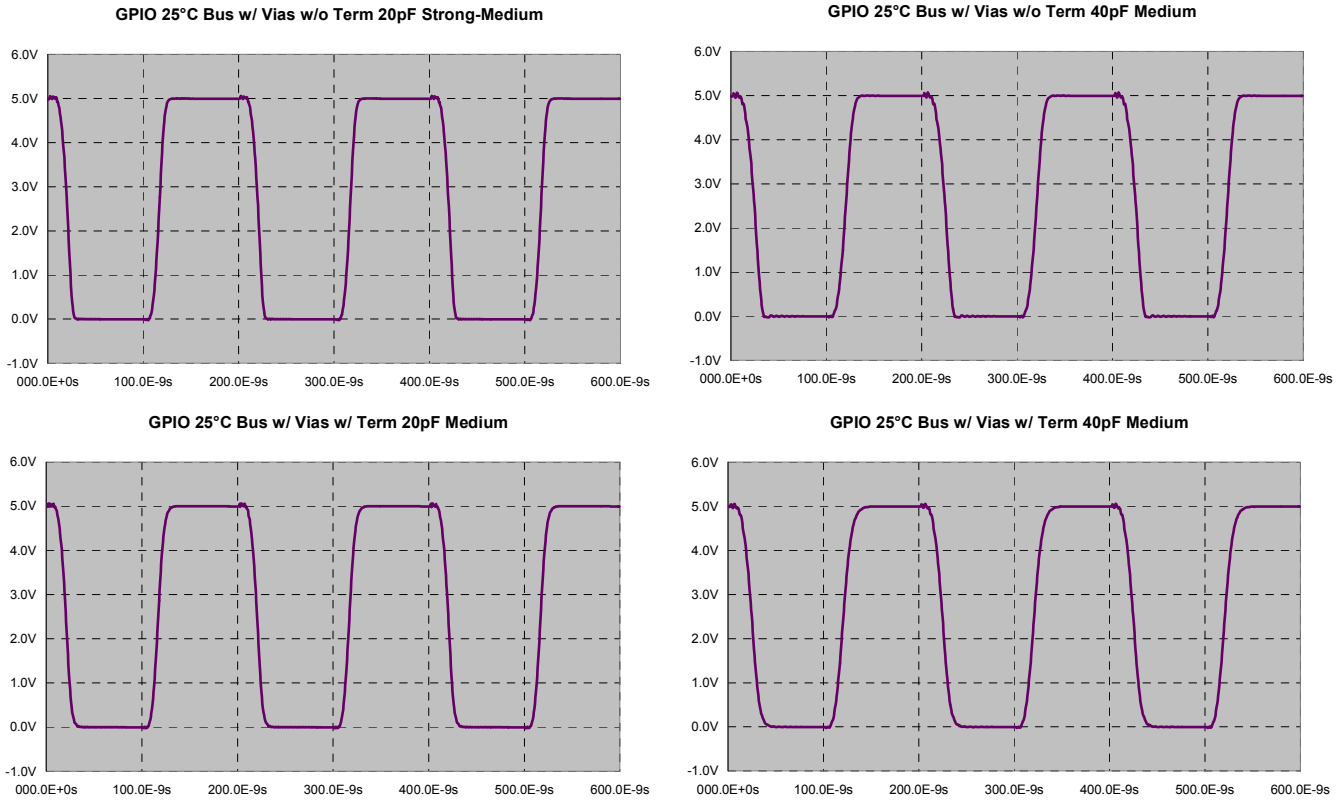


*Figure 88: Waveforms GPIO 5 MHz "Medium" / "Bus" at 25°C ambient temperature*

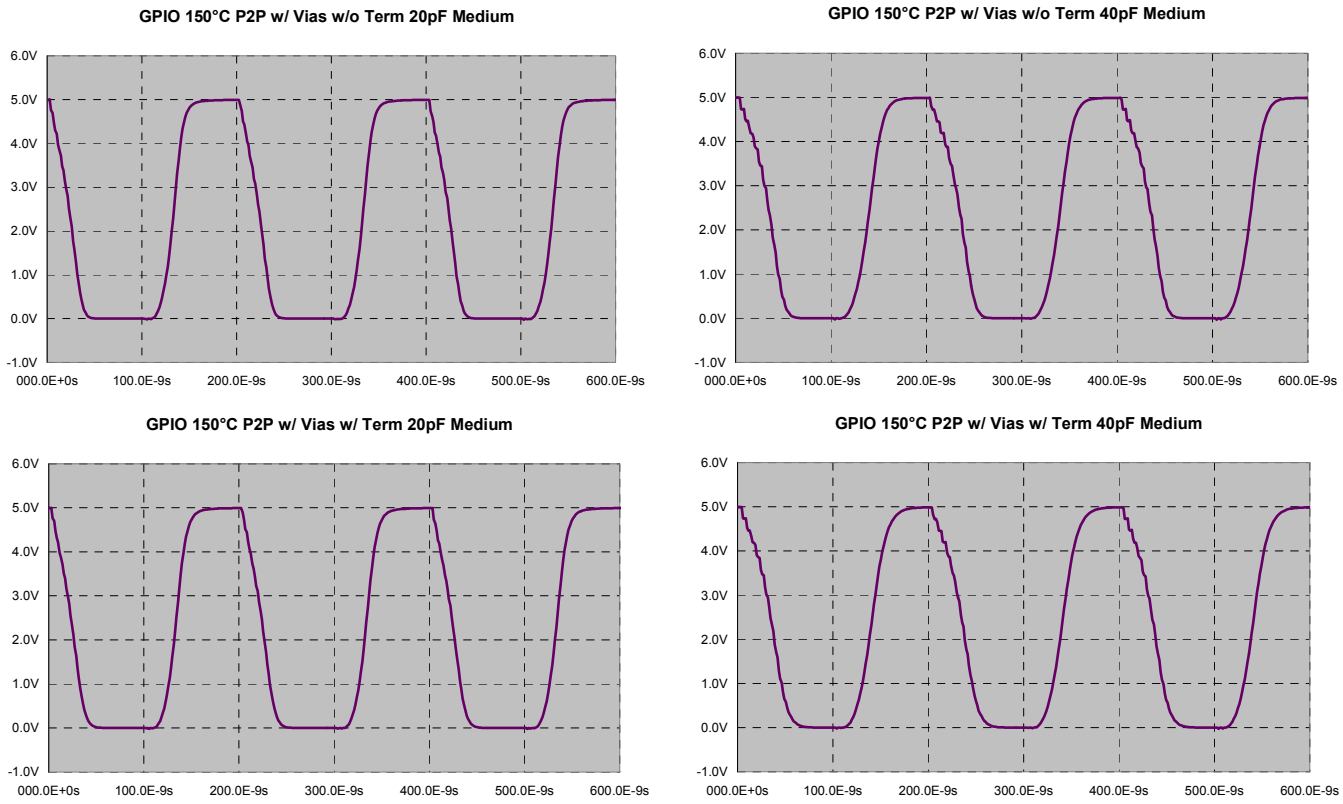


*Figure 89: Waveforms GPIO 5 MHz "Medium" / "Point-to-Point" at 150°C ambient temperature*

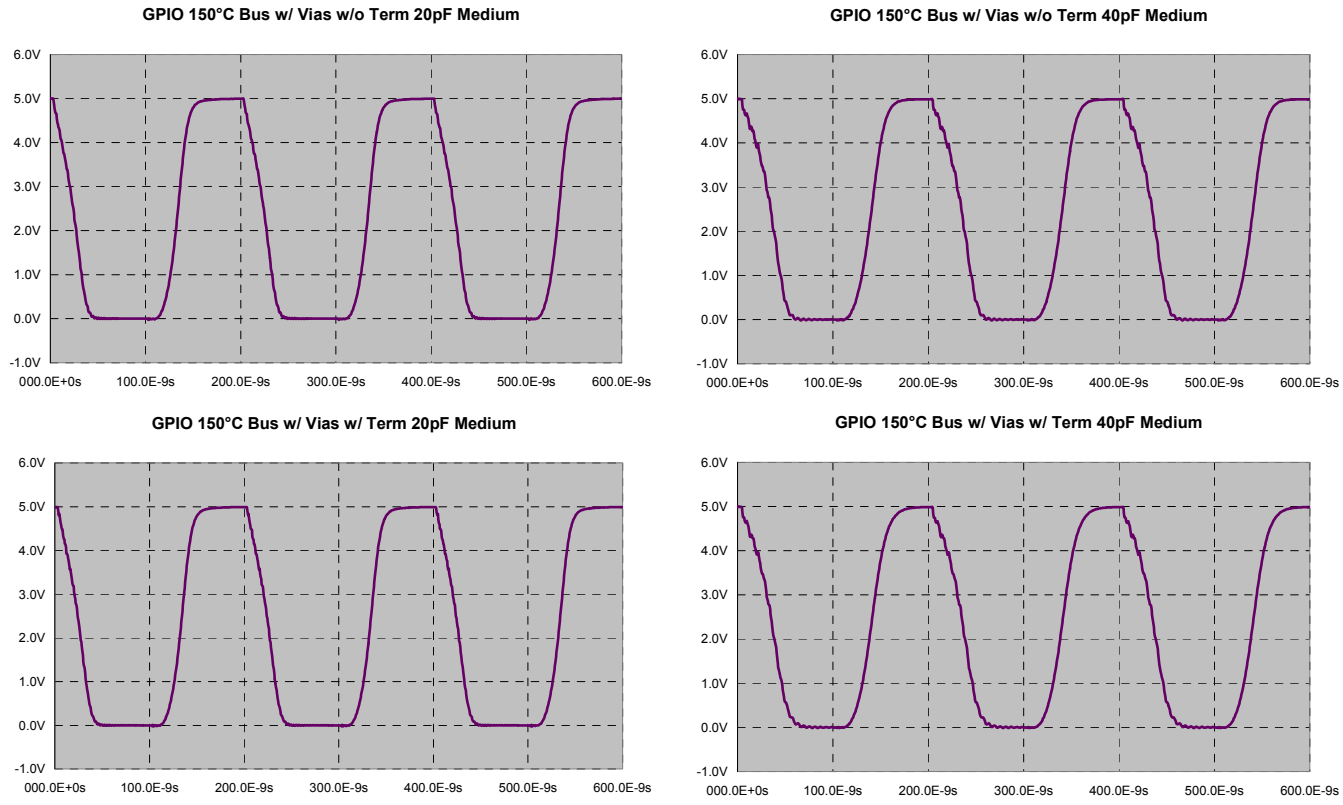


*Figure 90: Waveforms GPIO 5 MHz "Medium" / "Bus" at 150°C ambient temperature*

# 5 Measured Electromagnetic Emission

In addition to signal integrity, the scaling of pad drivers helps to reduce electromagnetic emission (EME) caused by switching output pins. This is because slower signal edges produce less high frequency contents in the emission spectra.

The following rule should be obeyed when selecting pad driver strength:

Use the weakest/slowest driver setting which provides the required signal timing at worst-case operating conditions.

Worst-case operating conditions are:

- maximum ambient temperature (e.g. +125°C)
- minimum pad supply voltage (e.g. 4.50V)
- realistic capacitive output load (consider trace length, trace structure, connected receiver input loads)

To illustrate the benefits of driver scaling for low EME, some sample measurement results are provided.

The measurements have been performed under two operating conditions:

Operating condition 1:
CLKOUT toggling at 40MHz with capacitive loads of 0pF, 10pF, 22pF, 33pF, 47pF.
All GPIOs inactive.
Core running in idle loop.
Conducted emission measured at pad supply (VDDP) and core supply (VDDC) according to chapter 5.1.1.
Radiated emission measured in mini-TEM cell according to chapter 5.1.2.

Operating condition 2:
GPIOs toggling at ca. 700kHz with capacitive loads of 0pF, 22pF, 47pF.
Toggling pins are: Port2[15:0].
CLKOUT inactive.
Conducted emission measured at pad supply (VDDP) and core supply (VDDC) according to chapter 5.1.1.
Radiated emission measured in mini-TEM cell according to chapter 5.1.2.

Please note that all emission peaks visible between 900 MHz and 1000 MHz result from cellular phone activity and should be ignored when assessing the IC-related emission.

## 5.1 Description of test equipment

### 5.1.1 Conducted emission test configuration

Conducted emission is measured using the standardized 150Ω network, see Fig. 91. This network is used for both port and power supply emission measurements. For reference purpose, only the emission measured at the supply domains VDDP (5.0V pad supply) and VDDC (2.5V core supply) are documented. Emission reduction can be observed in a similar way on passive (i.e. non-switching) pad pins.

150Ω networks are provided for conducted emission measurements according IEC 61967 part 4 and BISS emission test specification.

For the measurements the probing points shown in Fig. 91 connected to VDD1 (is VDDC) and VDD2 (is VDDP) are used. No testing was performed at passive I/Os.

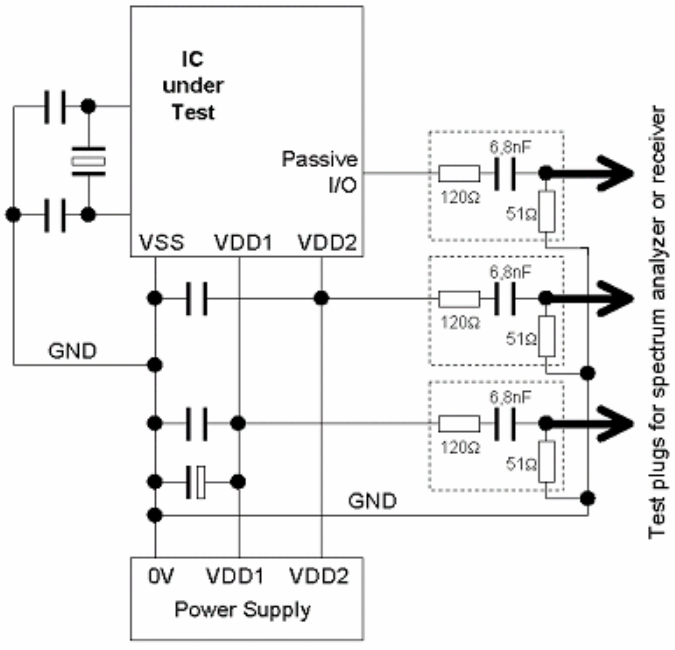


*Figure 91: Conducted emission probing points*

### 5.1.2 Radiated emission test configuration

Radiated emission is measured using the standard Mini TEM Cell according IEC 61967 part 2 and BISS emission test specification. The frequency range is from 150kHz to 1000MHz.

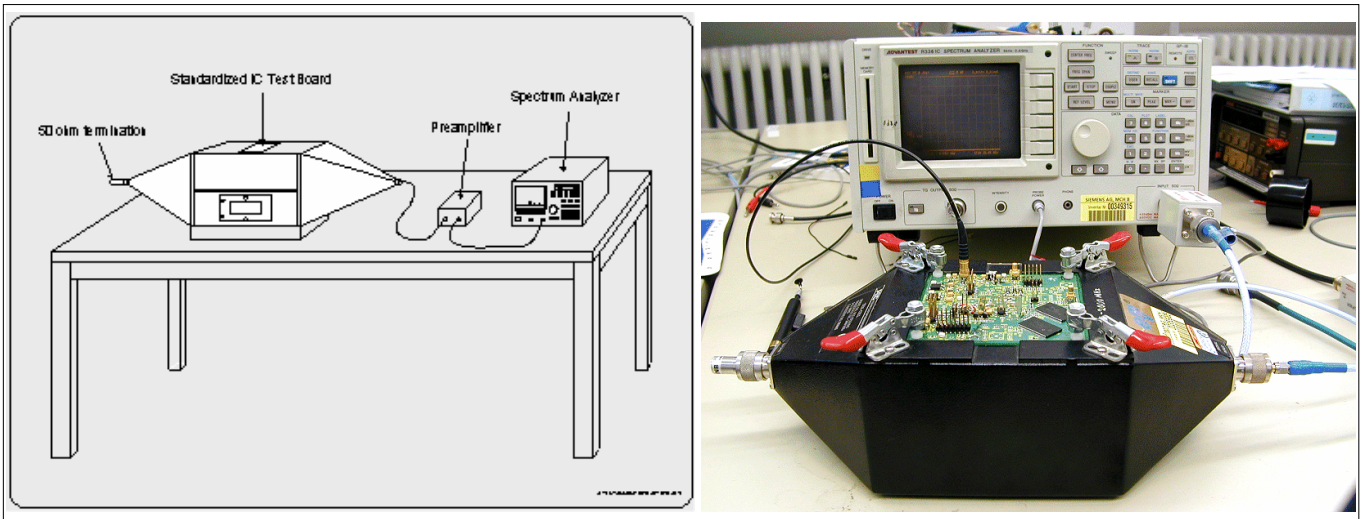


*Figure 92: Radiated emission test setup*

### 5.1.3 Instruments and software for emission data recognition

| | |
|---|---|
| Spectrum analyzer: | Advantest R3361C |
| Detector type: | Peak detector |
| Measurement time: | For all measurements, the emission measurement time (10ms) at one frequency is longer than the test software loop duration. |
| Pre-Amplifier: | Advantest R14601A |
| Data generation software: | Rohde&Schwarz EMIPAK 9950 |
| Environment: | temperature 23°C ±5°C |
| Supply: | nominal voltage ±5% |

For all measurements the noise floor is at least 6dB below the limit.

| Frequency range | | | | Spectrum Analyzer | |
|---|---|---|---|---|---|
| | | | | RBW | Sweep time* |
| 150 Ω | TEM | 150 kHz | to 30 MHz | 10kHz | $t_s = \frac{NP \cdot LT \cdot FR}{RBW}$ |
| | | 30 MHz | to 200 MHz | 100kHz | |
| | | 200 MHz | to 1000 MHz | | |

Table 4: Spectrum analyzer settings for EME measurements

*) NP=number of points; LT=loop time; FR=frequency range

## 5.2 Emission measurement results

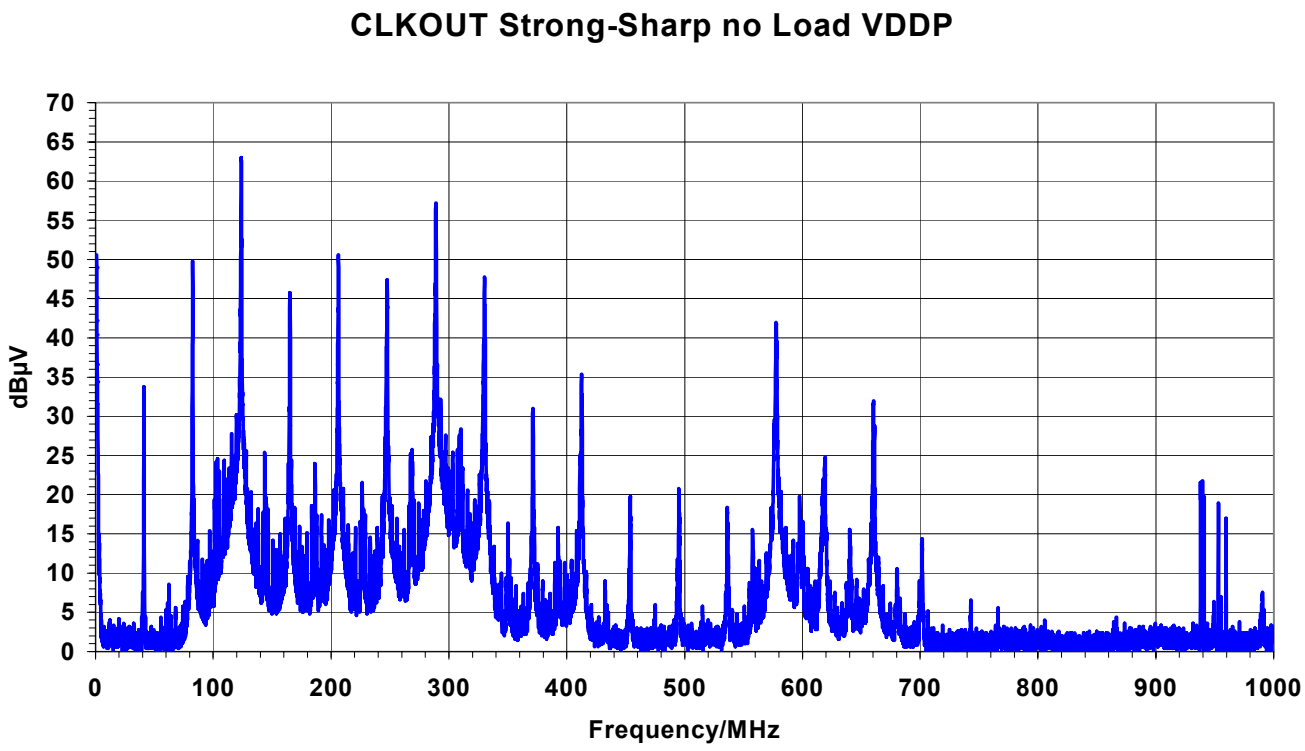


*Figure 93: CLKOUT „Strong-Sharp“ driver at 0pF load – conducted emission on VDDP*

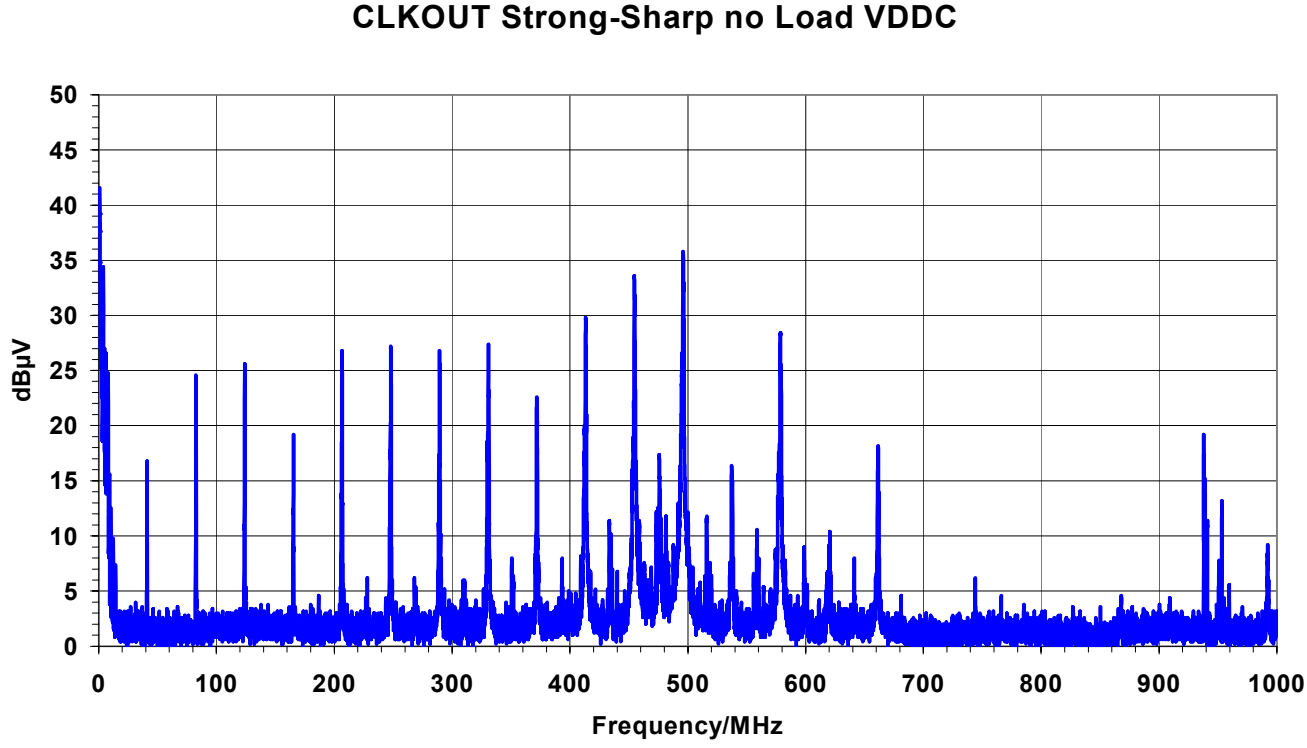


*Figure 94: CLKOUT „Strong-Sharp“ driver at 0pF load – conducted emission on VDDC*

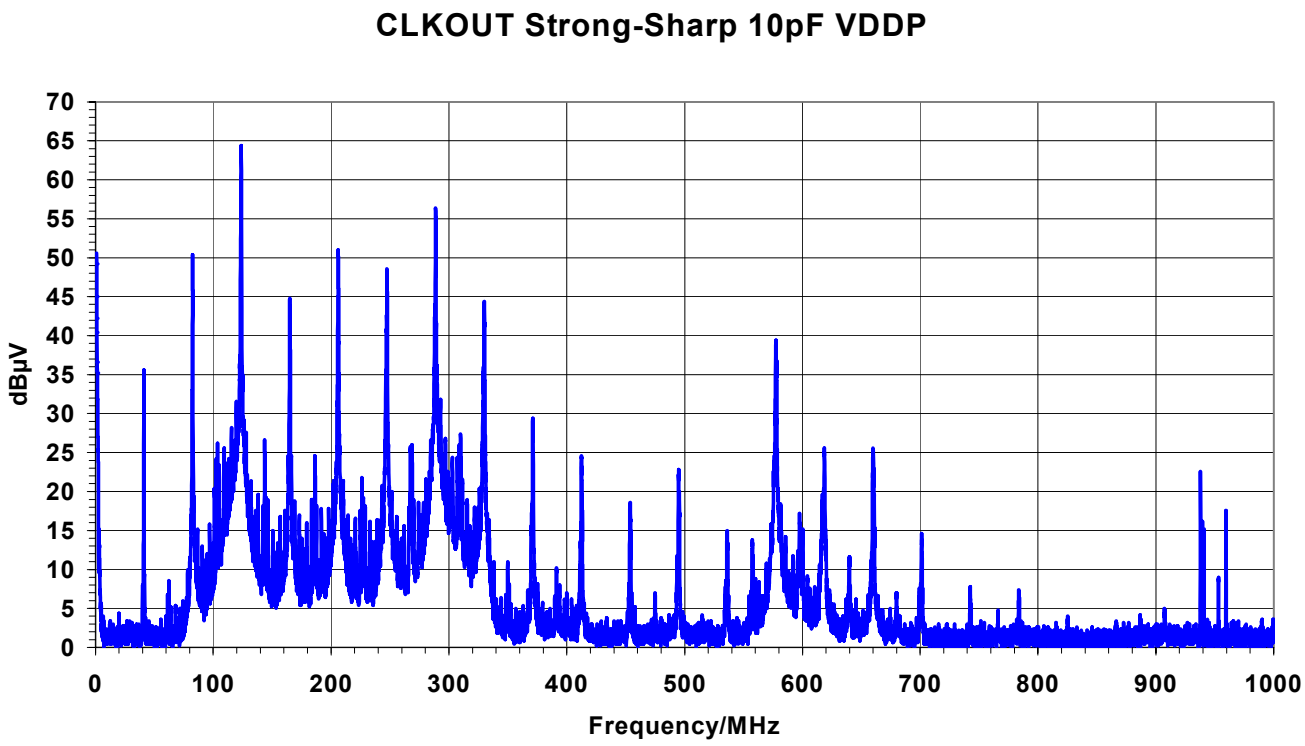


*Figure 95: CLKOUT „Strong-Sharp“ driver at 10pF load – conducted emission on VDDP*

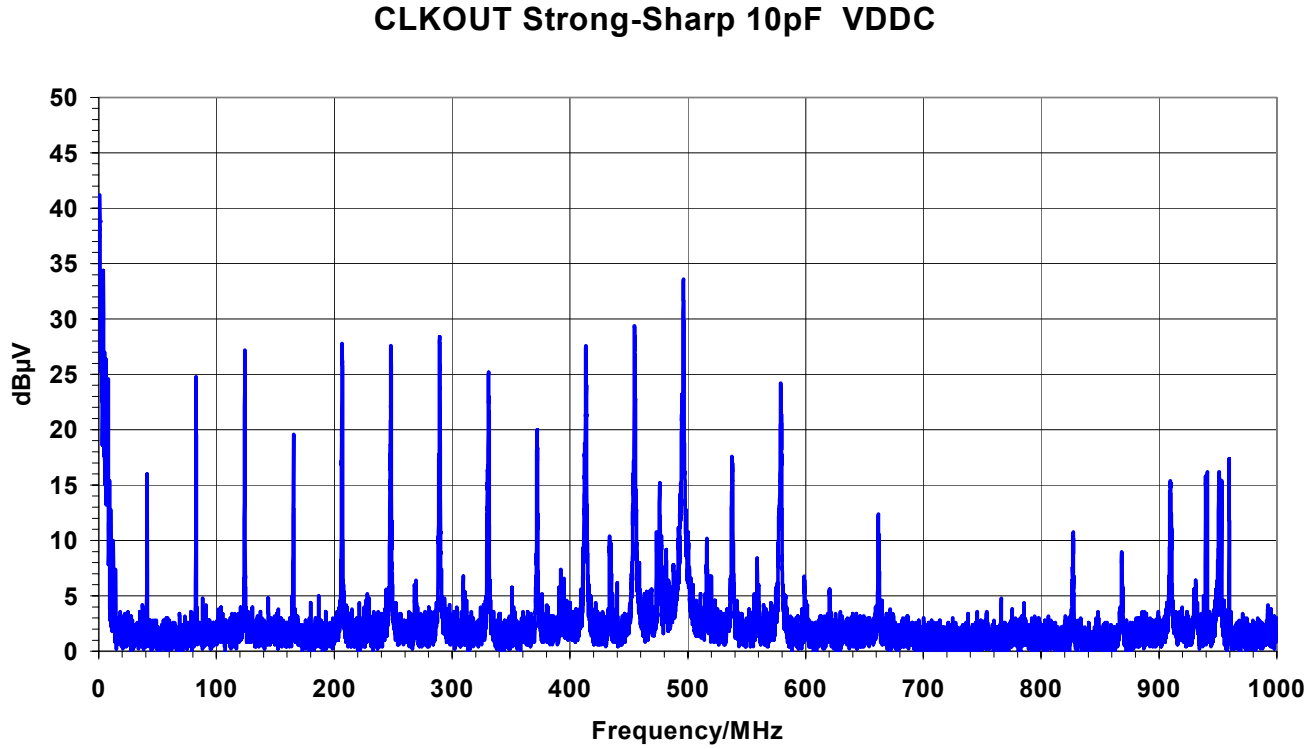


*Figure 96: CLKOUT „Strong-Sharp“ driver at 10pF load – conducted emission on VDDC*

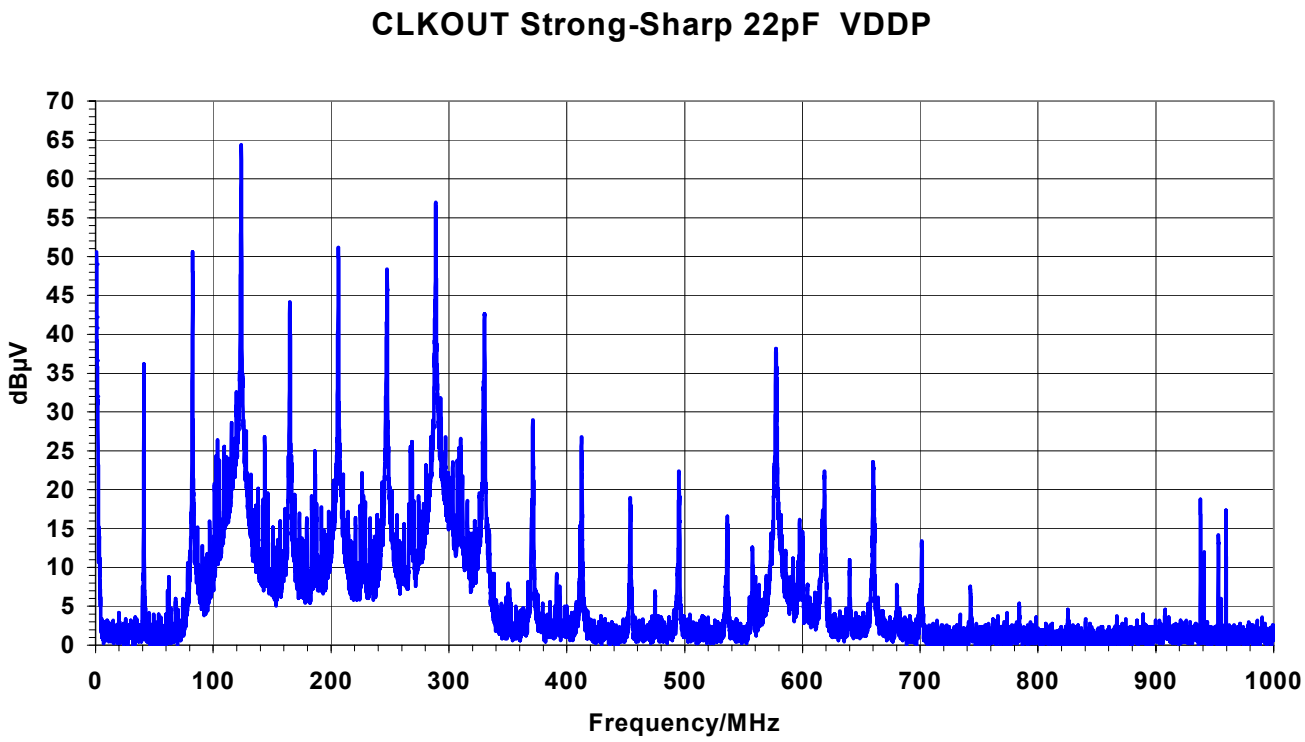


*Figure 97: CLKOUT „Strong-Sharp“ driver at 22pF load – conducted emission on VDDP*

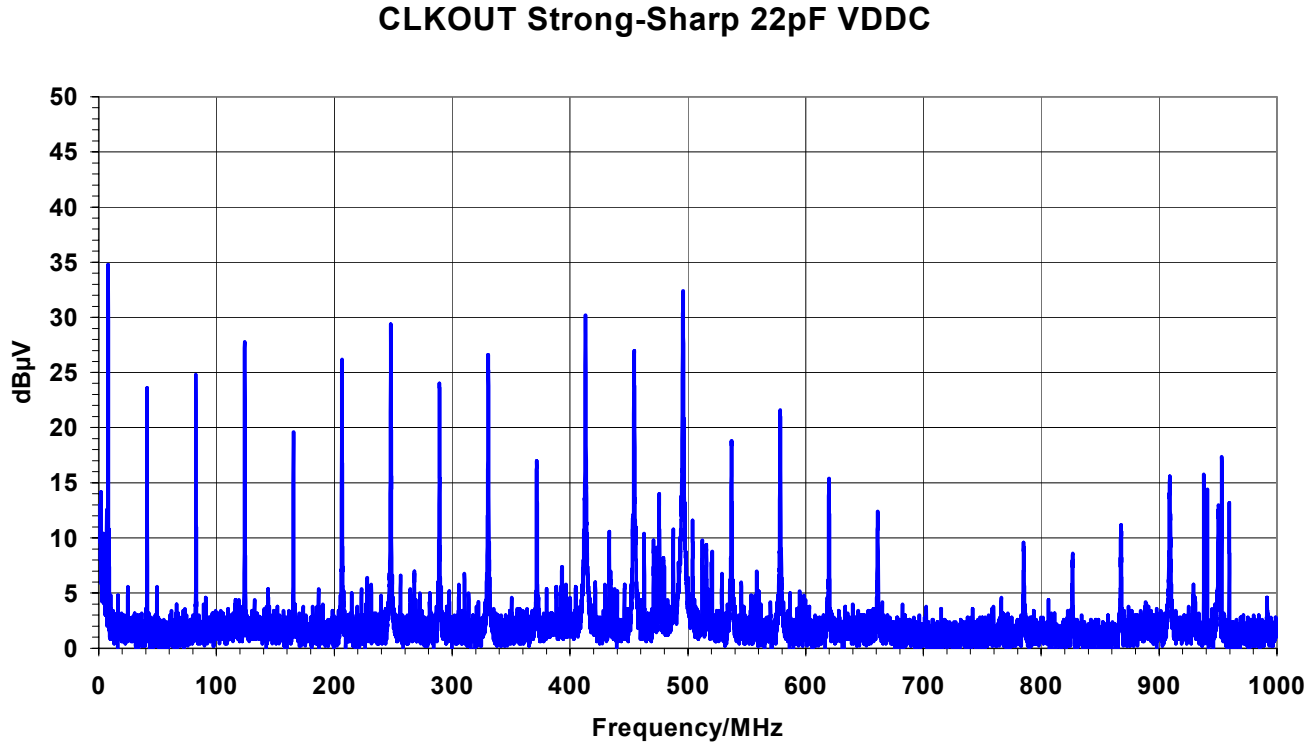


*Figure 98: CLKOUT „Strong-Sharp“ driver at 22pF load – conducted emission on VDDC*

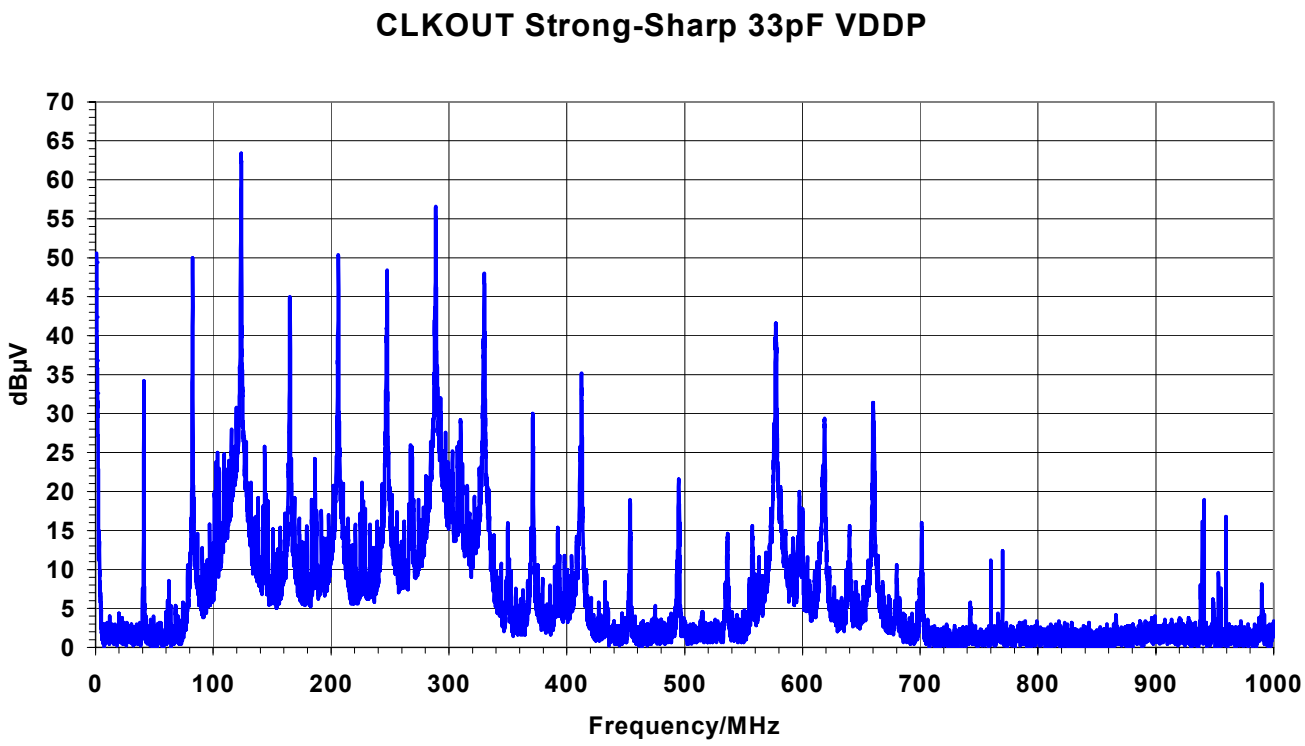


*Figure 99: CLKOUT „Strong-Sharp“ driver at 33pF load – conducted emission on VDDP*

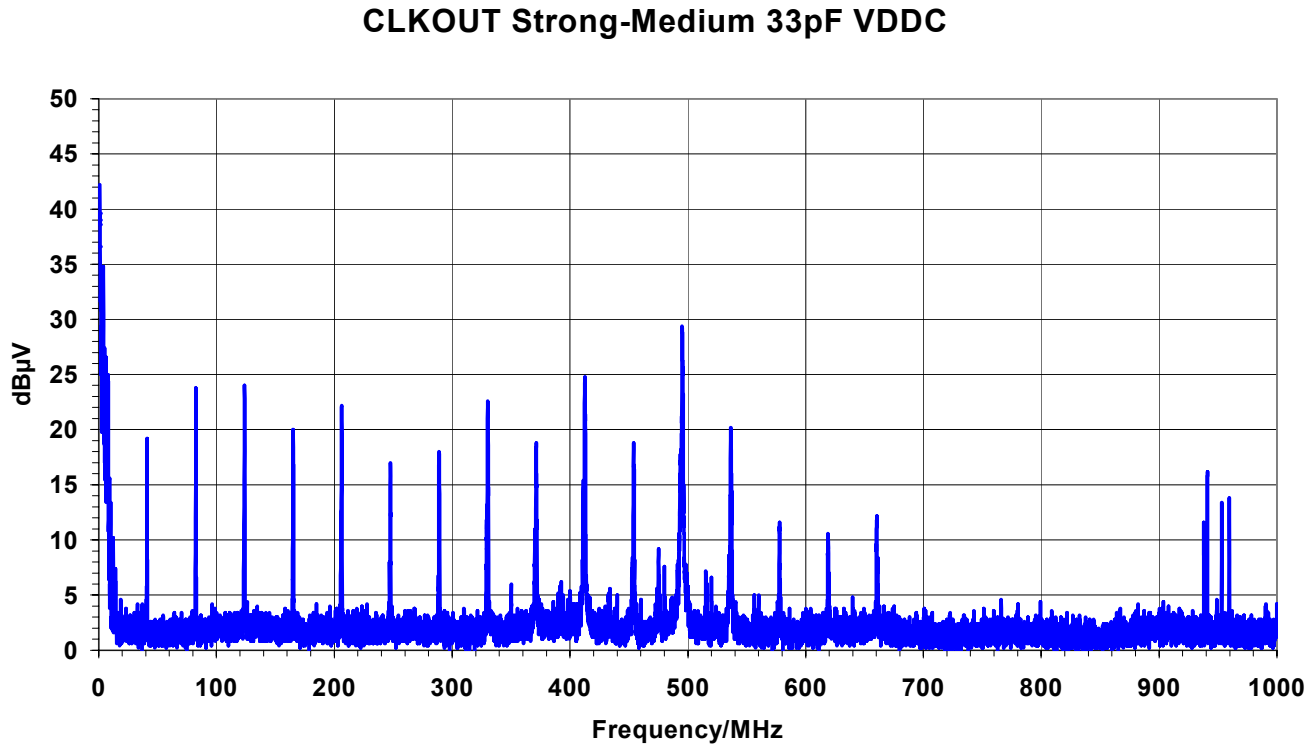


*Figure 100: CLKOUT „Strong-Sharp“ driver at 33pF load – conducted emission on VDDC*

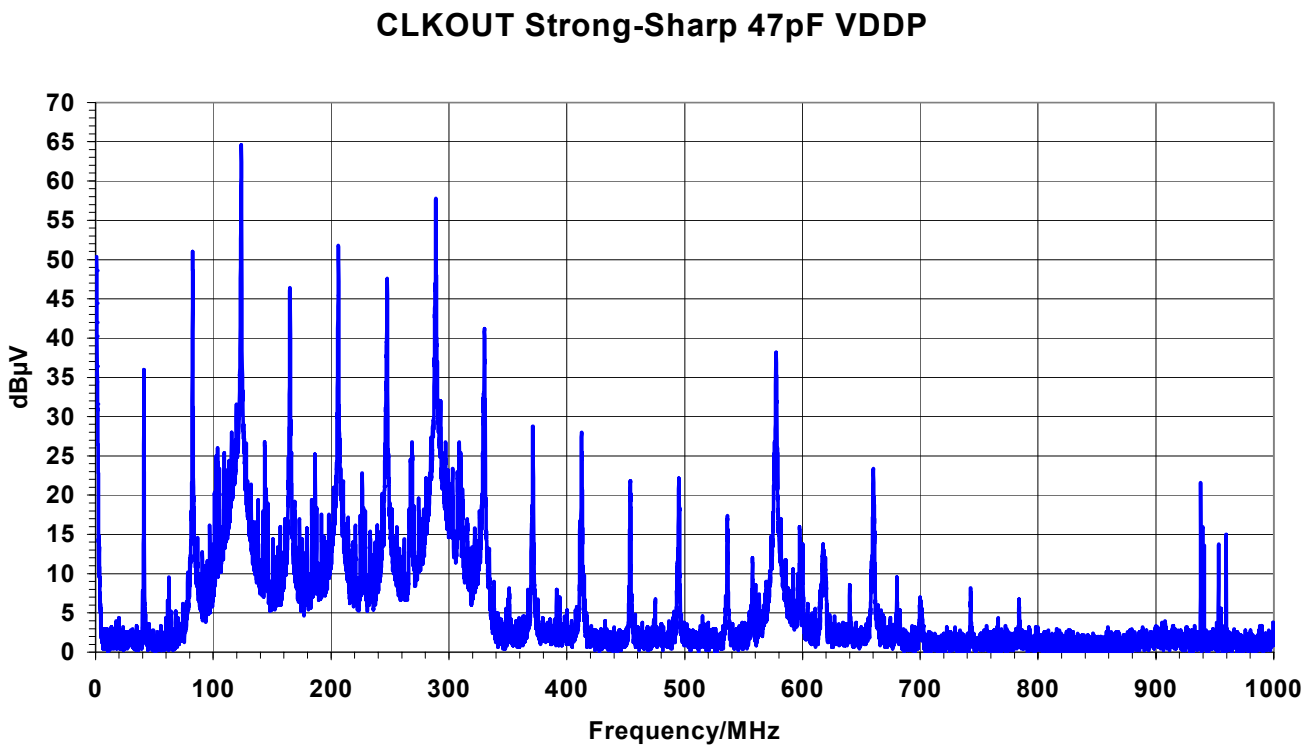


*Figure 101: CLKOUT „Strong-Sharp“ driver at 47pF load – conducted emission on VDDP*

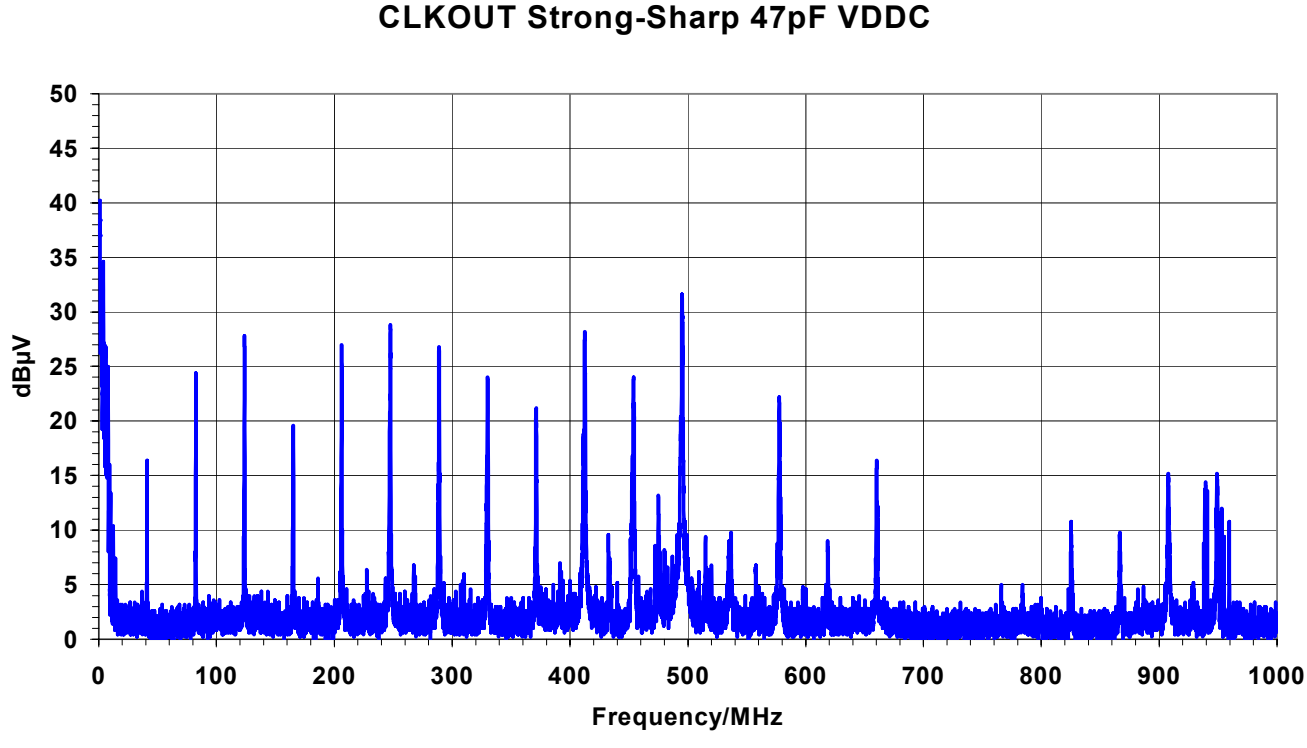


*Figure 102: CLKOUT „Strong-Sharp“ driver at 47pF load – conducted emission on VDDC*

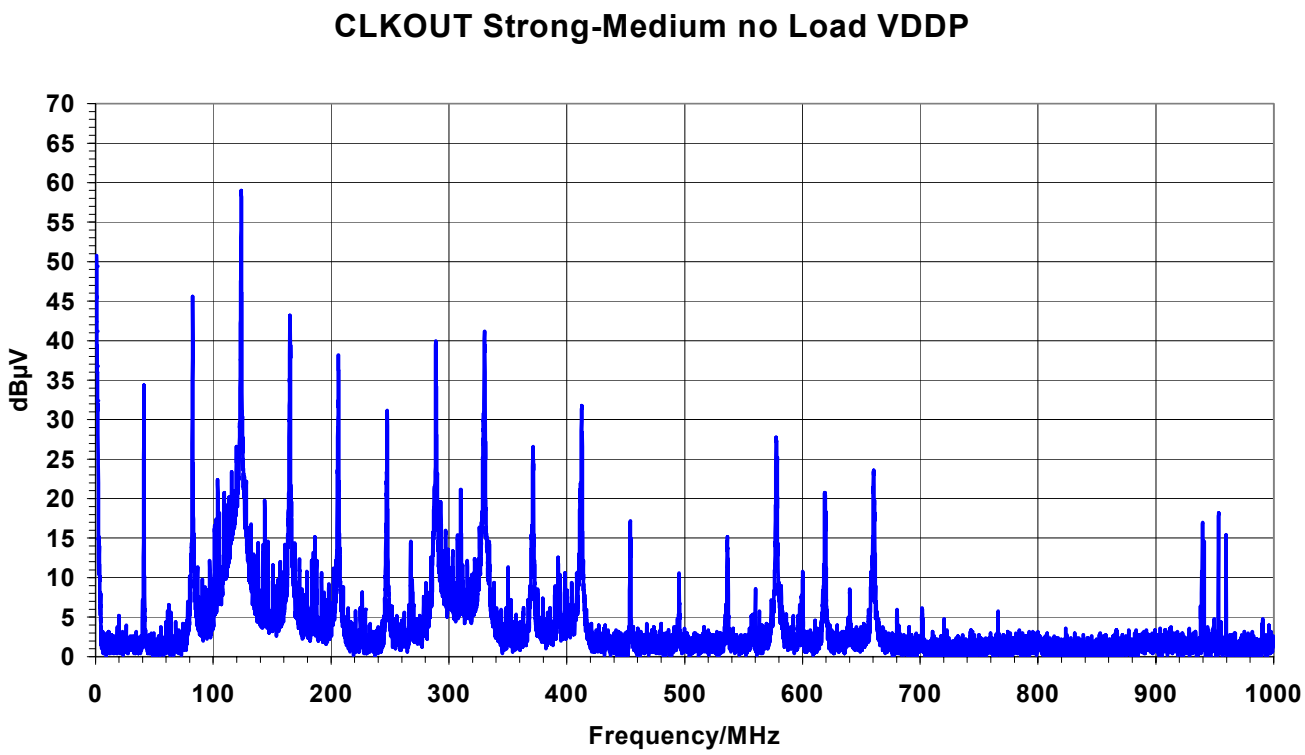


*Figure 103: CLKOUT „Strong-Medium“ driver at 0pF load – conducted emission on VDDP*

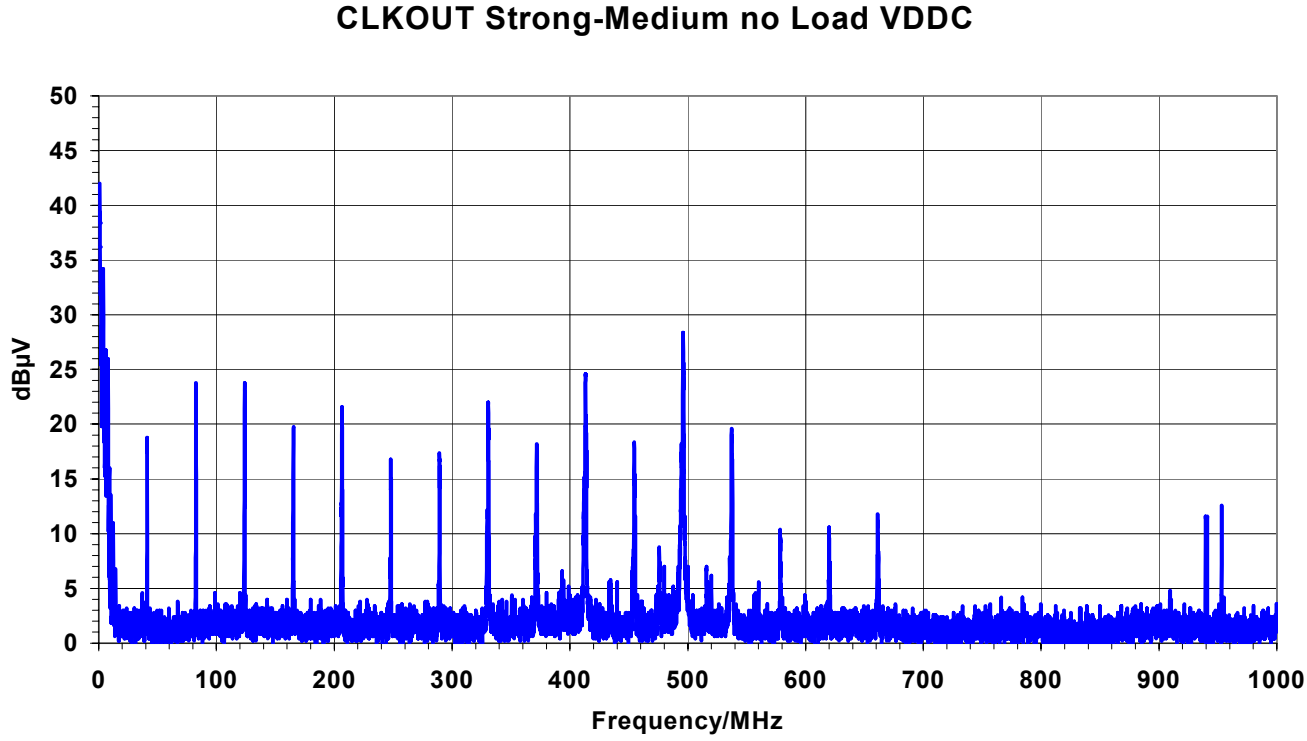


*Figure 104: CLKOUT „Strong-Medium“ driver at 0pF load – conducted emission on VDDC*

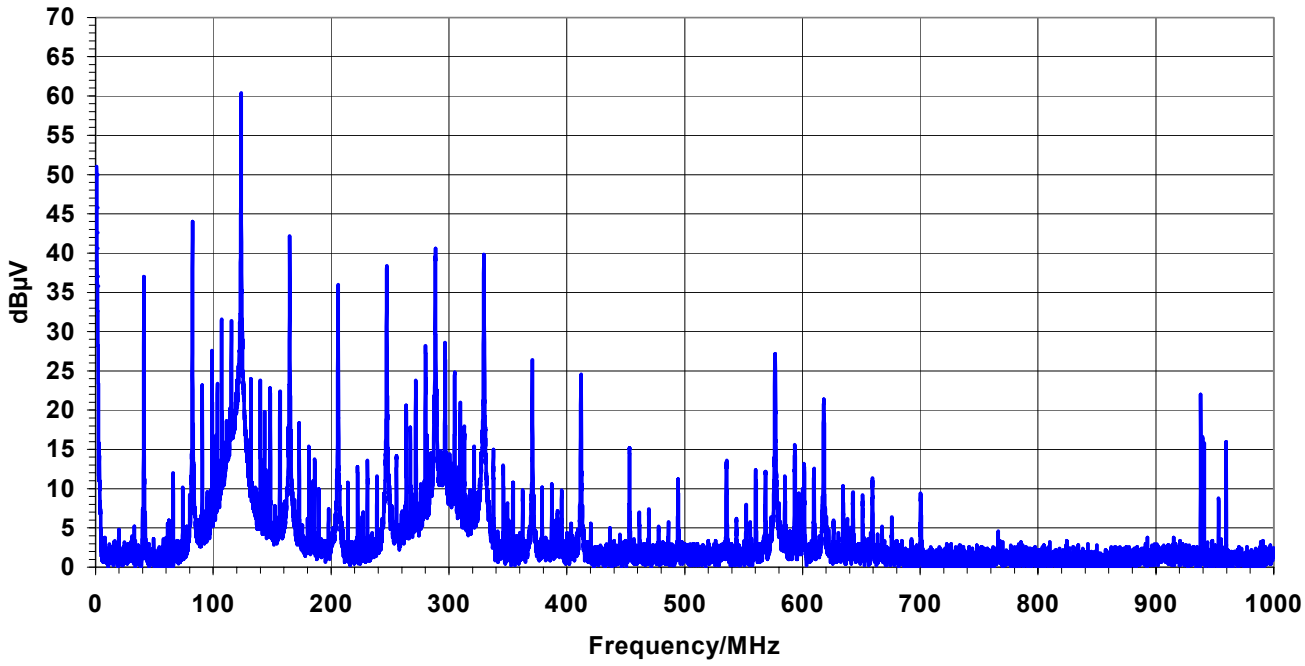


*Figure 105: CLKOUT „Strong-Medium“ driver at 10pF load – conducted emission on VDDP*

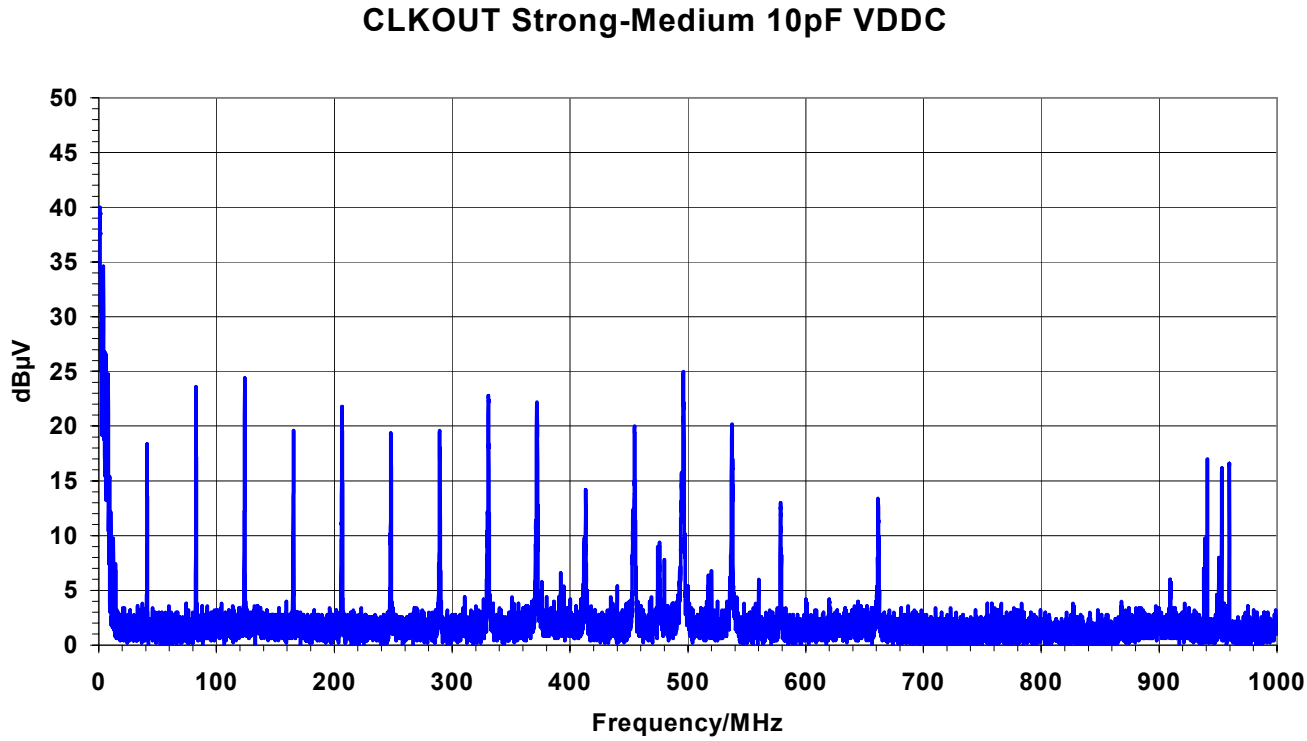


*Figure 106: CLKOUT „Strong-Medium“ driver at 10pF load – conducted emission on VDDC*

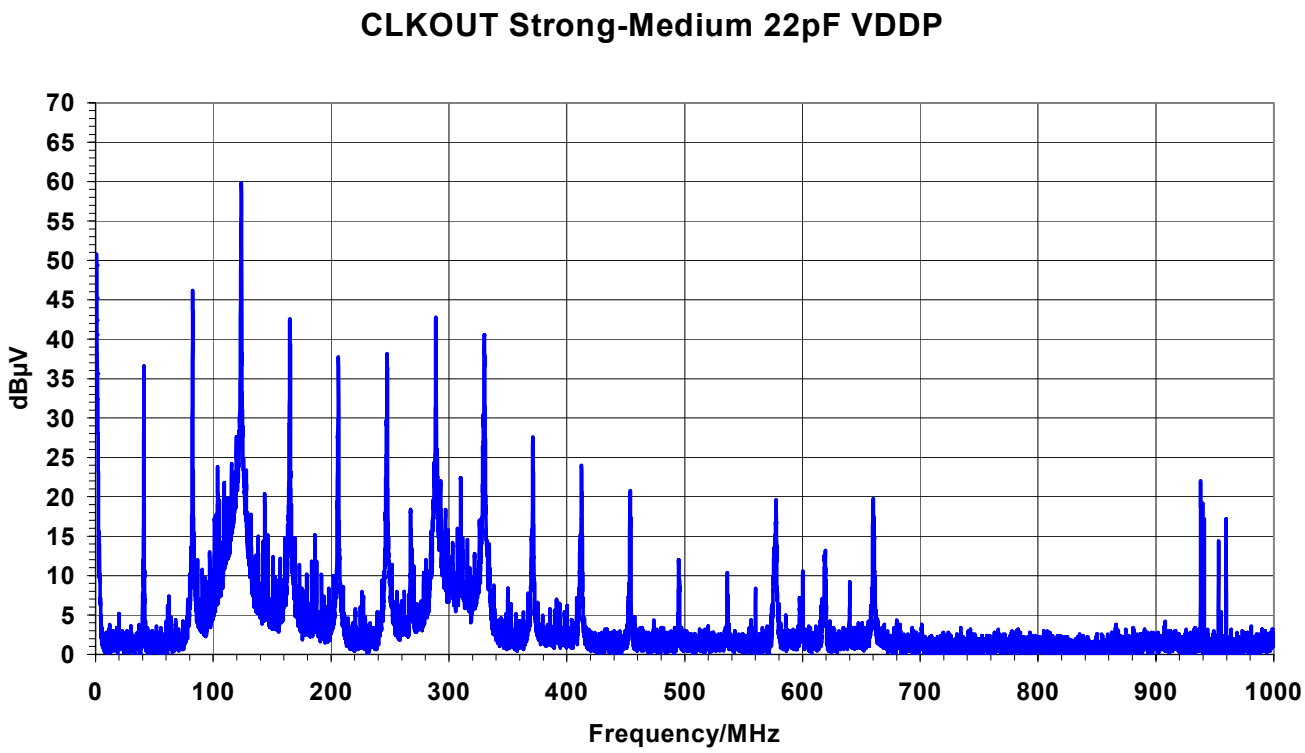


*Figure 107: CLKOUT „Strong-Medium“ driver at 22pF load – conducted emission on VDDP*

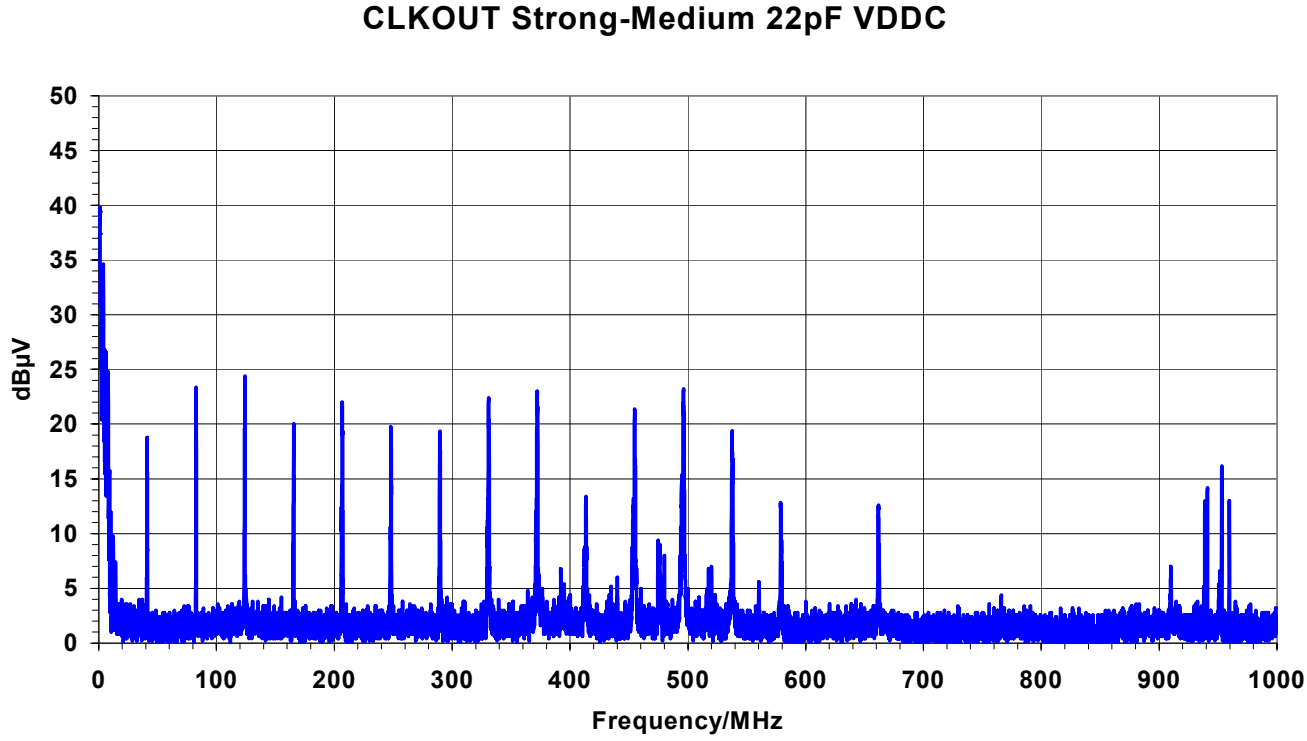


*Figure 108: CLKOUT „Strong-Medium“ driver at 22pF load – conducted emission on VDDC*

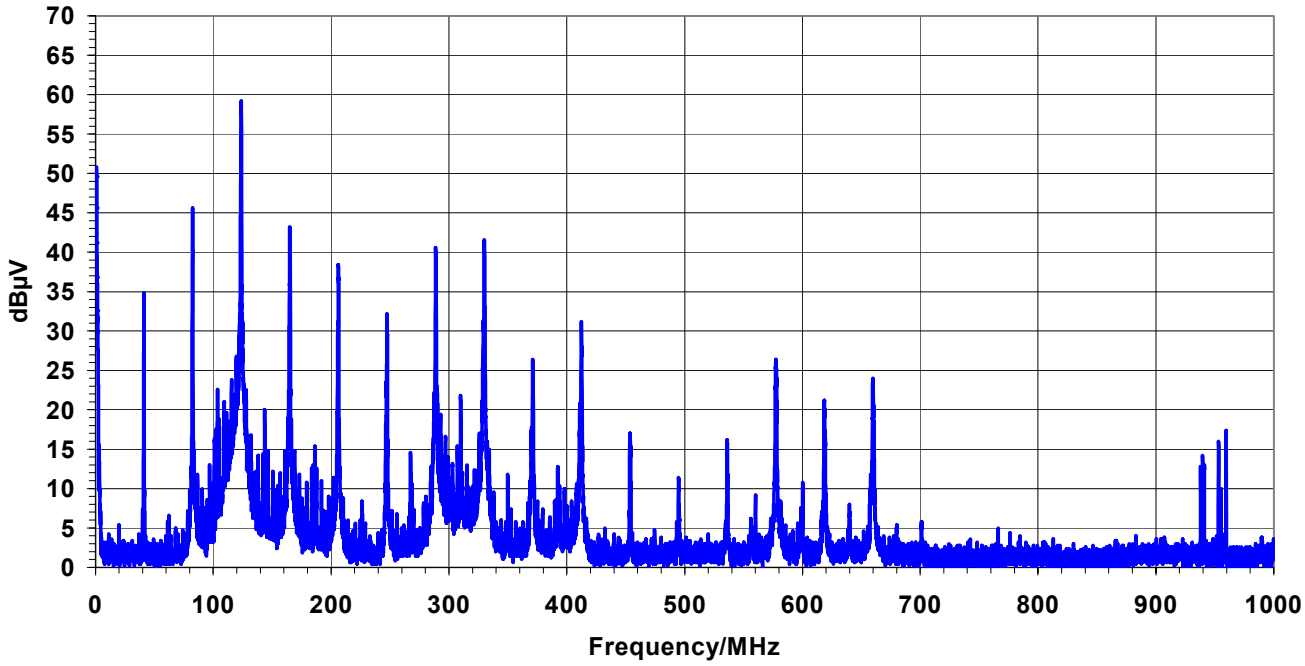


*Figure 109: CLKOUT „Strong-Medium“ driver at 33pF load – conducted emission on VDDP*

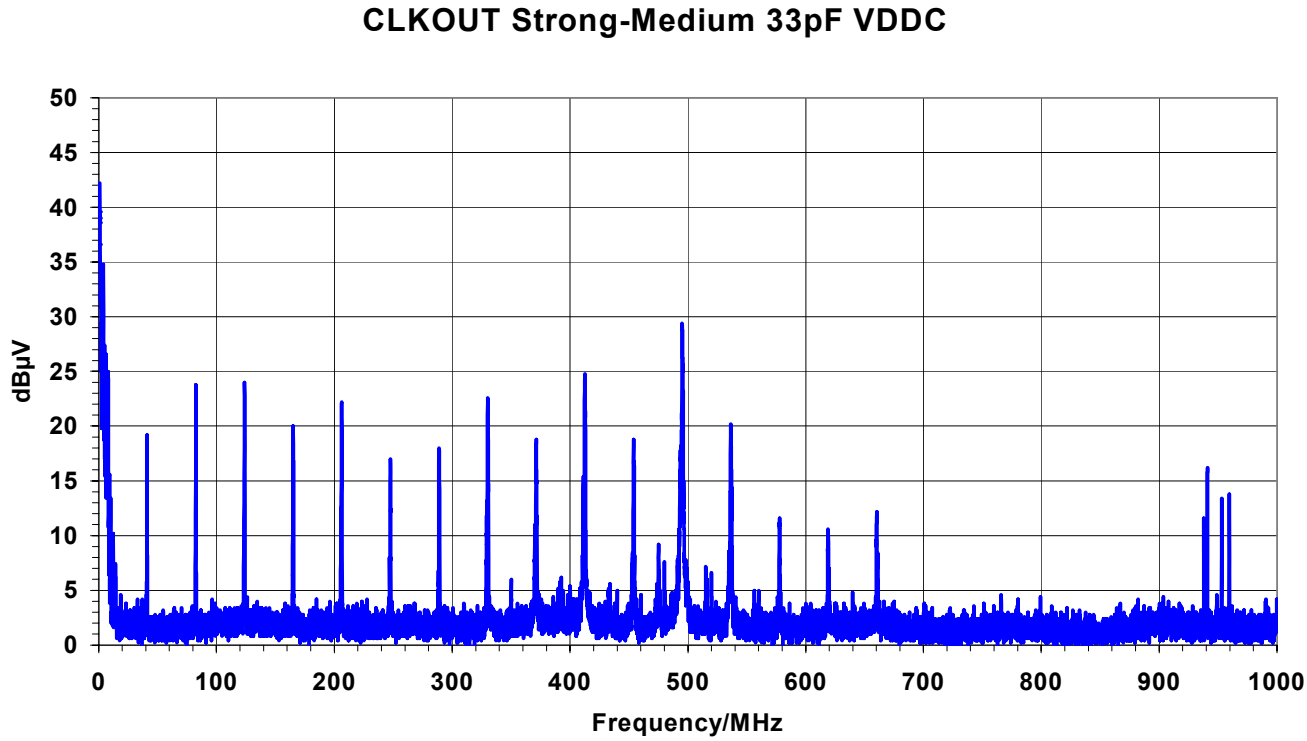


*Figure 110: CLKOUT „Strong-Medium“ driver at 33pF load – conducted emission on VDDC*

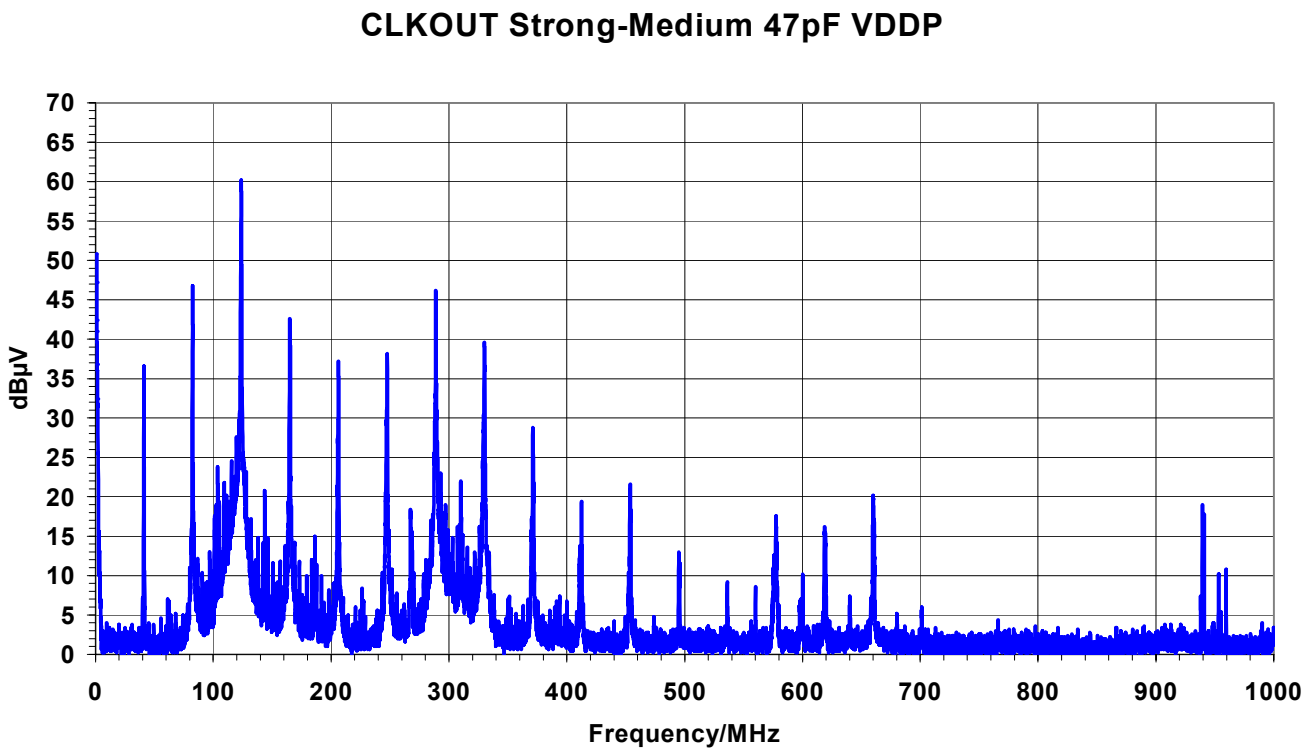


*Figure 111: CLKOUT „Strong-Medium“ driver at 47pF load – conducted emission on VDDP*

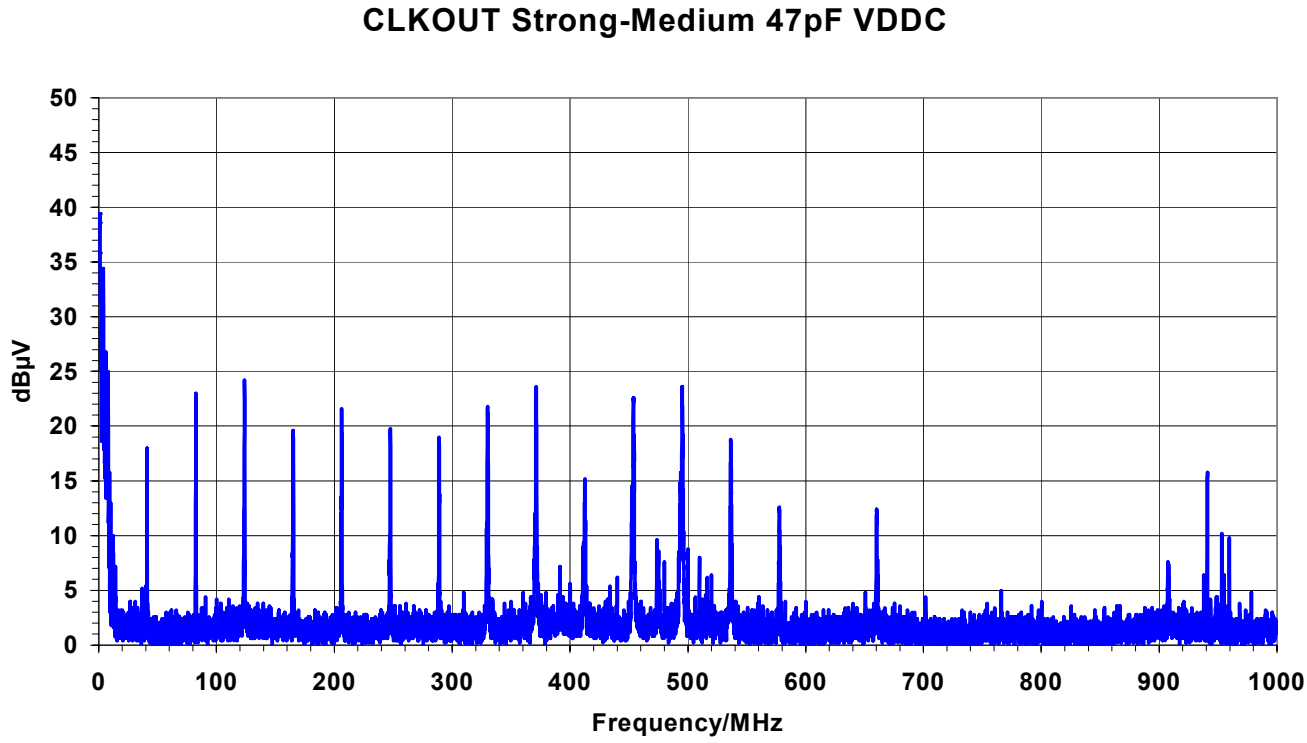


*Figure 112: CLKOUT „Strong-Medium“ driver at 47pF load – conducted emission on VDDC*

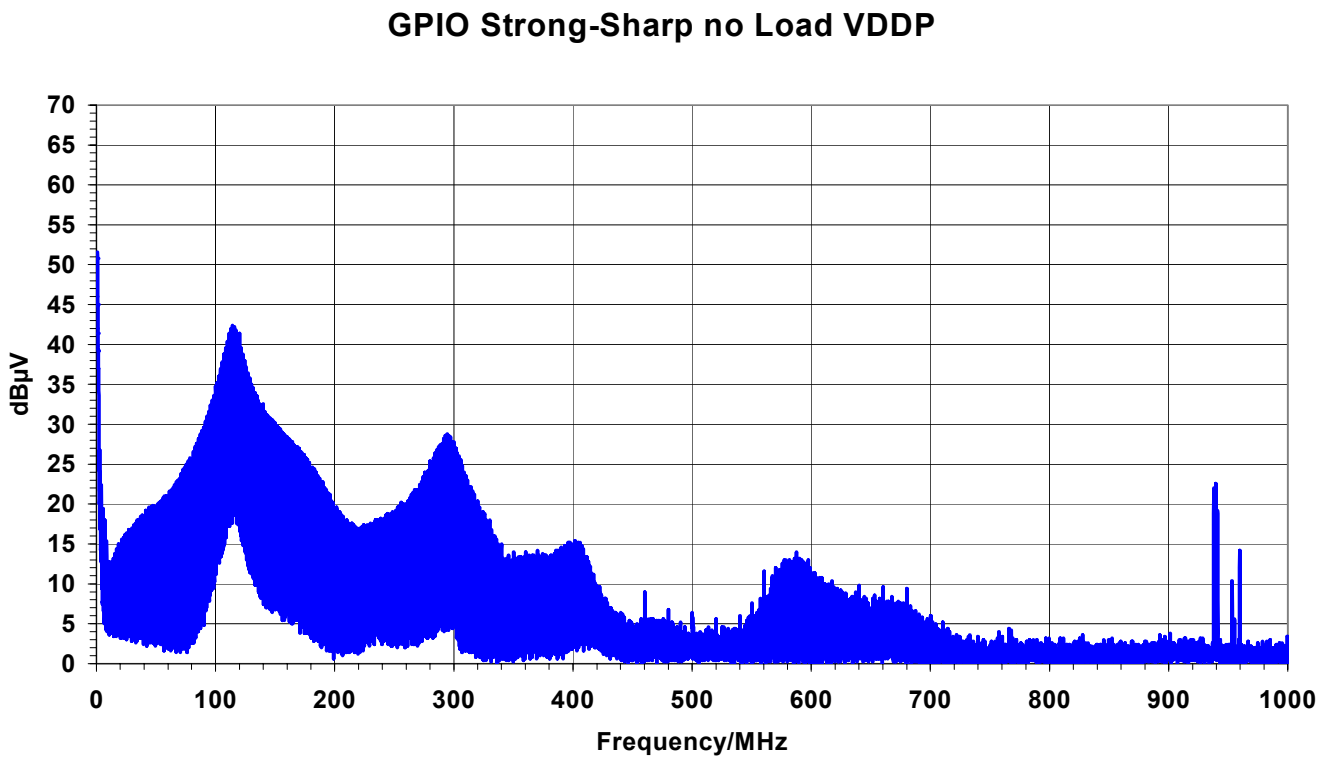


*Figure 113: GPIO „Strong-Sharp“ driver at 0pF load – conducted emission on VDDP*

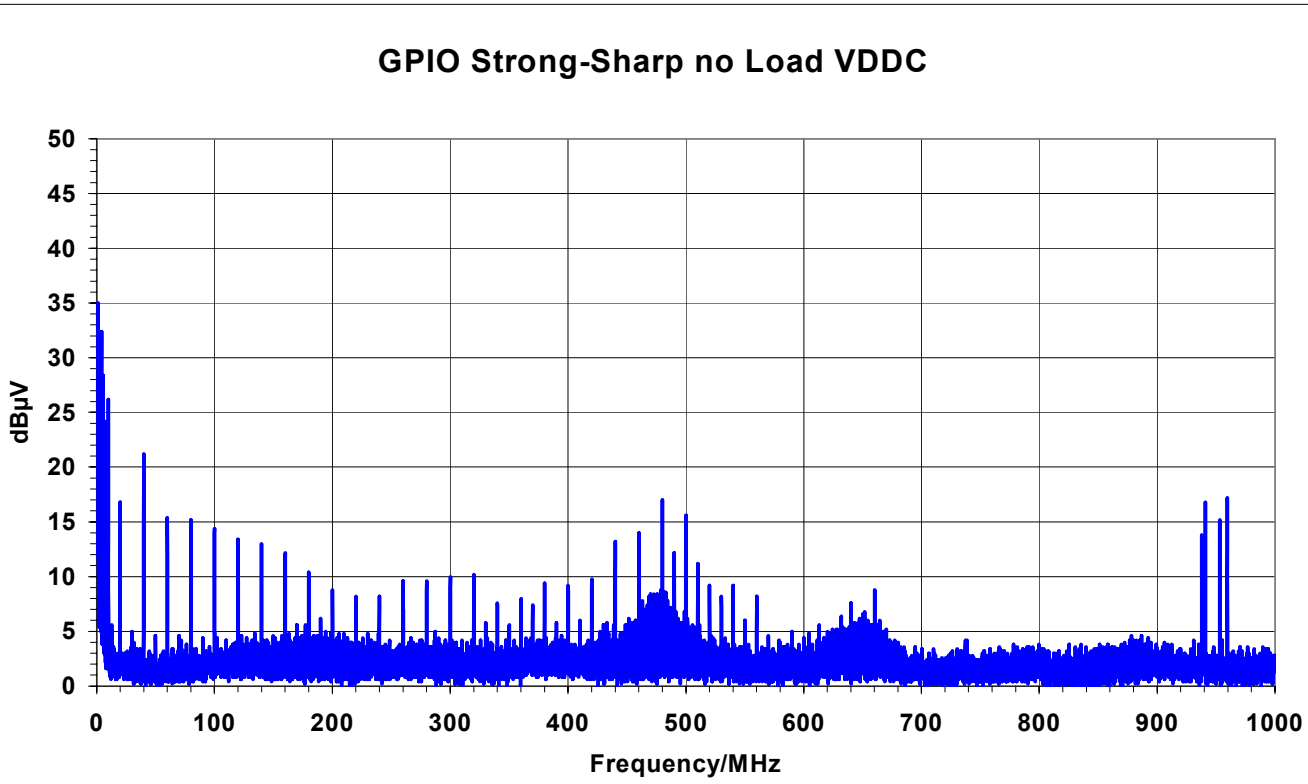


*Figure 114: GPIO „Strong-Sharp“ driver at 0pF load – conducted emission on VDDC*

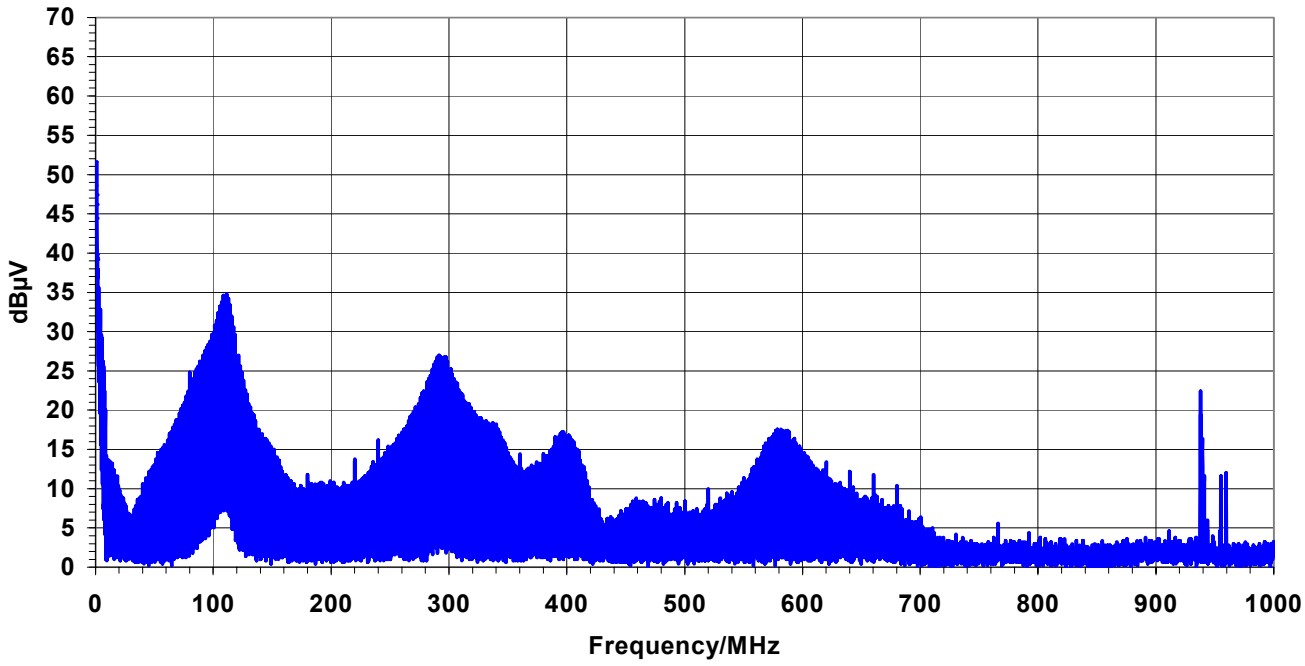


*Figure 115: GPIO „Strong-Sharp“ driver at 22pF load – conducted emission on VDDP*

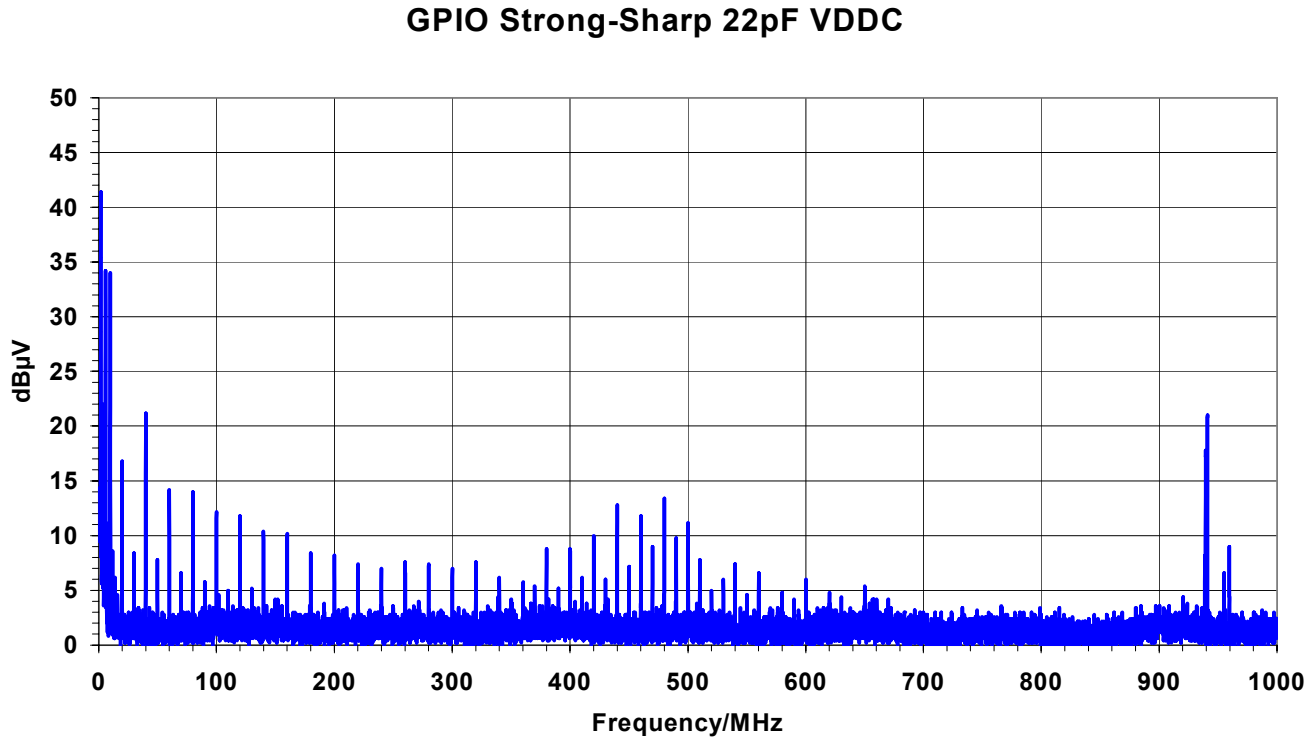


*Figure 116: GPIO „Strong-Sharp“ driver at 22pF load – conducted emission on VDDC*

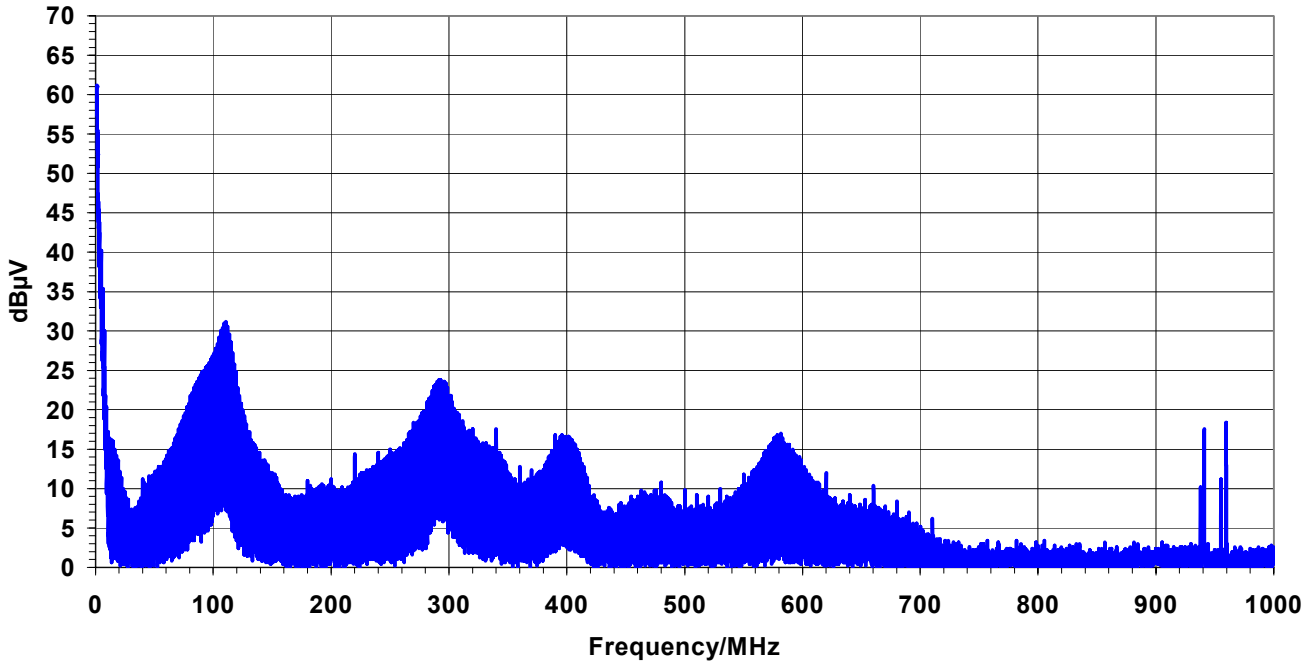


*Figure 117 GPIO „Strong-Sharp“ driver at 47pF load – conducted emission on VDDP*

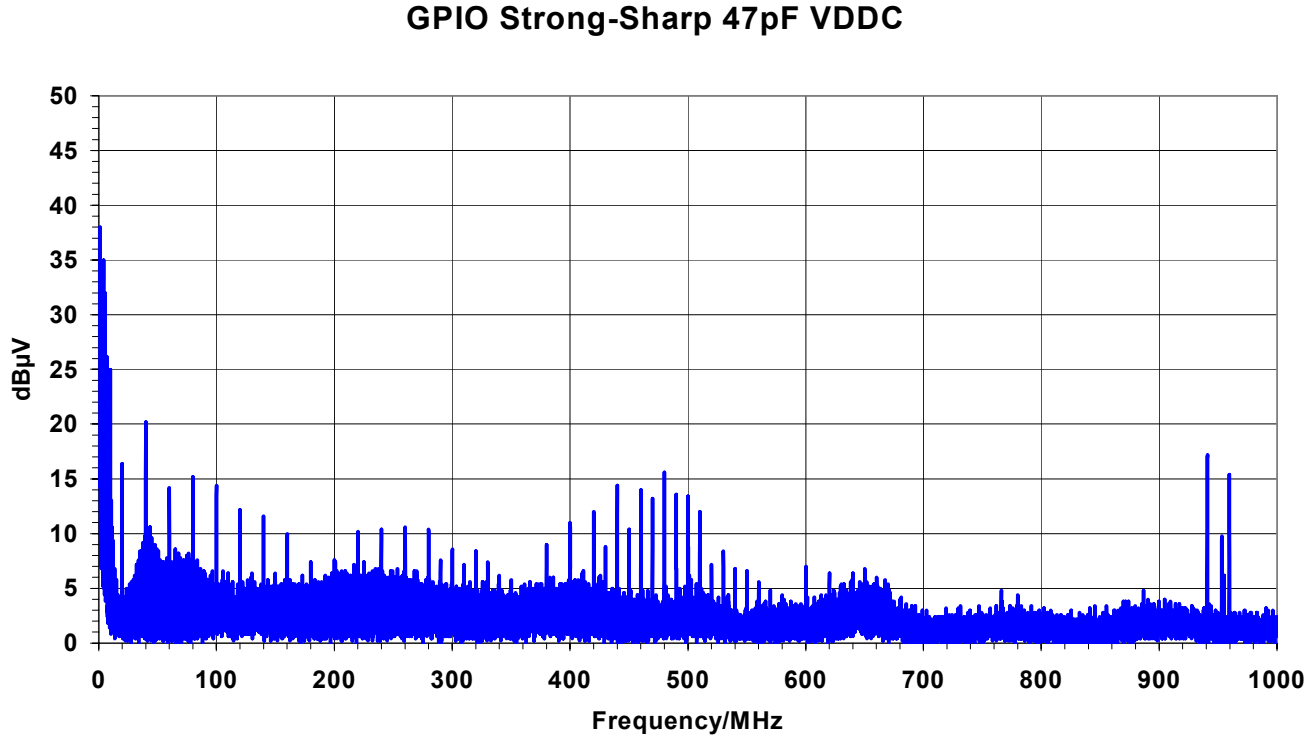


*Figure 118: GPIO „Strong-Sharp“ driver at 47pF load – conducted emission on VDDC*

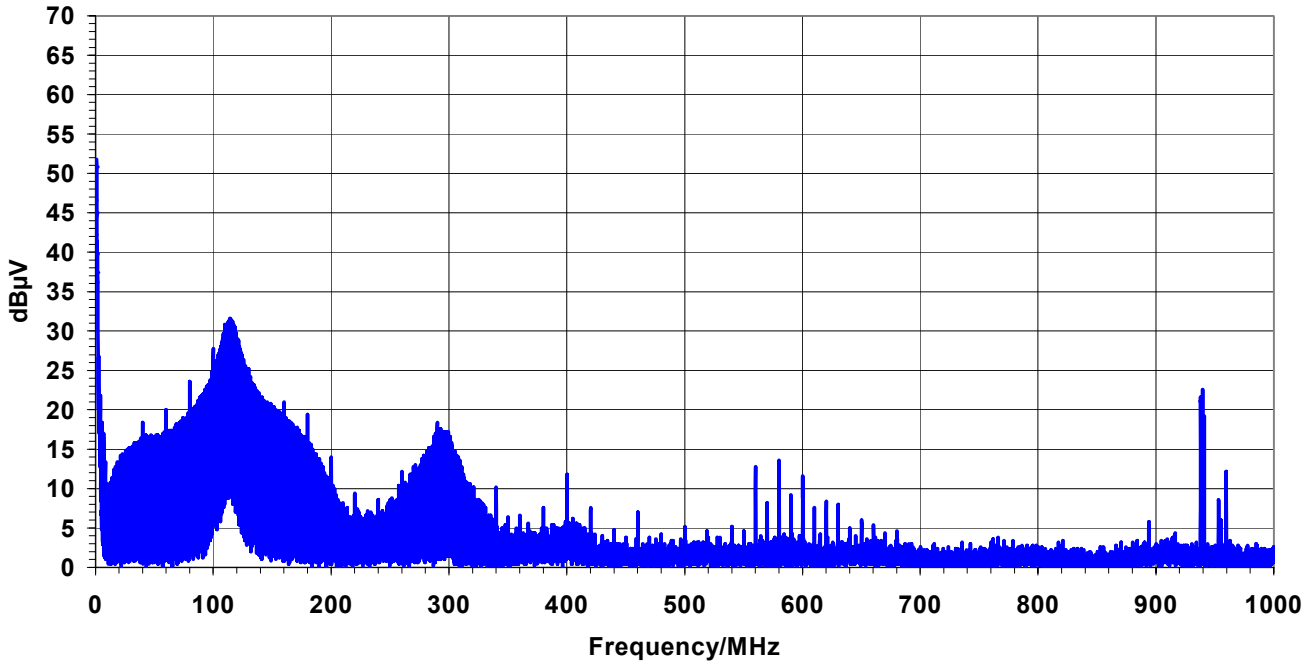


*Figure 119: GPIO „Strong-Medium“ driver at 0pF load – conducted emission on VDDP*

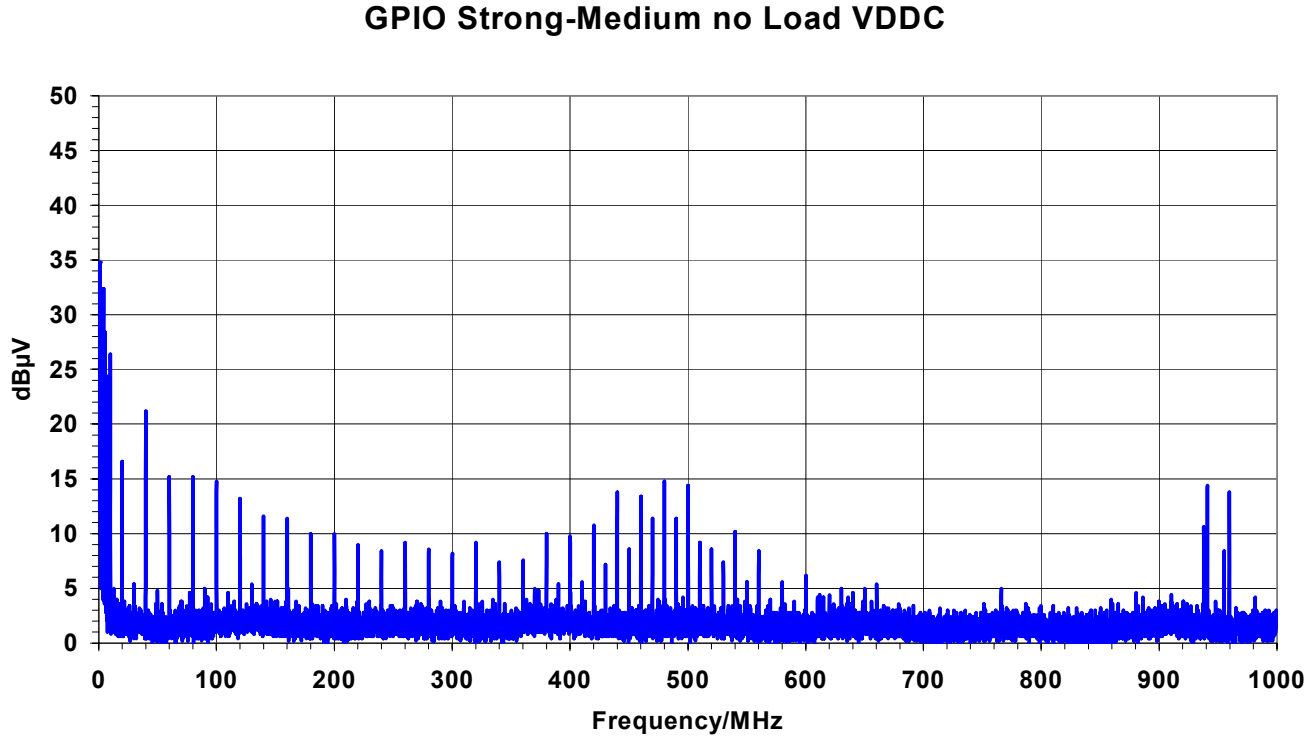


*Figure 120: GPIO „Strong-Medium“ driver at 0pF load – conducted emission on VDDC*

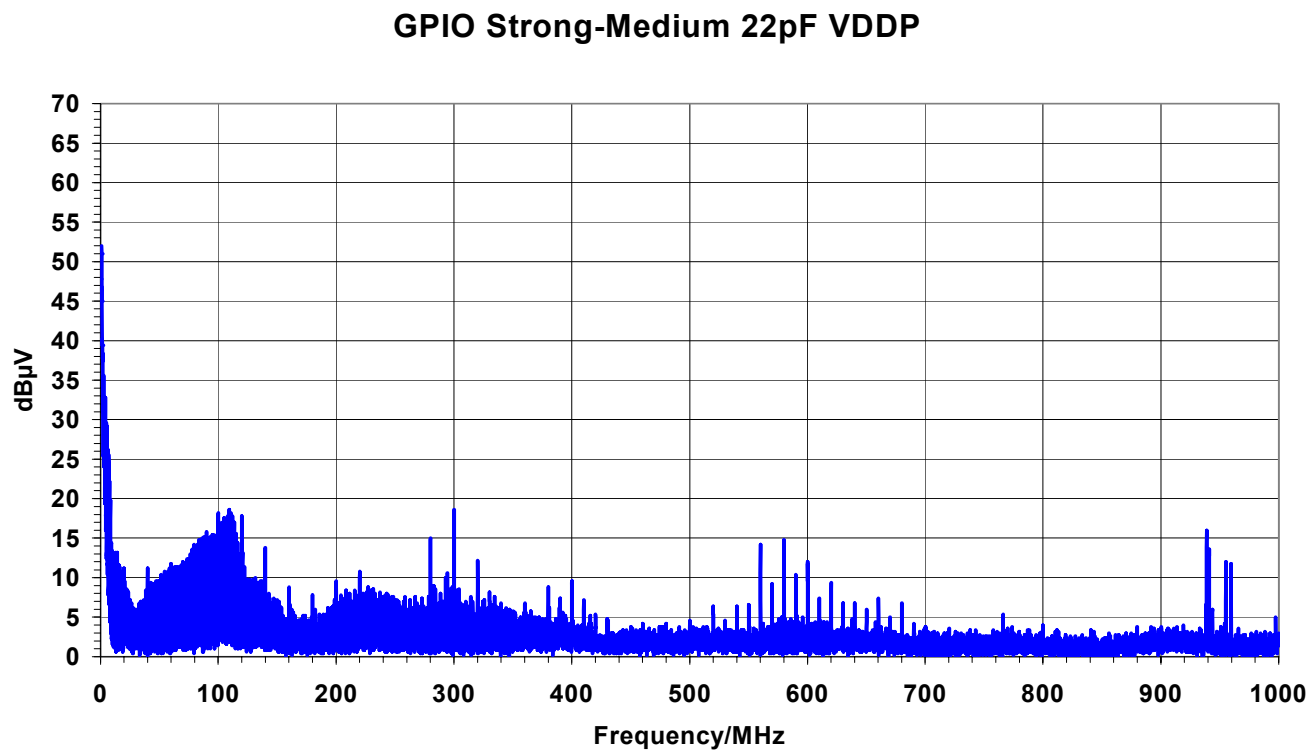


*Figure 121: GPIO „Strong-Medium“ driver at 22pF load – conducted emission on VDDP*

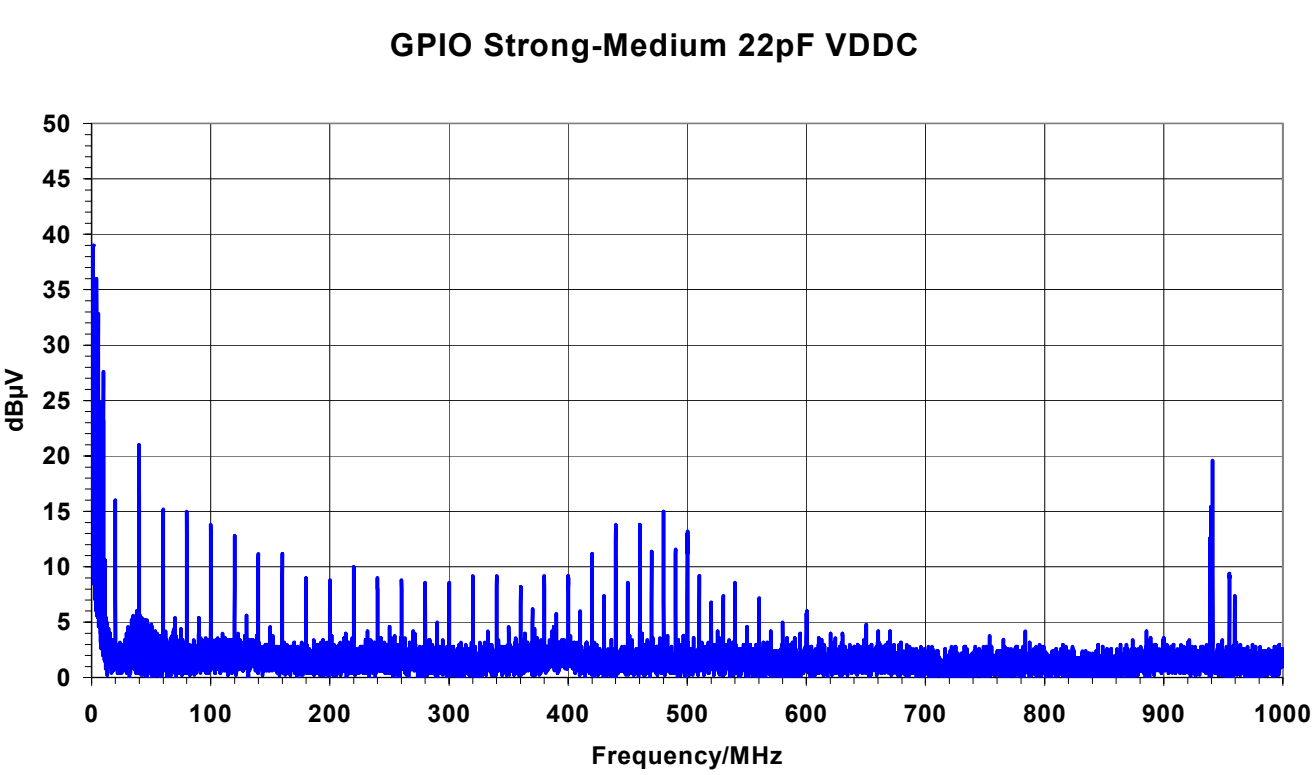


*Figure 122: GPIO „Strong-Medium“ driver at 22pF load – conducted emission on VDDC*

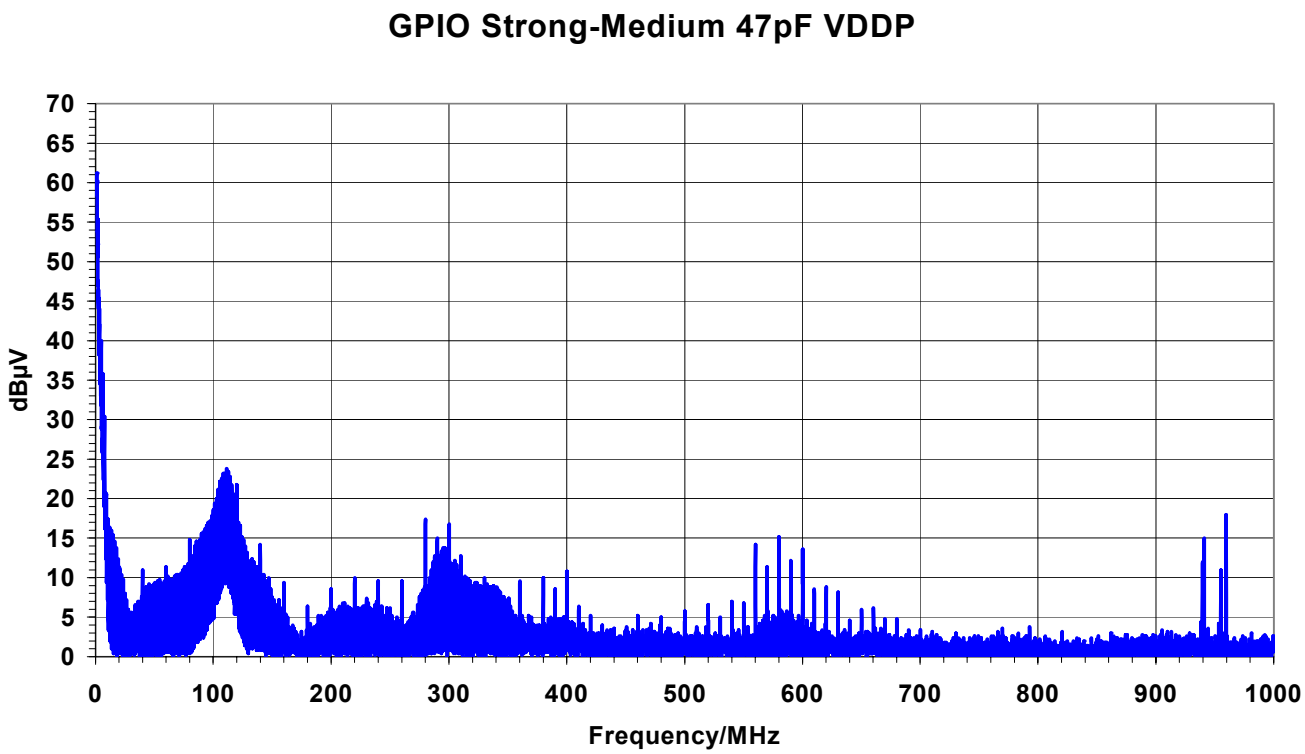


*Figure 123: GPIO „Strong-Medium“ driver at 47pF load – conducted emission on VDDP*

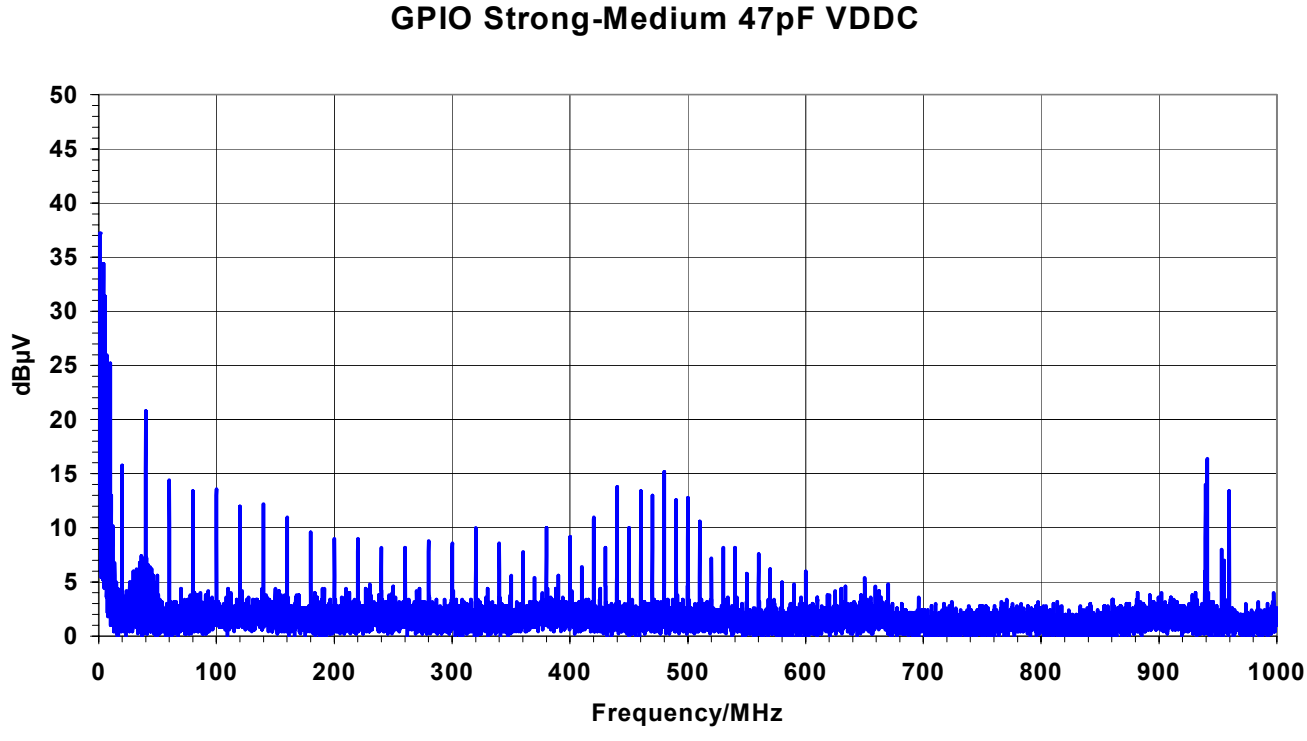


*Figure 124: GPIO „Strong-Medium“ driver at 47pF load – conducted emission on VDDC*

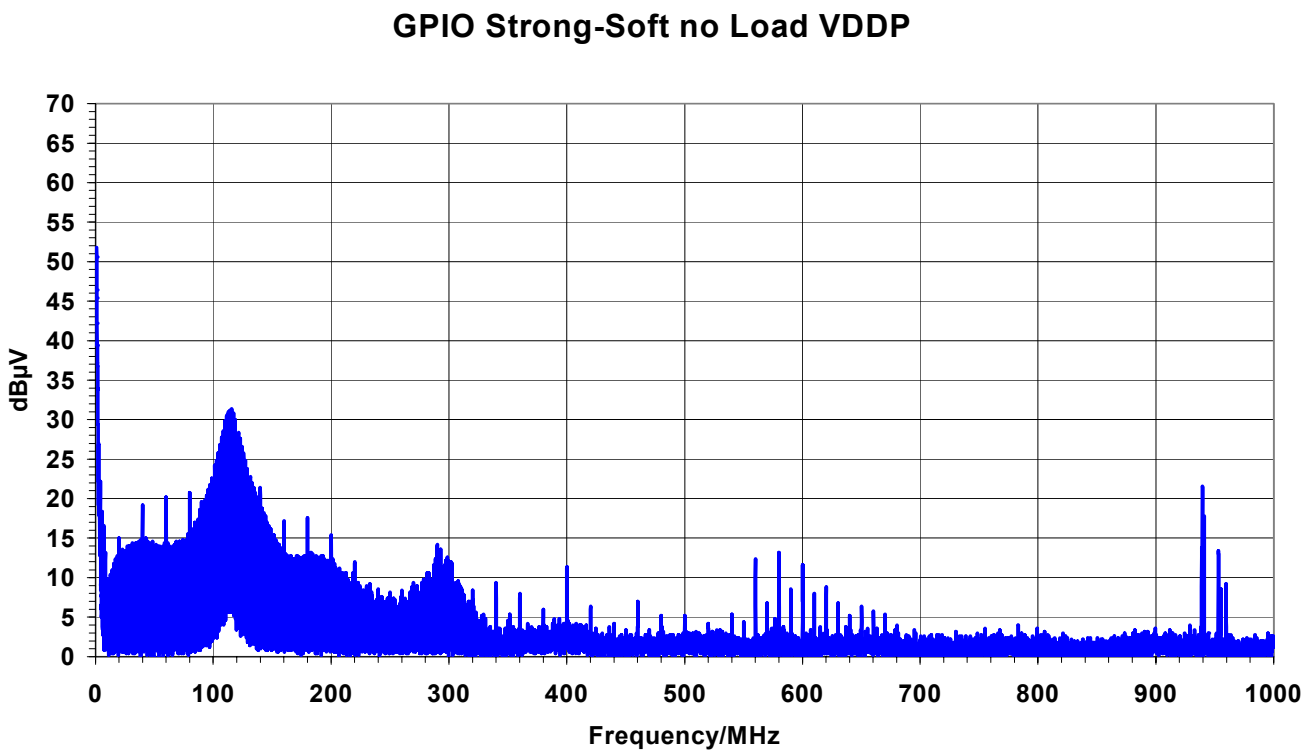


*Figure 125: GPIO „Strong-Soft“ driver at 0pF load – conducted emission on VDDP*

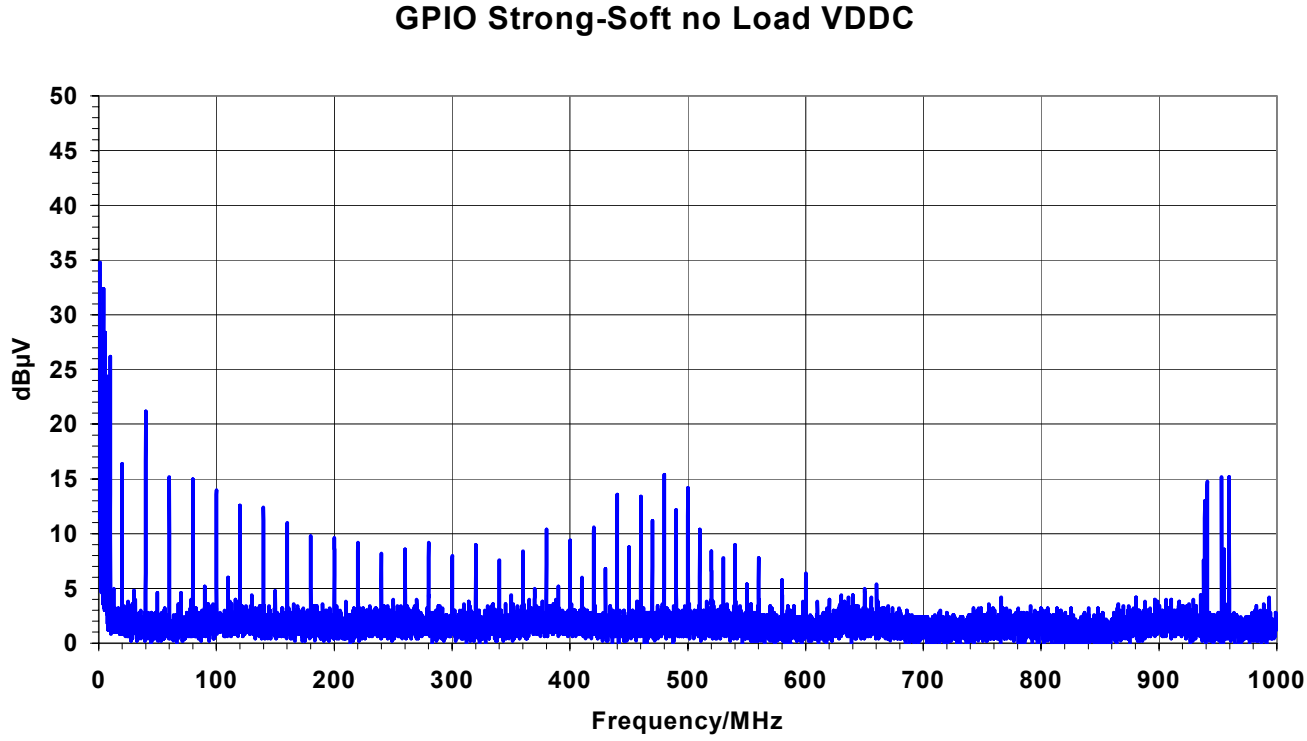


*Figure 126: GPIO „Strong-Soft“ driver at 0pF load – conducted emission on VDDC*

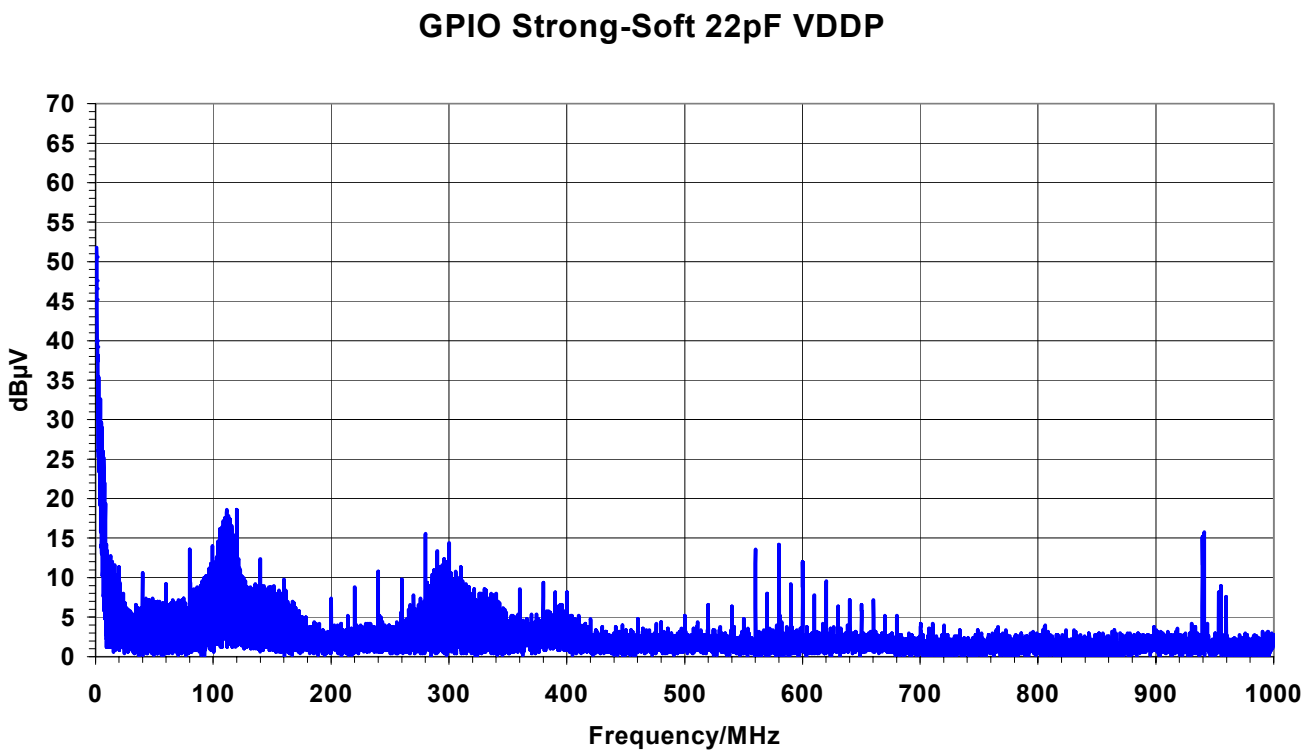


*Figure 127: GPIO „Strong-Soft“ driver at 22pF load – conducted emission on VDDP*

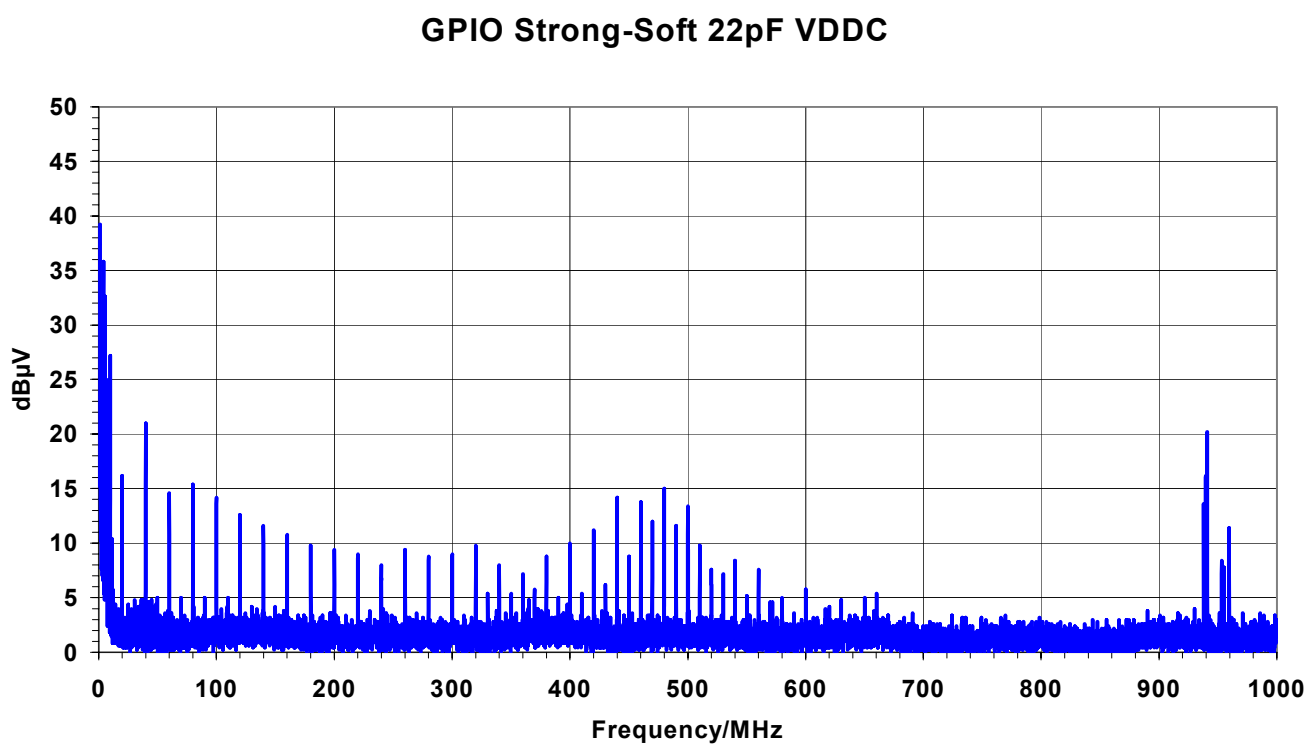


*Figure 128: GPIO „Strong-Soft“ driver at 22pF load – conducted emission on VDDC*

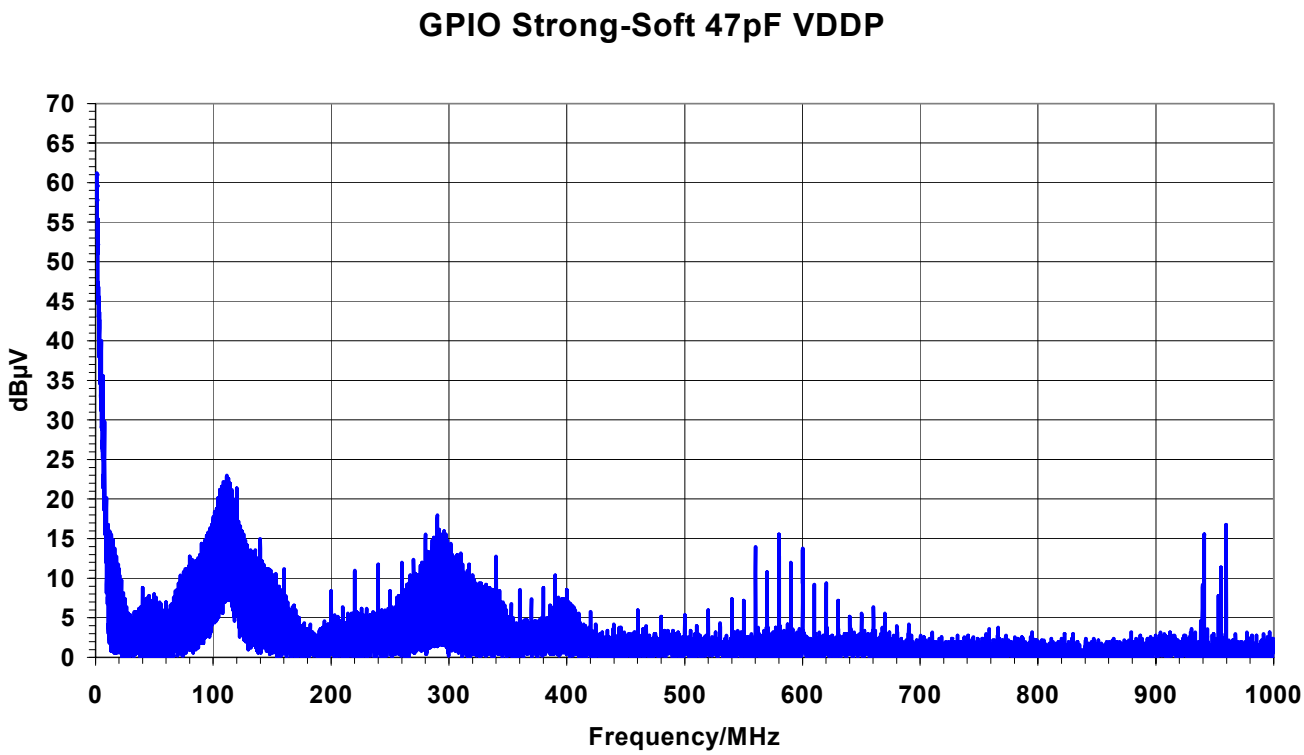


*Figure 129: GPIO „Strong-Soft“ driver at 47pF load – conducted emission on VDDP*

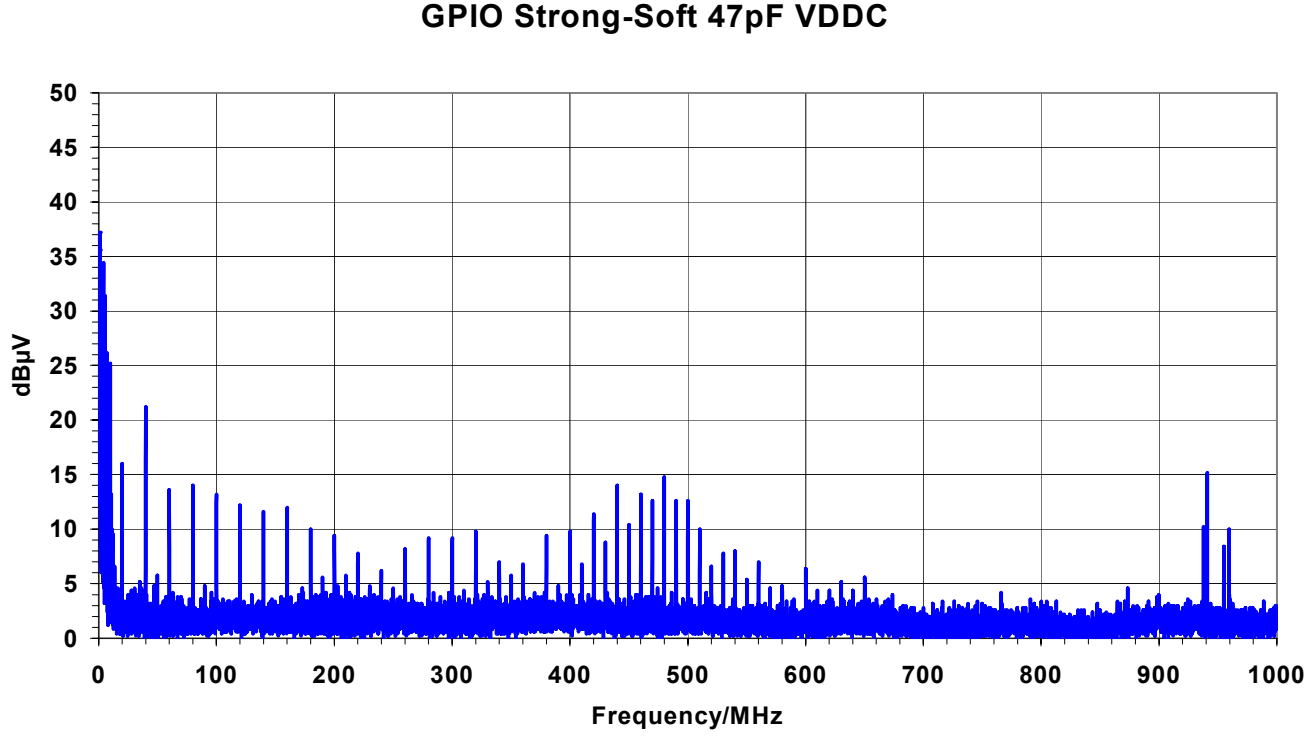


*Figure 130: GPIO „Strong-Soft“ driver at 47pF load – conducted emission on VDDC*

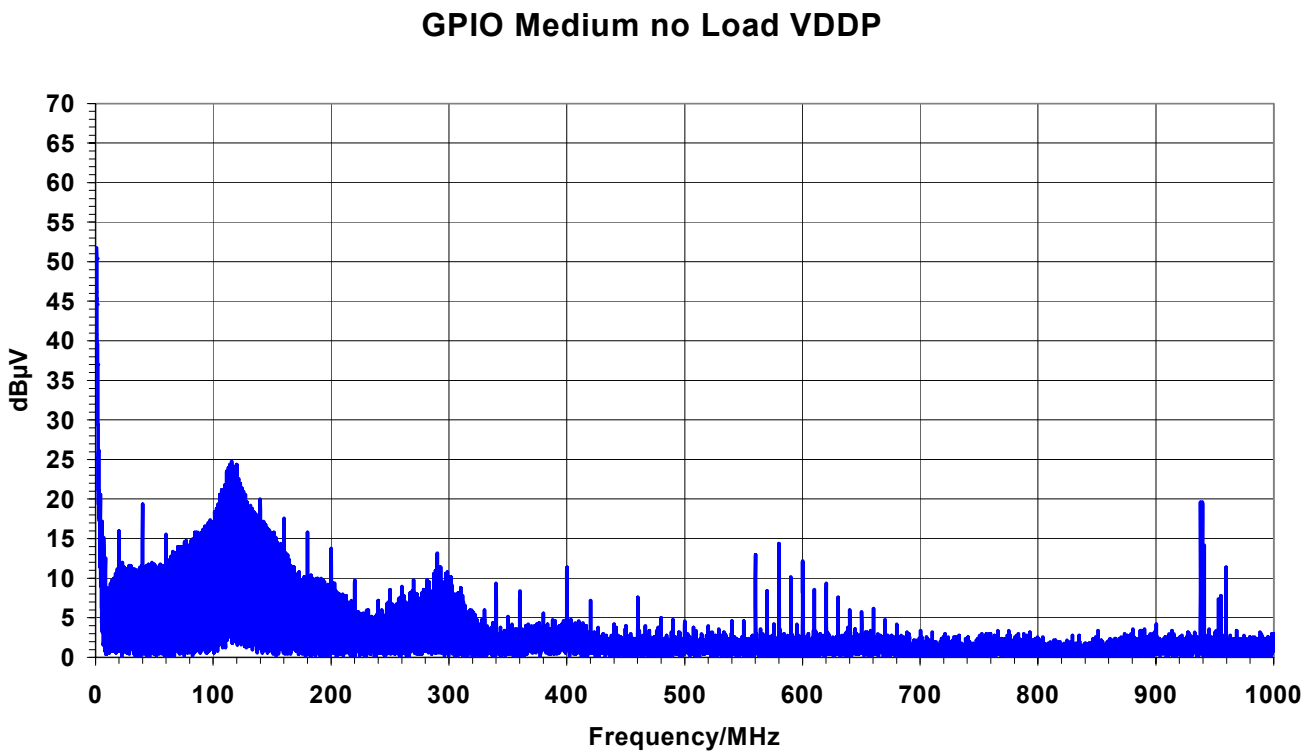


*Figure 131: GPIO „Medium“ driver at 0pF load – conducted emission on VDDP*

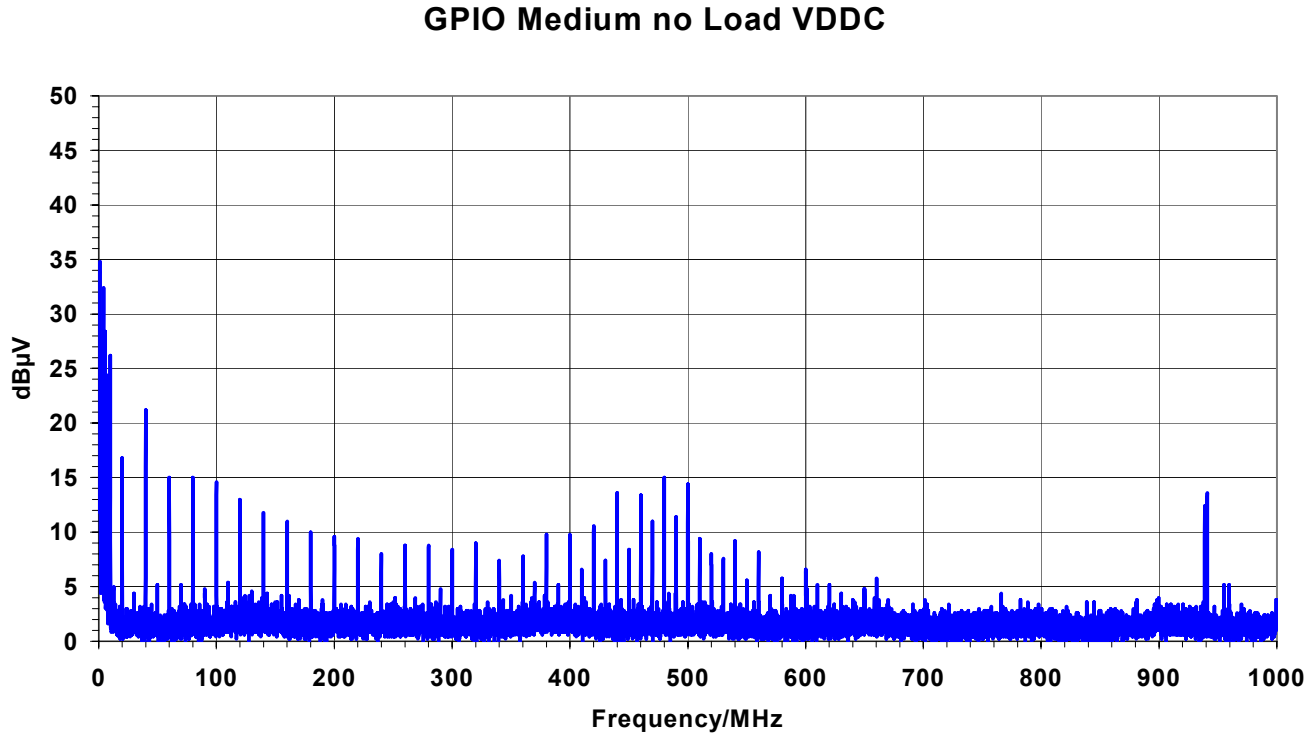


*Figure 132: GPIO „Medium“ driver at 0pF load – conducted emission on VDDC*

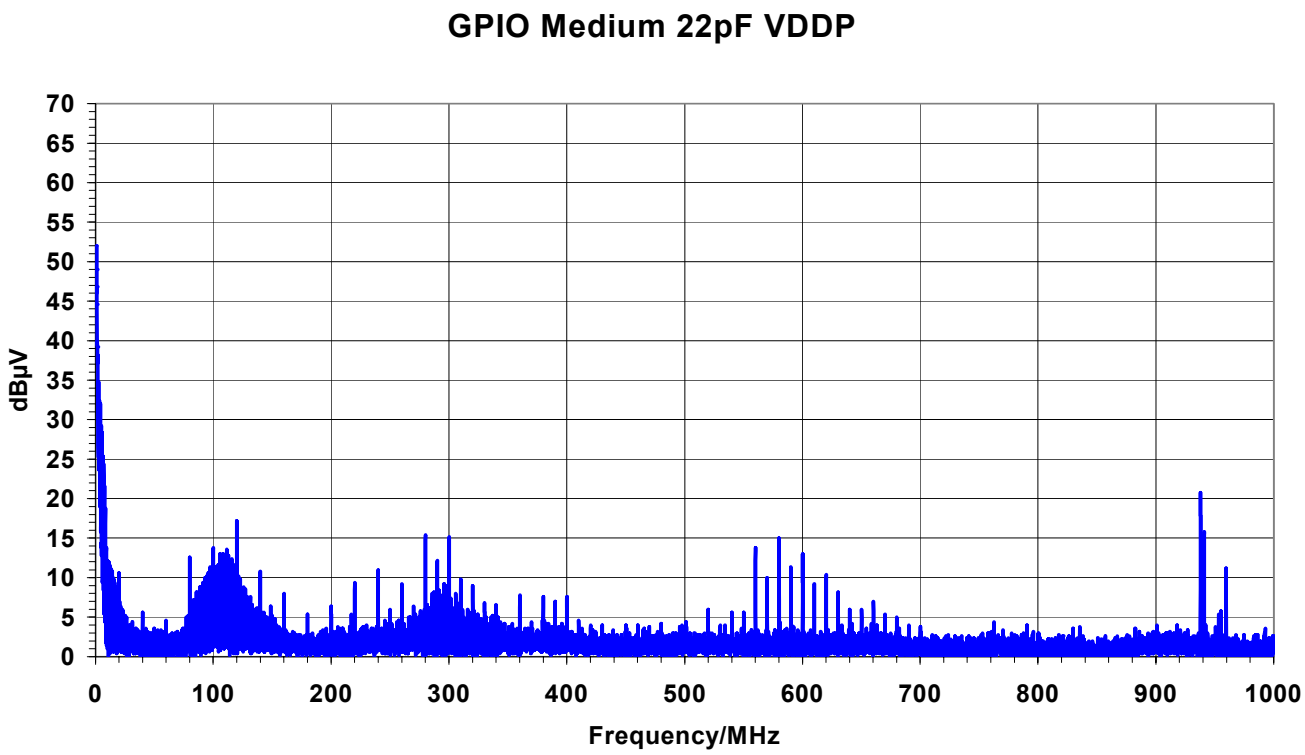


*Figure 133: GPIO „Medium“ driver at 22pF load – conducted emission on VDDP*

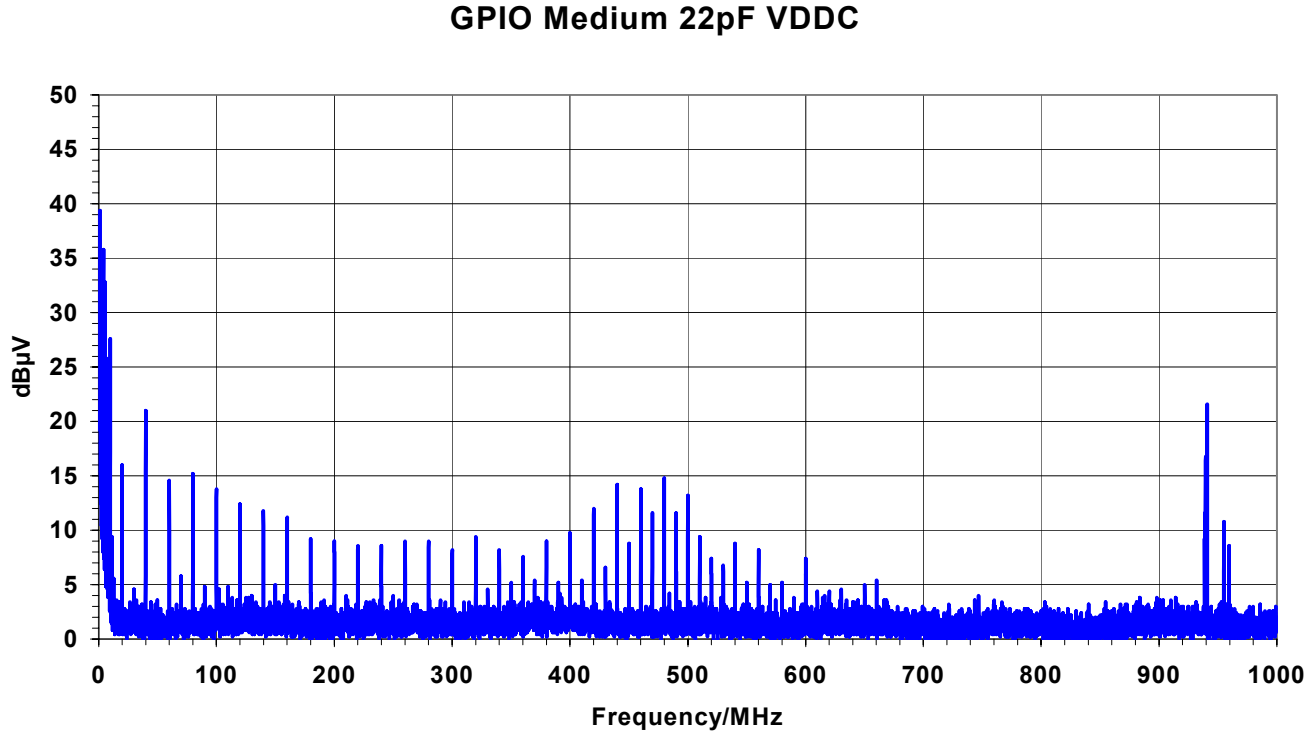


*Figure 134: GPIO „Medium“ driver at 22pF load – conducted emission on VDDC*

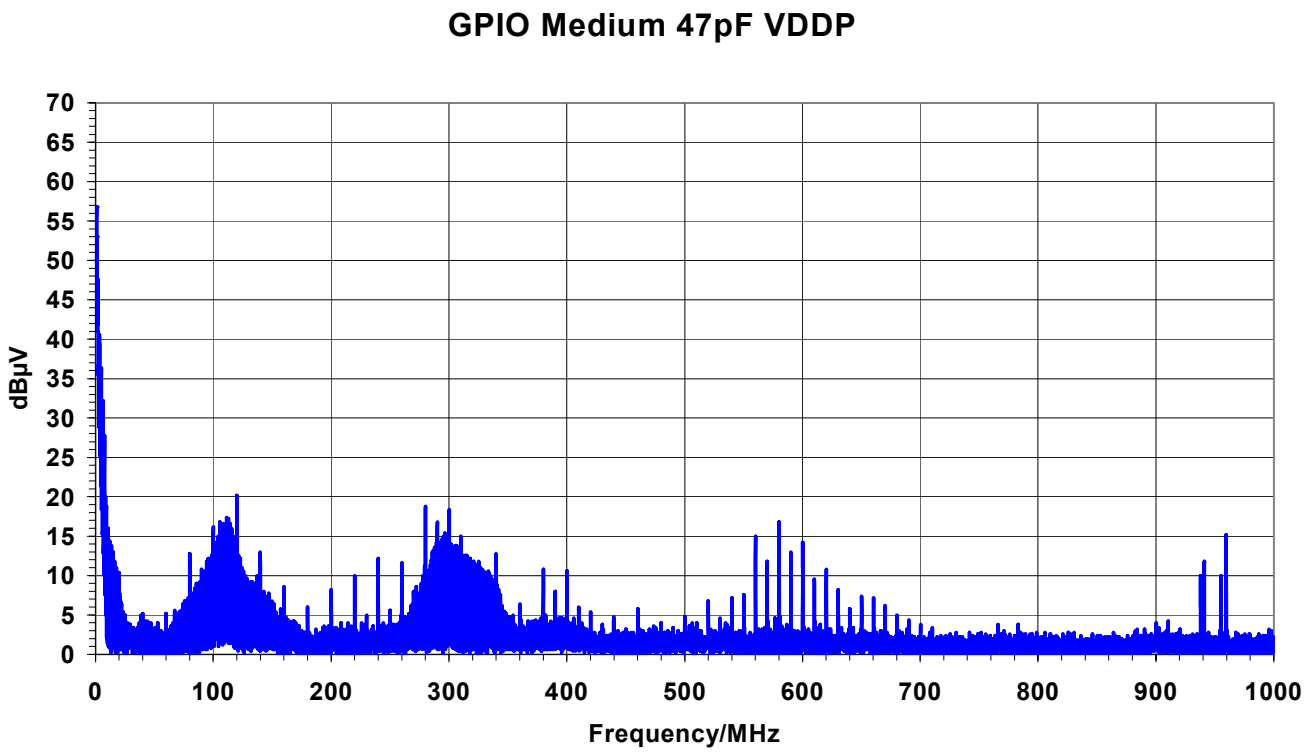


*Figure 135: GPIO „Medium“ driver at 47pF load – conducted emission on VDDP*

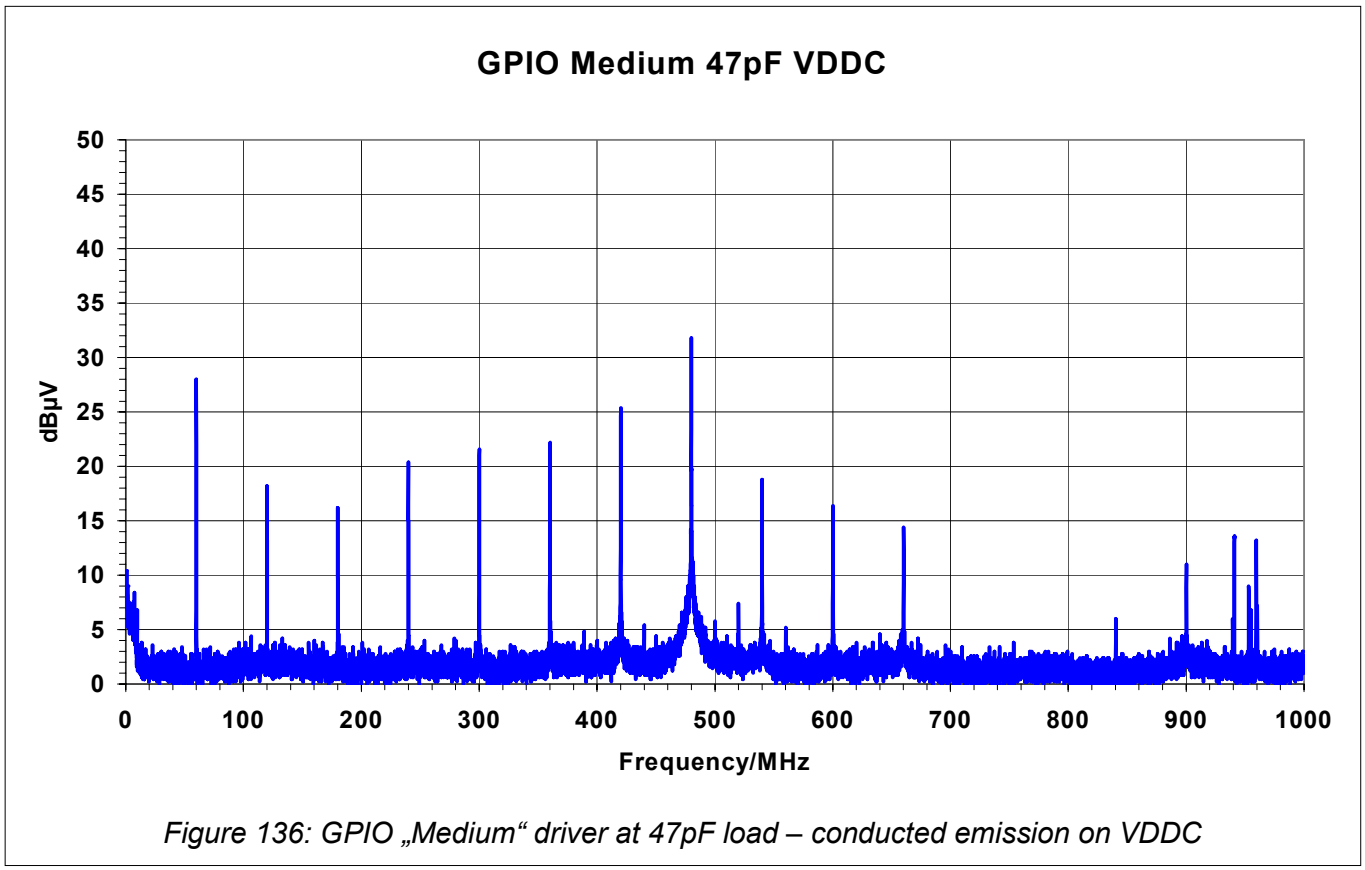


*Figure 136: GPIO „Medium“ driver at 47pF load – conducted emission on VDDC*

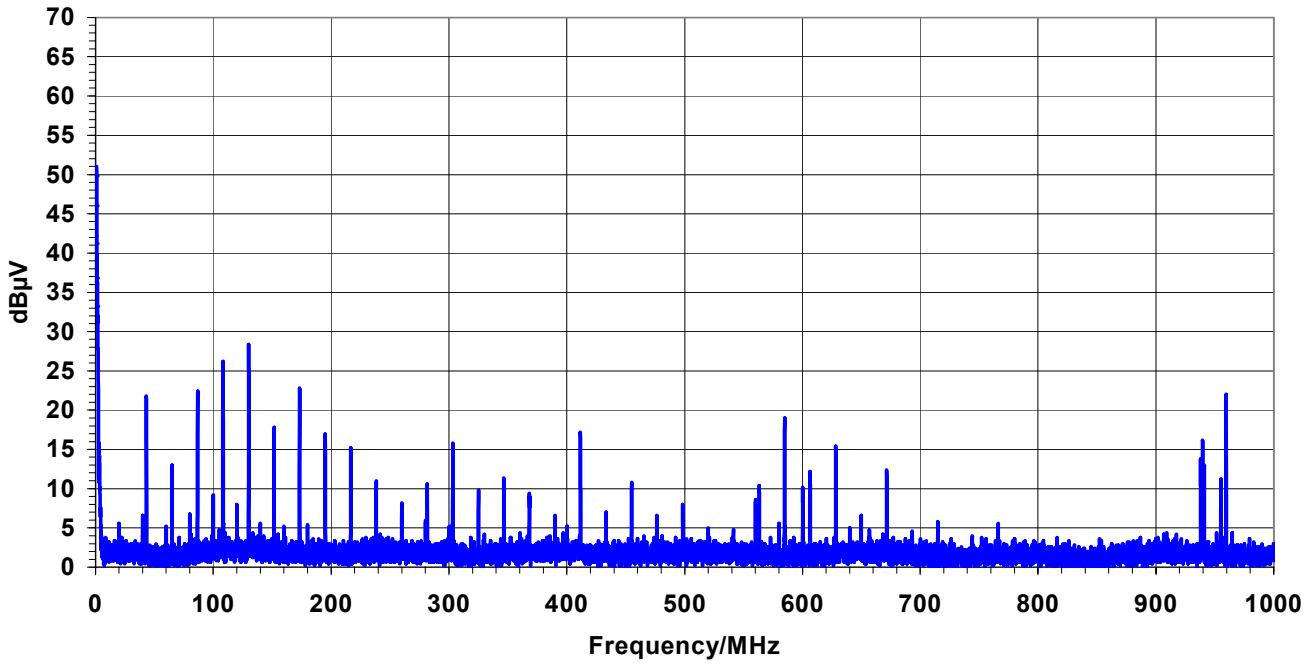


*Figure 137: GPIO „Weak“ driver at 0pF load – conducted emission on VDDP*

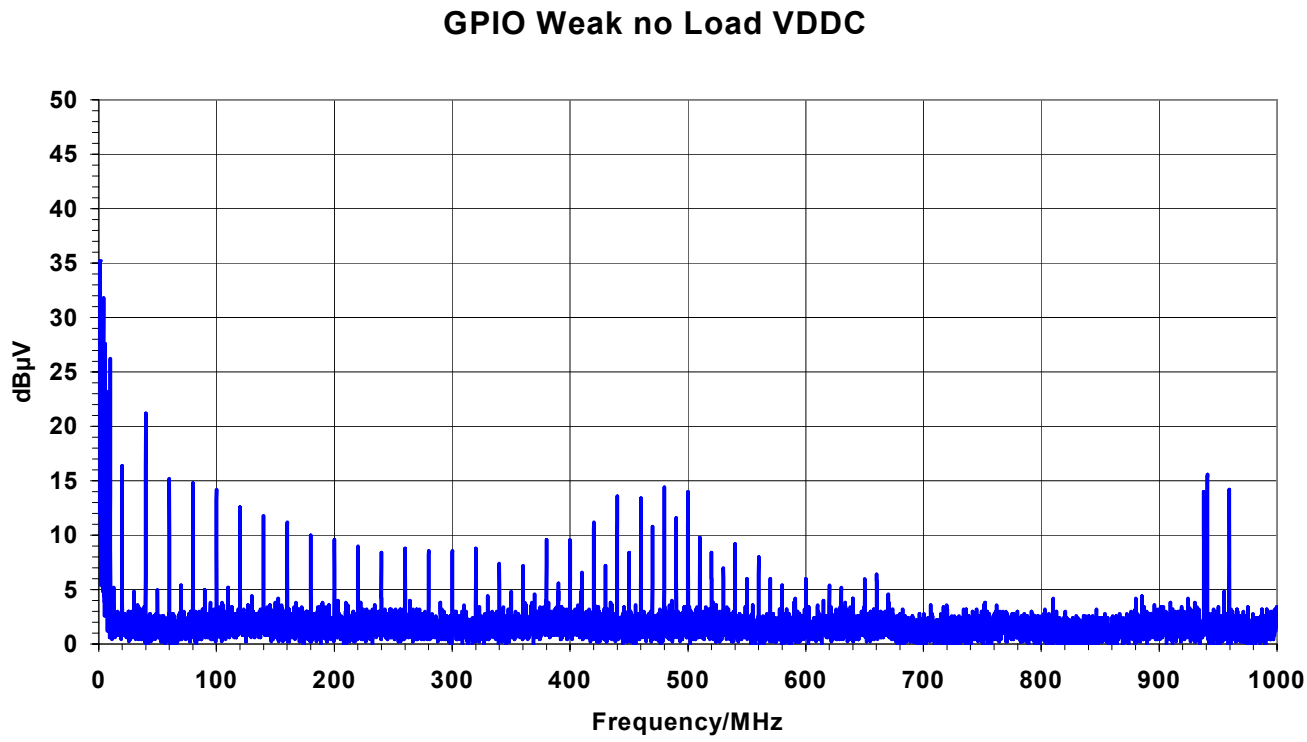


*Figure 138: GPIO „Weak“ driver at 0pF load – conducted emission on VDDC*

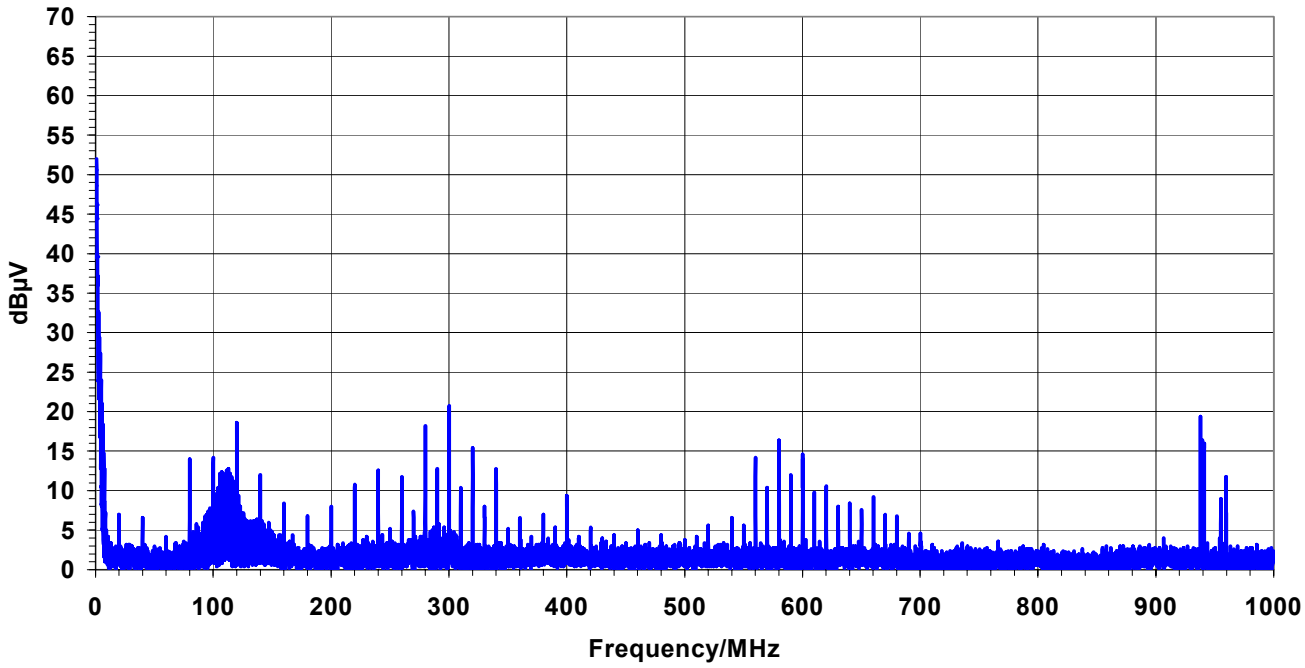


*Figure 139: GPIO „Weak“ driver at 22pF load – conducted emission on VDDP*

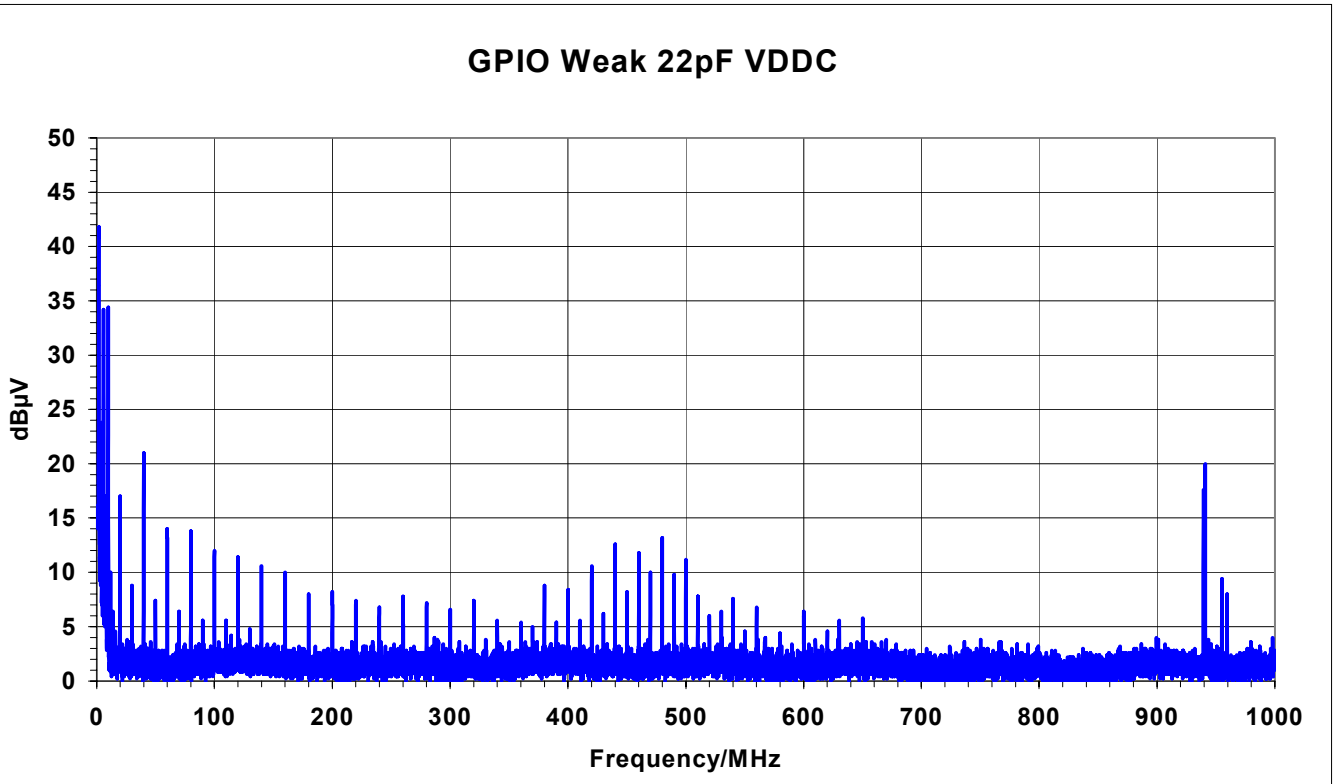


*Figure 140: GPIO „Weak“ driver at 22pF load – conducted emission on VDDC*

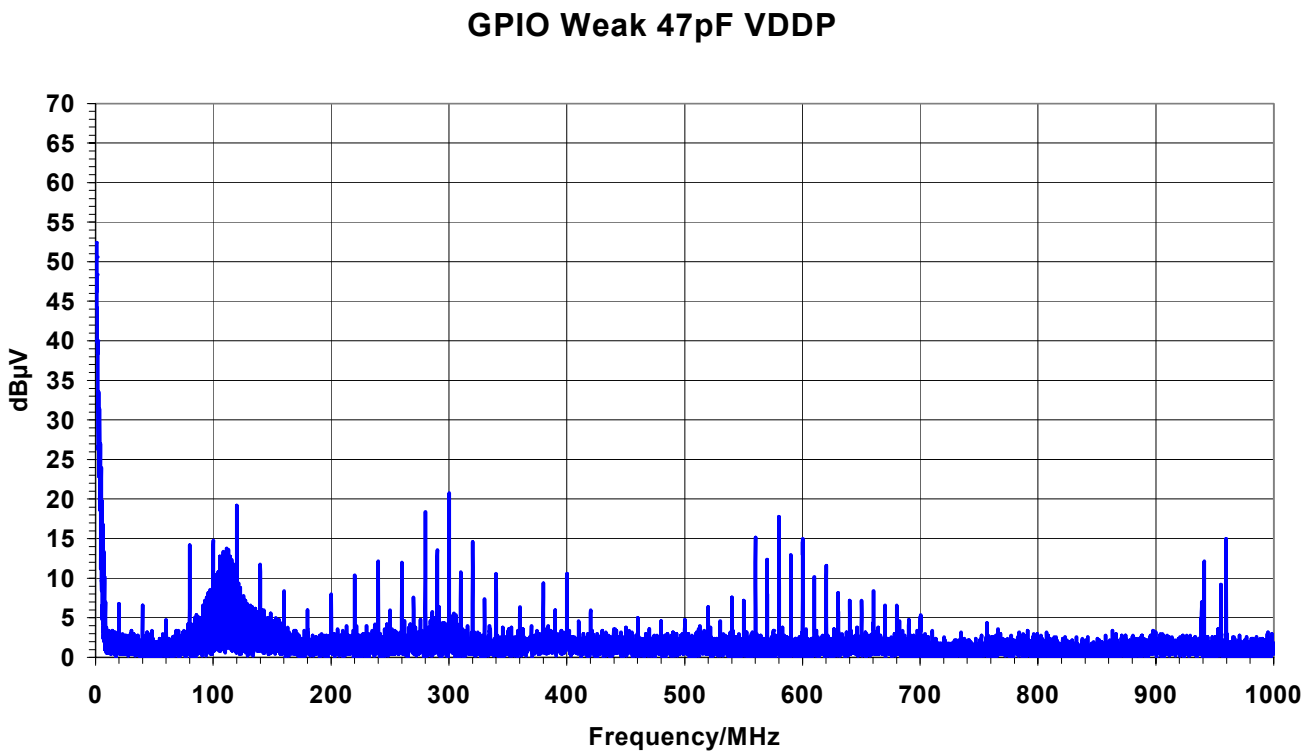


*Figure 141: GPIO „Weak“ driver at 47pF load – conducted emission on VDDP*

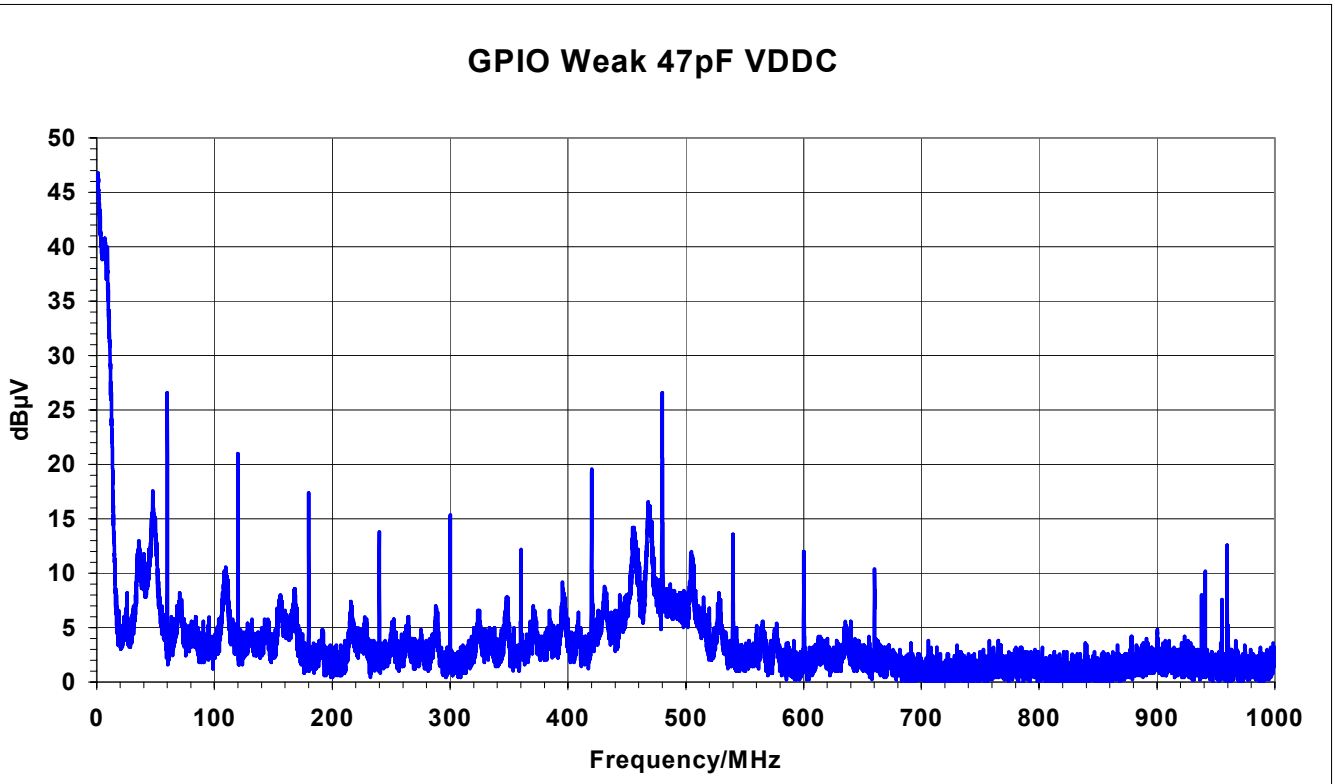


*Figure 142: GPIO „Weak“ driver at 47pF load – conducted emission on VDDC*

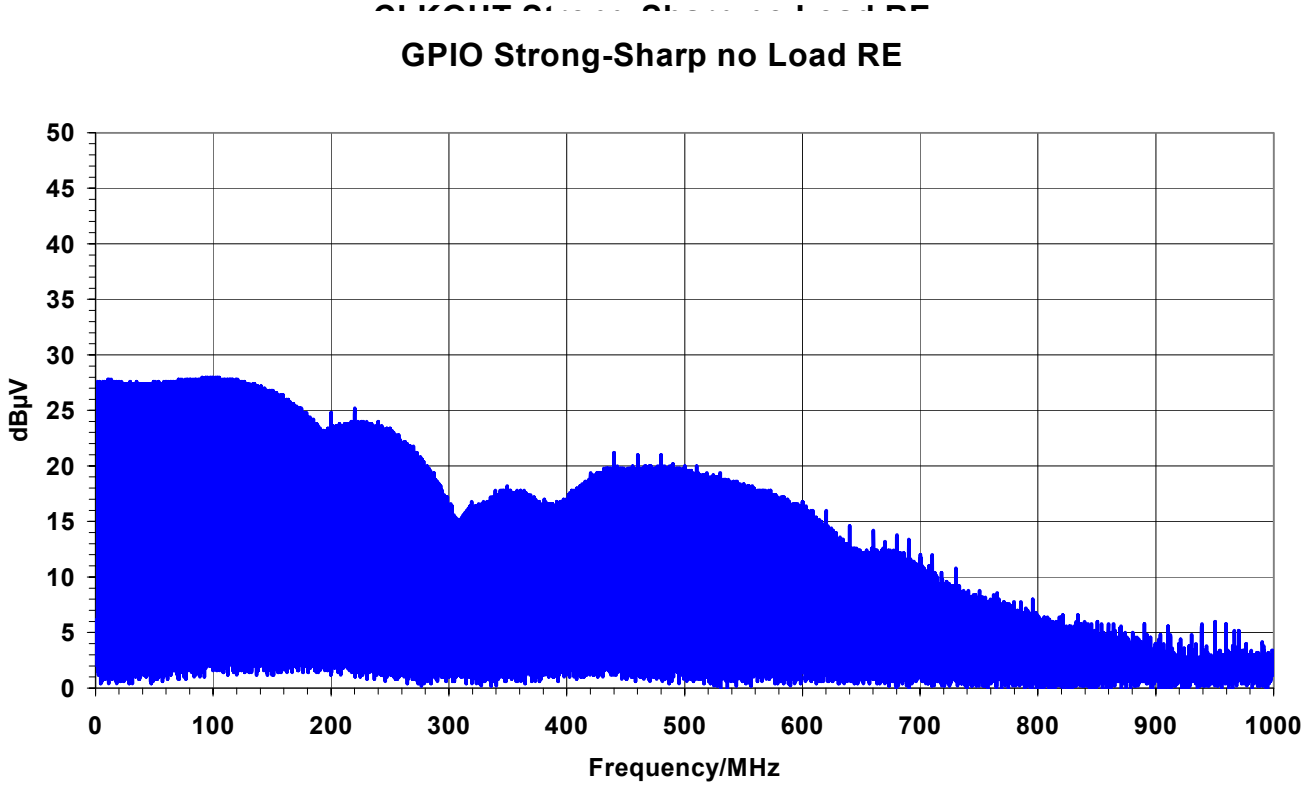


Figure 145: GPIO „Strong-Sharp“ driver at 0pF load – radiated emission

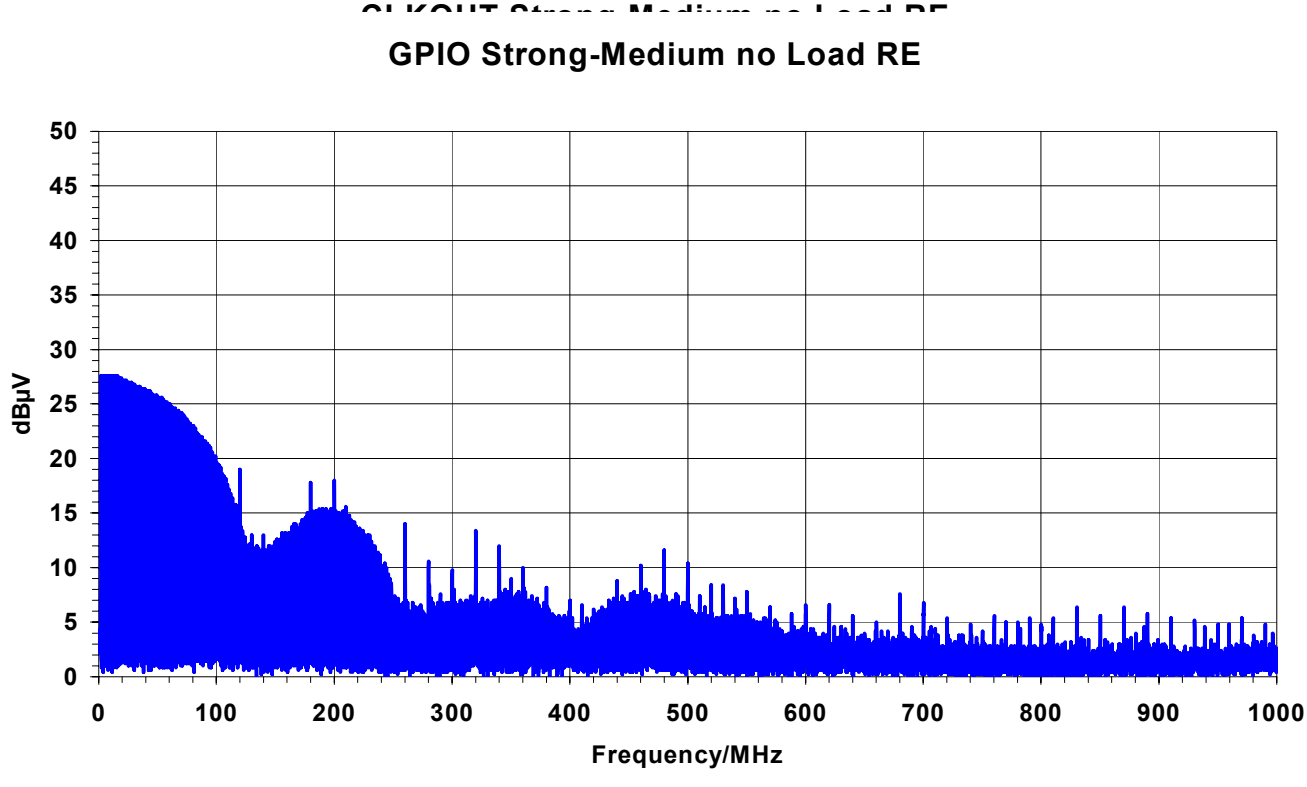


Figure 146: GPIO „Strong-Medium“ driver at 0pF load – radiated emission

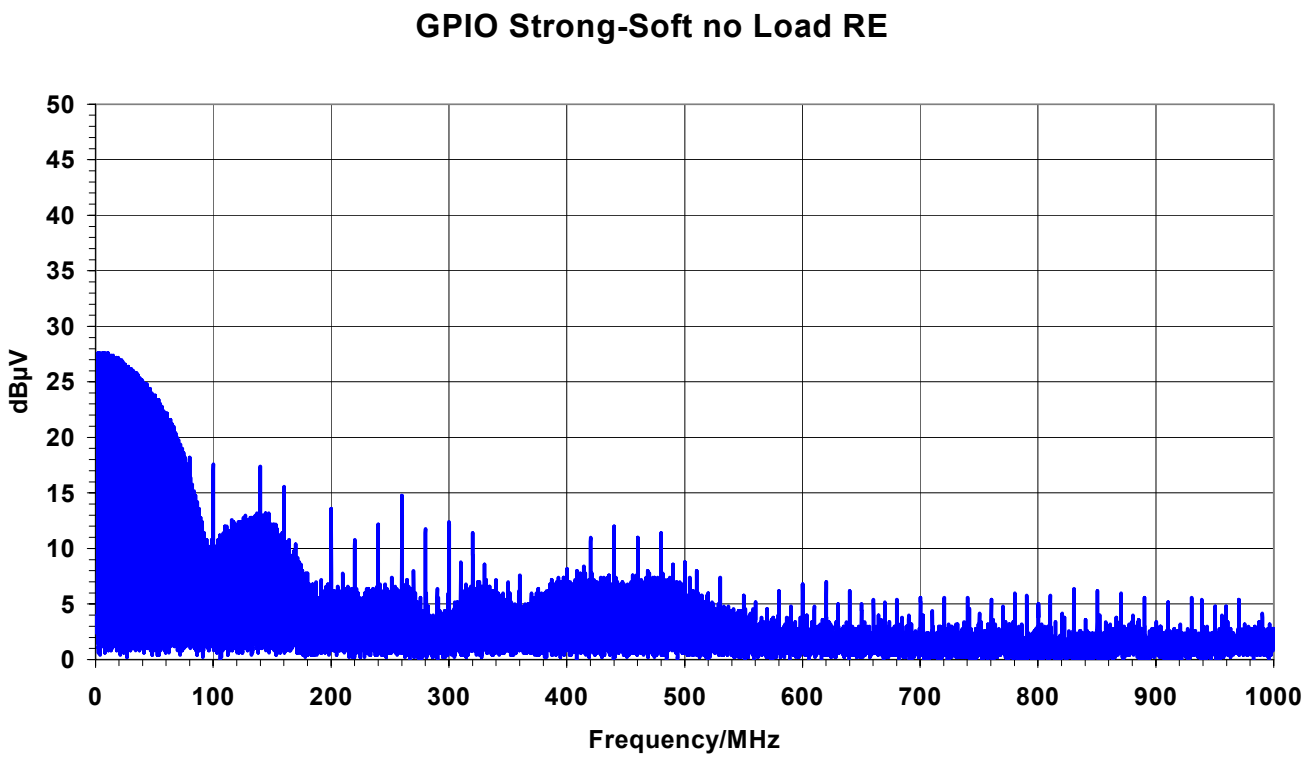


*Figure 147: GPIO „Strong-Soft“ driver at 0pF load – radiated emission*

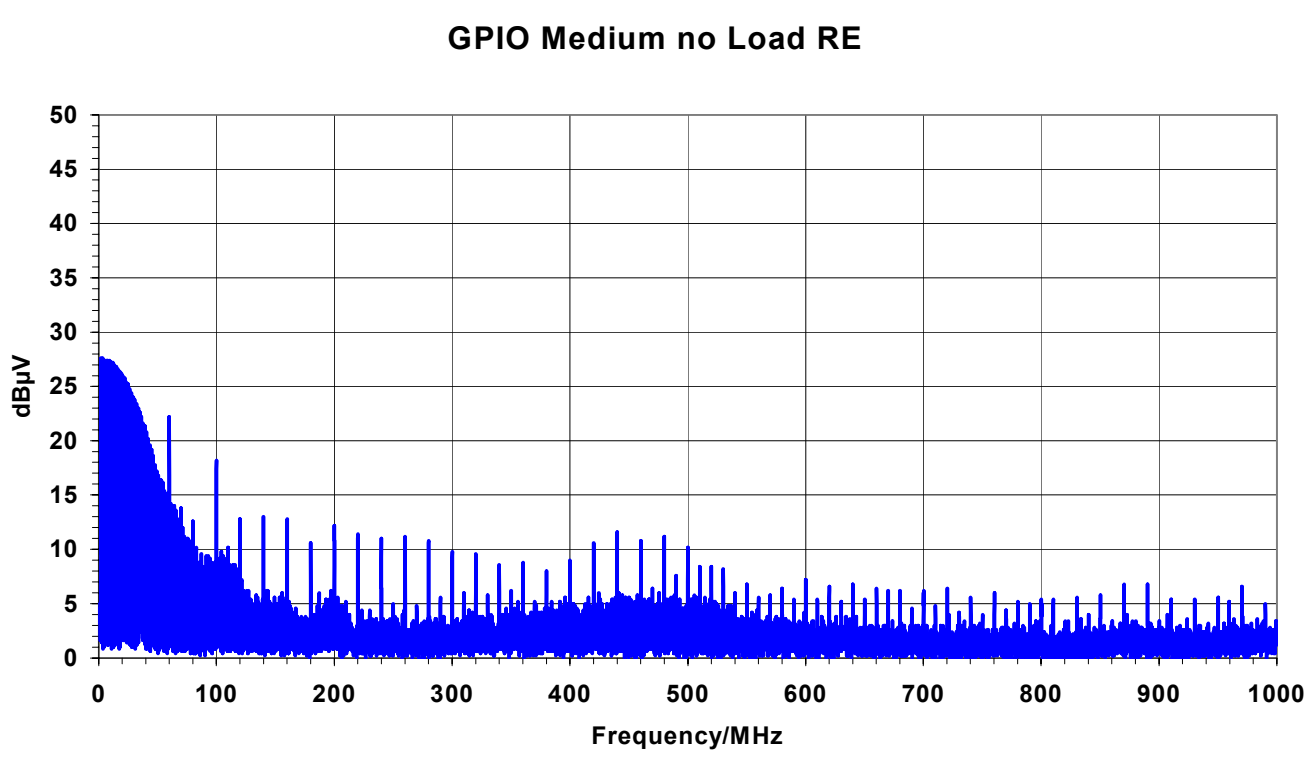


*Figure 148: GPIO „Medium“ driver at 0pF load – radiated emission*

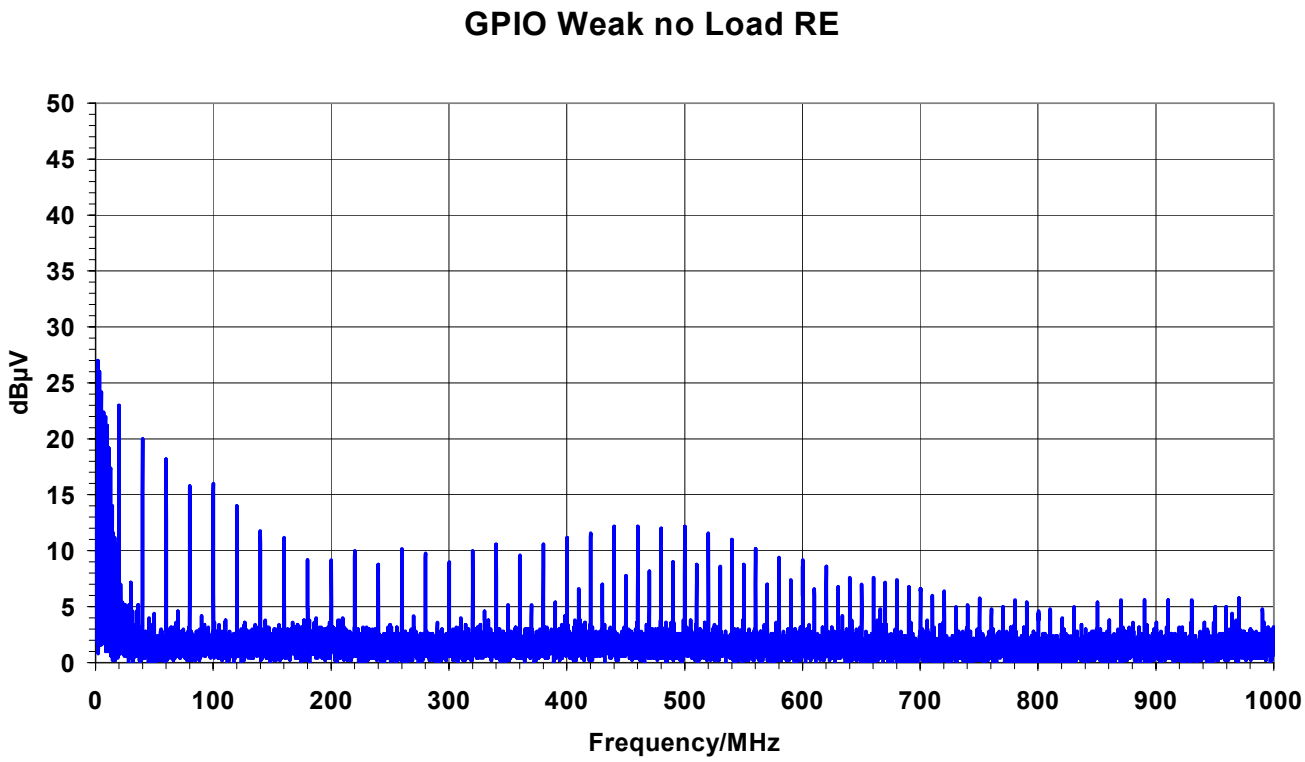


*Figure 149: GPIO „Weak“ driver at 0pF load – radiated emission*

# 6 Result discussion

The emission results presented in chapter 5 need a closer discussion regarding the impact of pad driver scaling and connected capacitive loads on the peak emission levels.

This discussion is based on selected comparison data extracted from the emission tests.

## 6.1 CLKOUT driver, conducted emission

CLKOUT uses a stronger driver than all other GPIOs. Its purpose is the distribution of the system clock either original or divided. In the presented measurements, CLKOUT was operated at 40MHz, which is equal to the system frequency. To maintain good signal integrity, no driver setting less than strong-medium must be selected.

Fig. 150 compares the emissions coupled onto VDDC for strong-medium and strong-sharp settings for CLKOUT while driving different load capacitors of 0pF (i.e. no load), 10pF, 22pF, 33pF and 47pF. No additional probe capacitance was connected to the CLKOUT pin.

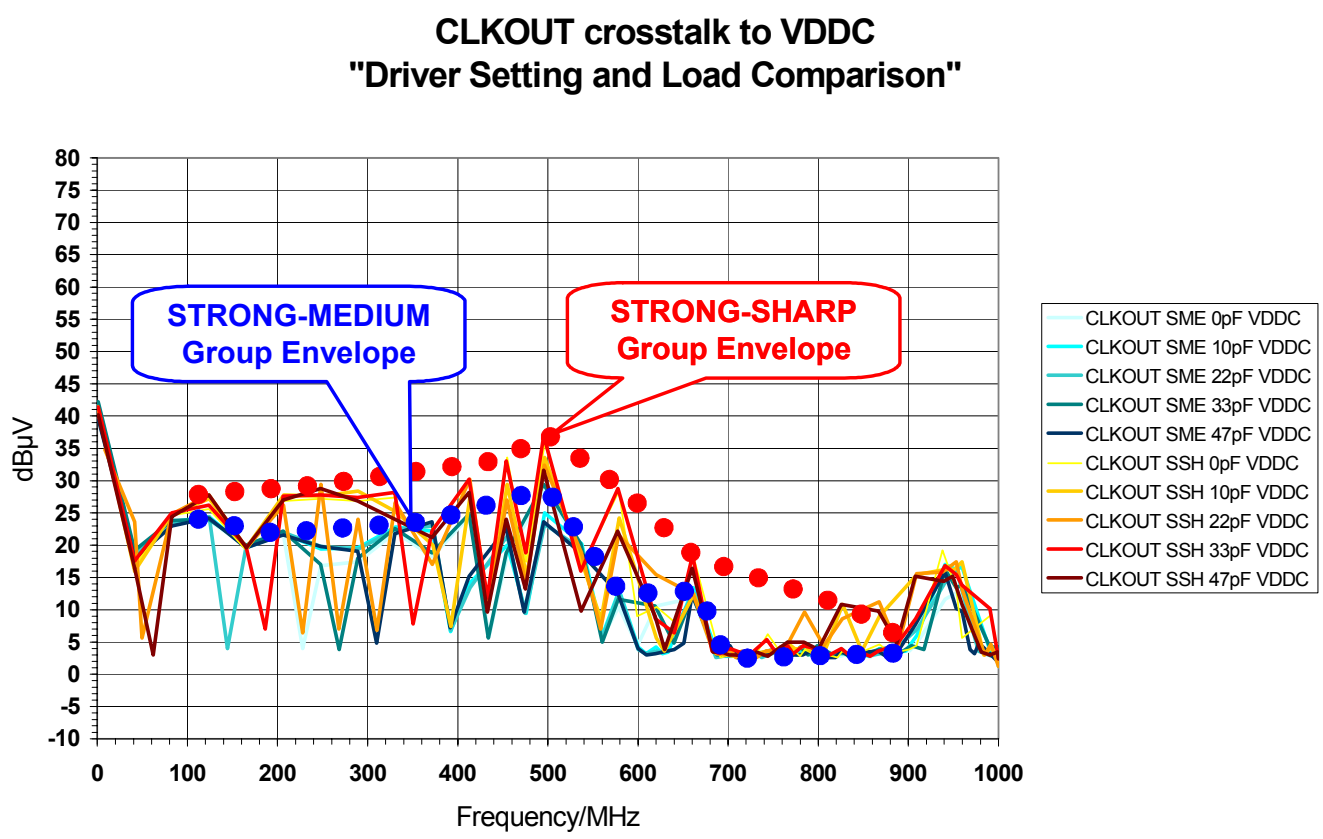


*Figure 150: CLKOUT „Strong-Sharp“ and “strong-soft” driver at various loads – conducted emission on VDDC*

Using strong-medium instead of strong-sof driver setting for CLKOUT reduces the resulting emission on VDDC up to 10dB.

Fig. 151 compares the emissions coupled onto VDDP for strong-medium and strong-sharp settings for CLKOUT while driving different load capacitors of 0pF (i.e. no load), 10pF, 22pF, 33pF and 47pF. No additional probe capacitance was connected to the CLKOUT pin.

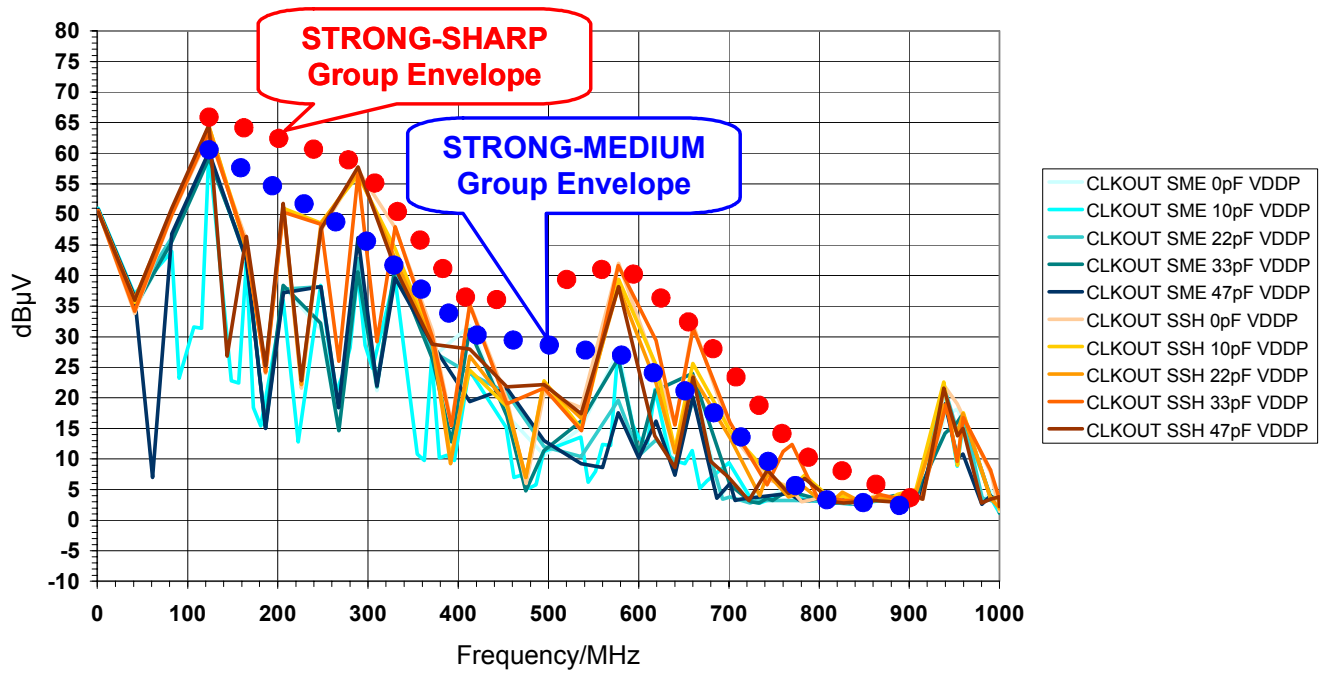


*Figure 151: CLKOUT „Strong-Sharp“ and “strong-soft” driver at various loads – conducted emission on VDDP*

Using strong-medium instead of strong-sof driver setting for CLKOUT reduces the resulting emission on VDDP up to 15dB.

## 6.2 GPIO drivers, conducted emission

GPIOs drive special peripheral functions up to a few MHz, but in real applications their data rates stay mostly in the range of 10kHz up to some 100kHz. During our emission measurement, the port switching was controlled by software. The resulting toggle rate was ca. 700kHz.

On VDDC, the crosstalk noise is mainly determined by the system clock and its derivatives. These clocks determine the synchronous switching of internal logic gates. Thus the emission observed on VDDC is mainly caused by the internal switching activity.

Fig. 152 compares the emission on VDDC for all possible driver settings at 22pF.

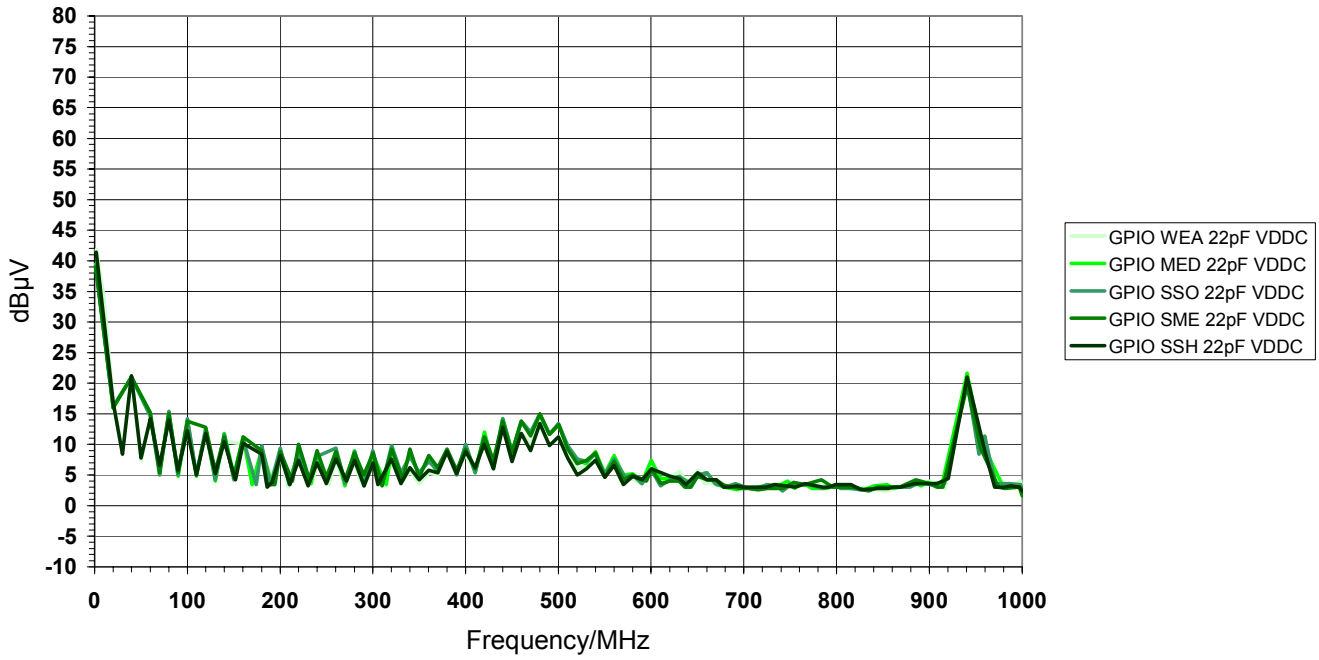


*Figure 152: GPIO various driver settings at 22pF load – conducted emission on VDDC*

From this result we see that the emission on VDDC is not influenced by the driver settings.

On VDDP, the crosstalk noise might be determined by the switching ports activity. This is because all pad drivers are connected to VDDP.

Fig. 153 compares the emission on VDDP for all possible driver settings at no external load.

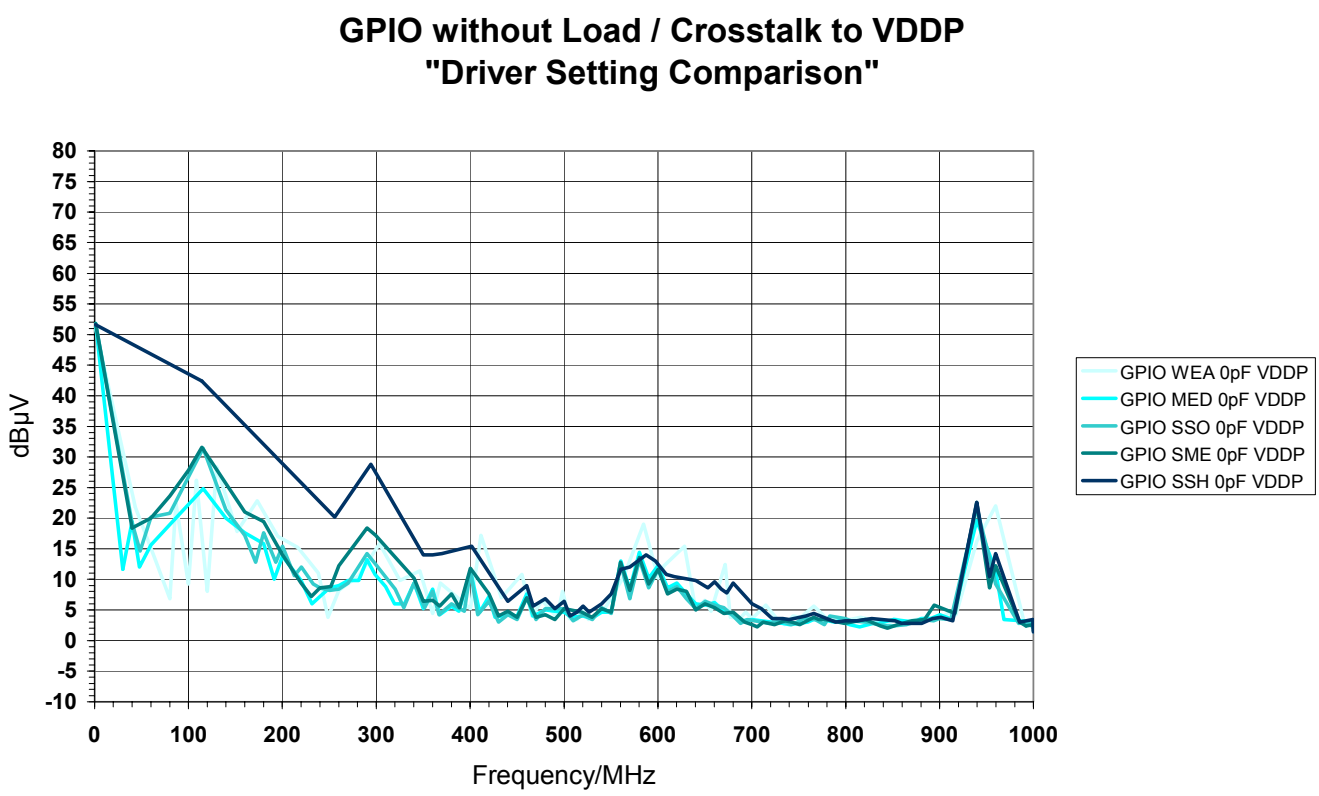


*Figure 153: GPIO various driver settings at no load – conducted emission on VDDP*

The emission amplitudes are mainly determined by the switching ports activity if any strong driver setting is used. For weak and medium driver settings the port emission stays below the system clock emission and is not visible in the envelope curves.

Fig. 154 compares the emission on VDDP for all possible driver settings at 22pF load.

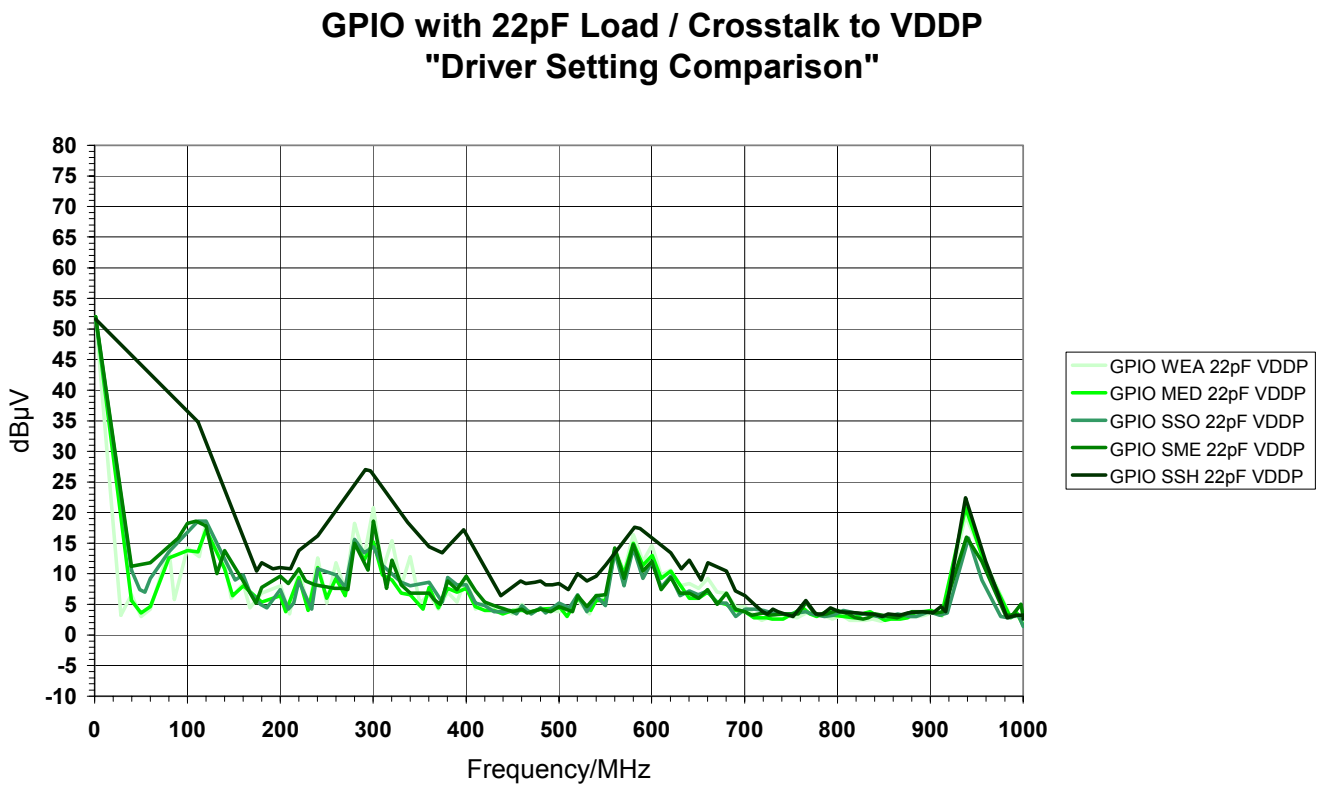


*Figure 154: GPIO various driver settings at 22pF load – conducted emission on VDDP*

Again the emission amplitudes are mainly determined by the switching ports activity if any strong driver setting is used. For weak and medium driver settings the port emission stays below the system clock emission and is not visible in the envelope curves.

Fig. 155 compares the emission on VDDP for all possible driver settings at 47pF load.

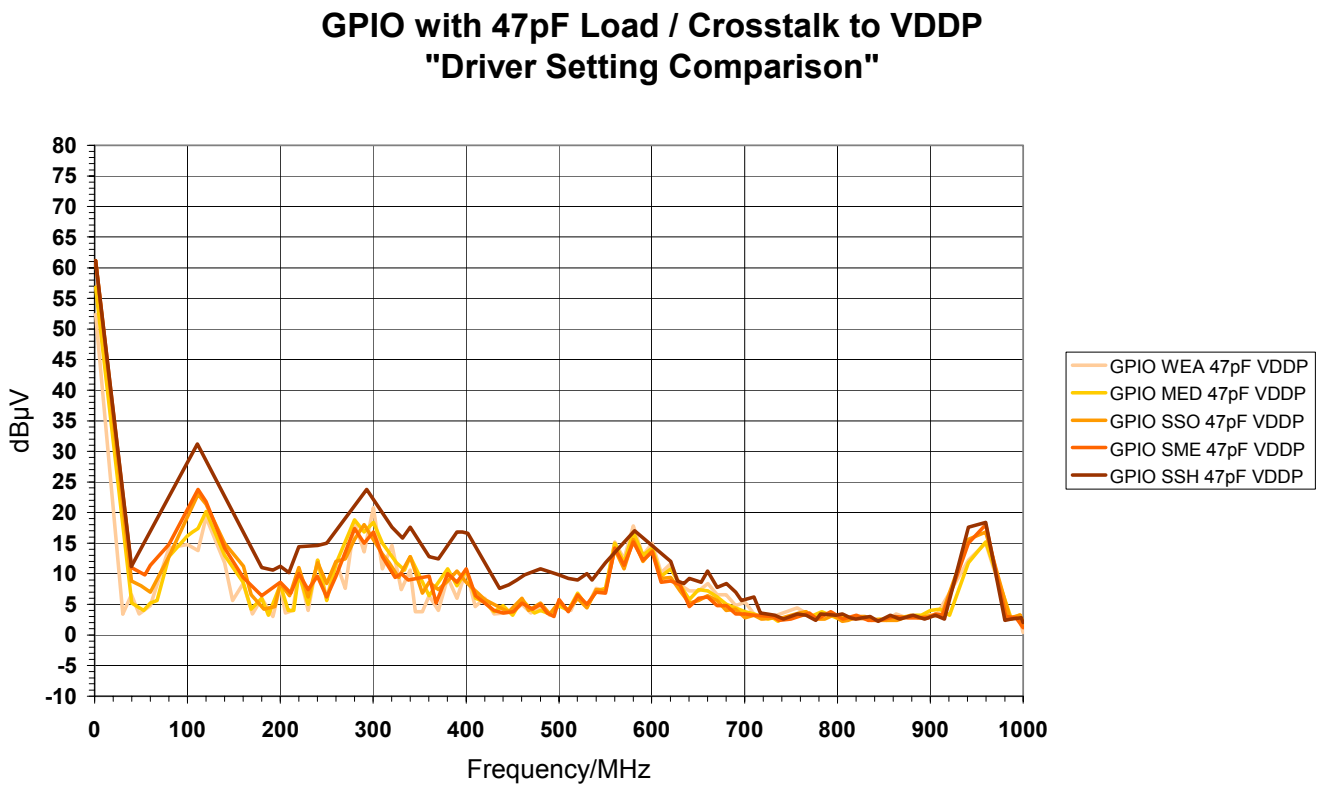


*Figure 155: GPIO various driver settings at 47pF load – conducted emission on VDDP*

Again the emission amplitudes are mainly determined by the switching ports activity if any strong driver setting is used. For weak and medium driver settings the port emission stays below the system clock emission and is not visible in the envelope curves.

However, for big external loads like the 47pF we used for comparison, the emission reduction when changing from strong-sharp to strong-medium or lower is not so efficient as for smaller loads like 22pF or smaller.

Fig. 156 compares the emission on VDDP in case of no load, 22pF load and 47pF load at “weak” driver setting.

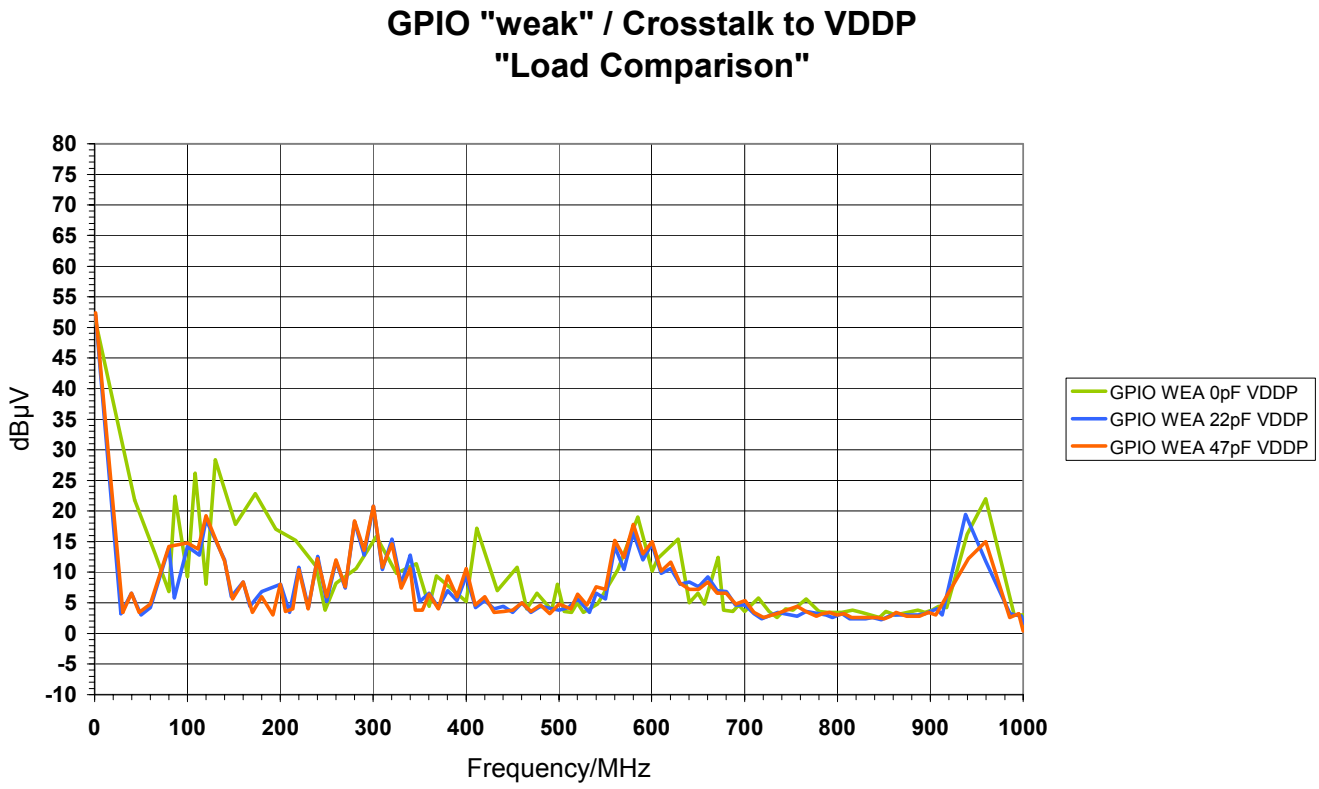


*Figure 156: GPIO “weak” driver settings at various loads – conducted emission on VDDP*

Emissions in the higher frequency range are comparable. At low frequencies, the minimum load causes maximum emission. This is due to the higher di/dt when charging/discharging of the load starts. Please refer to chapter 2.1.3 for a physical explanation.

Fig. 157 compares the emission on VDDP in case of no load, 22pF load and 47pF load at “medium” driver setting.

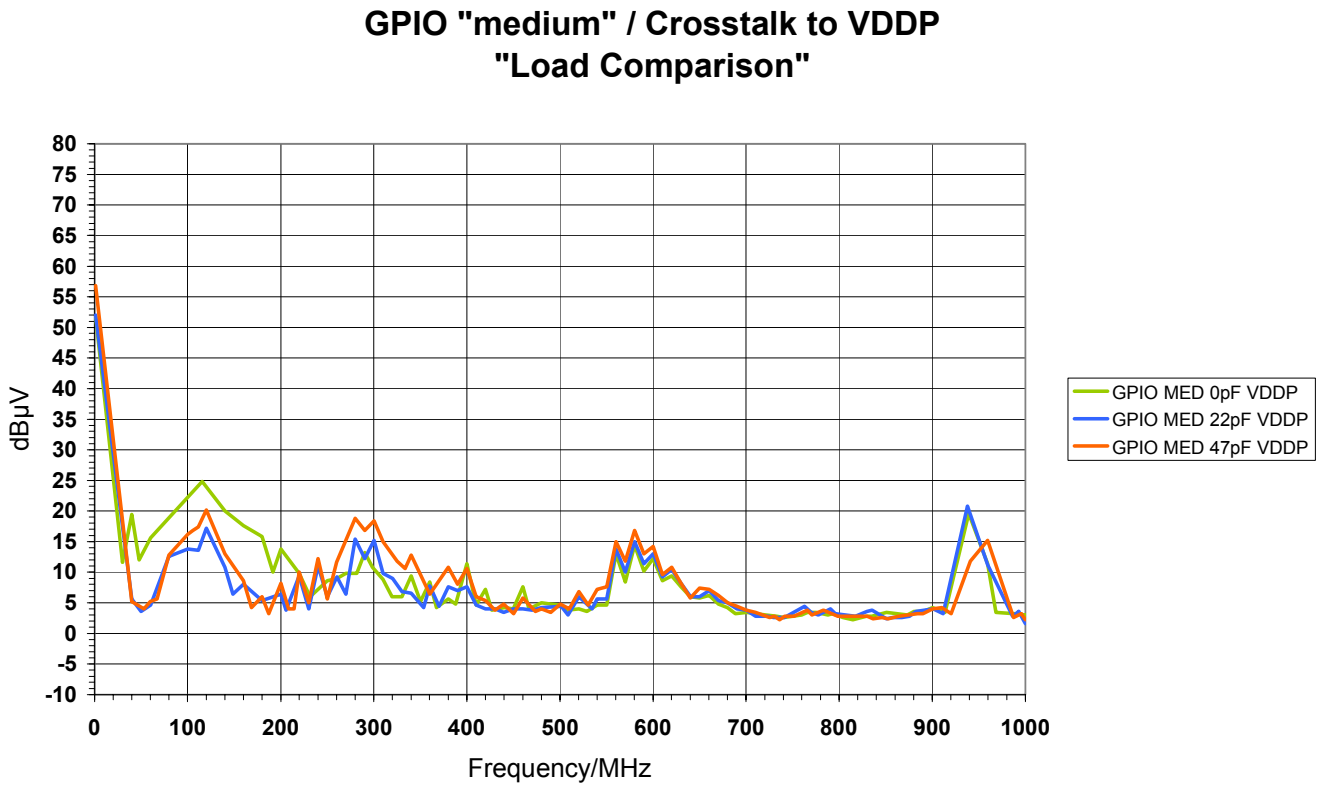


*Figure 157: GPIO “medium” driver settings at various loads – conducted emission on VDDP*

Emissions in the higher frequency range are comparable. At low frequencies, the minimum load causes maximum emission. This is due to the higher di/dt when charging/discharging of the load starts. Please refer to chapter 2.1.3 for a physical explanation.

Fig. 158 compares the emission on VDDP in case of no load, 22pF load and 47pF load at “strong-soft” driver setting.

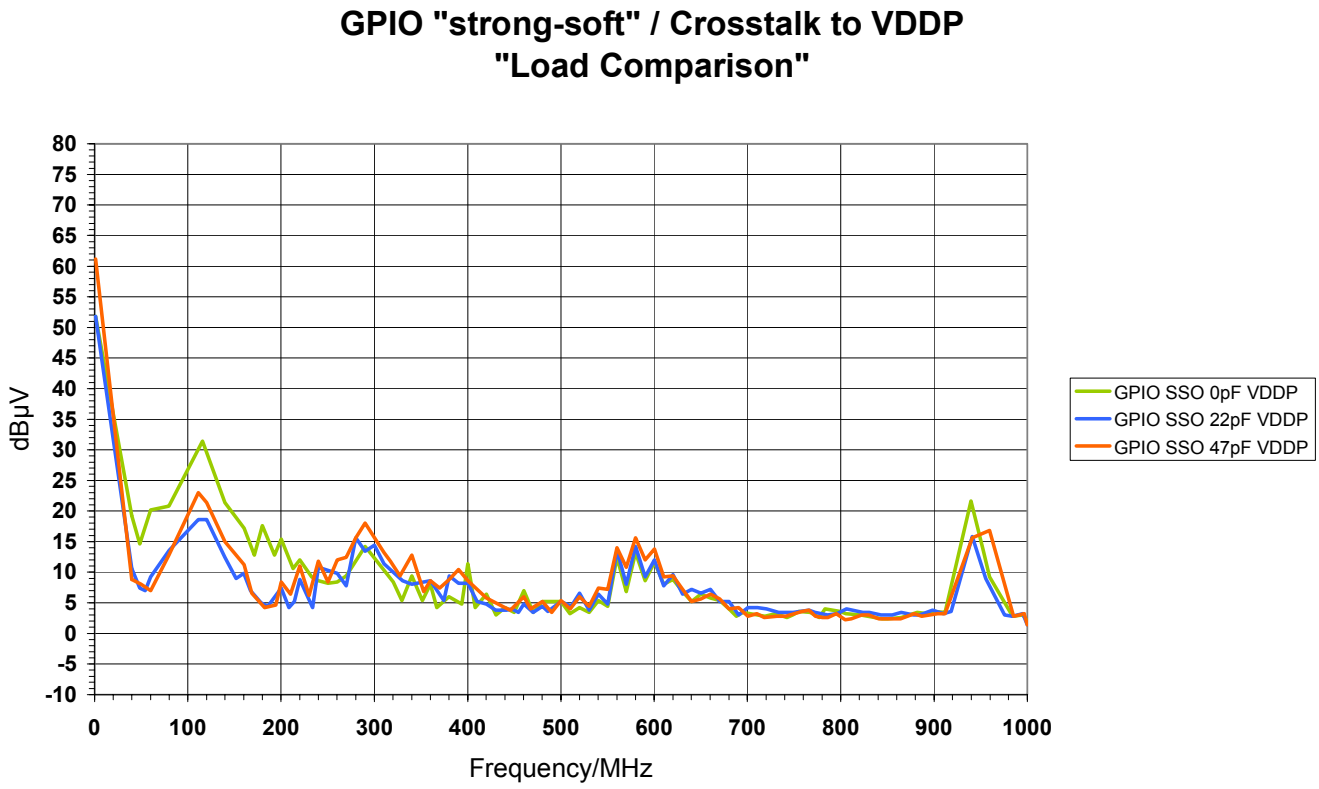


*Figure 158: GPIO “strong-soft” driver settings at various loads – conducted emission on VDDP*

Emissions in the higher frequency range are comparable. At low frequencies, the minimum load causes maximum emission. This is due to the higher di/dt when charging/discharging of the load starts. Please refer to chapter 2.1.3 for a physical explanation.

Fig. 159 compares the emission on VDDP in case of no load, 22pF load and 47pF load at “strong-medium” driver setting.

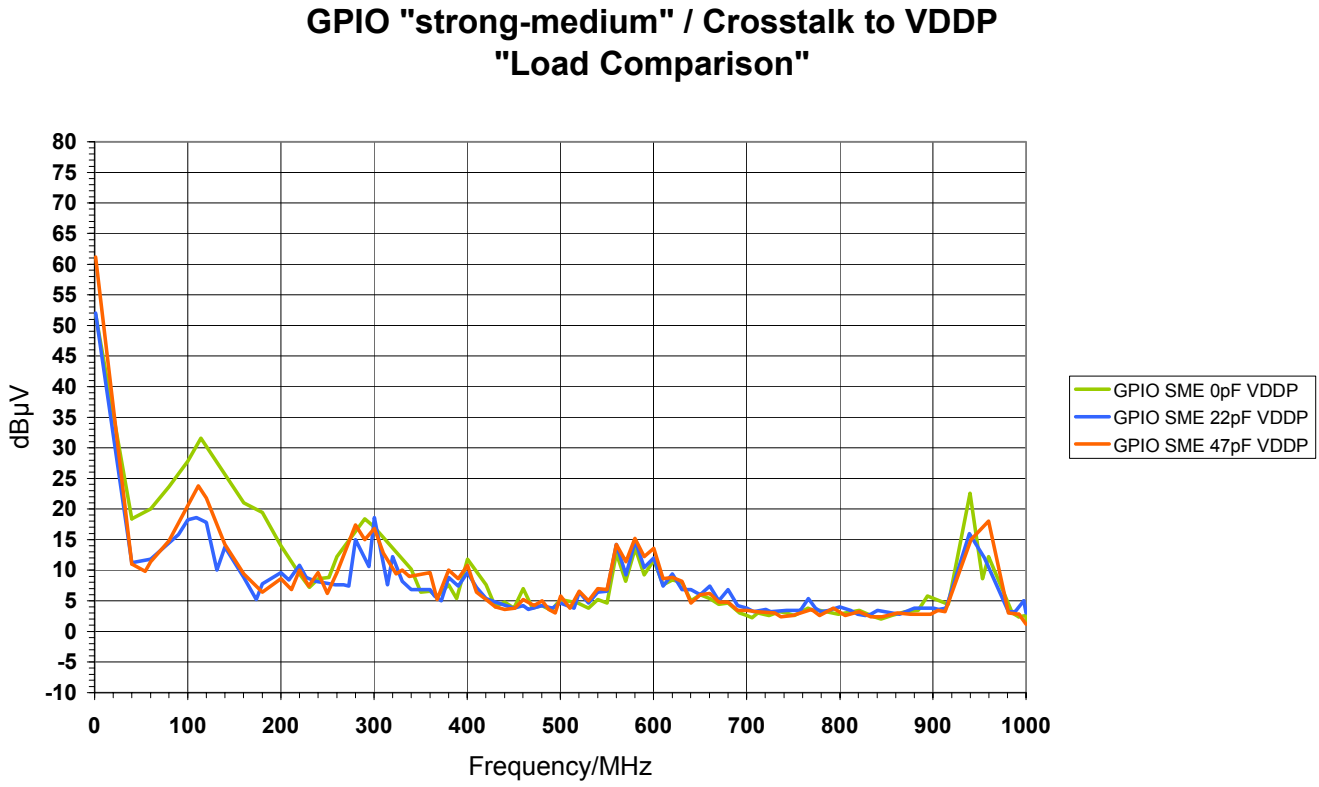


*Figure 159: GPIO “strong-medium” driver settings at various loads – conducted emission on VDDP*

Emissions in the higher frequency range are comparable. At low frequencies, the minimum load causes maximum emission. This is due to the higher di/dt when charging/discharging of the load starts. Please refer to chapter 2.1.3 for a physical explanation.

Fig. 160 compares the emission on VDDP in case of no load, 22pF load and 47pF load at “strong-sharp” driver setting.

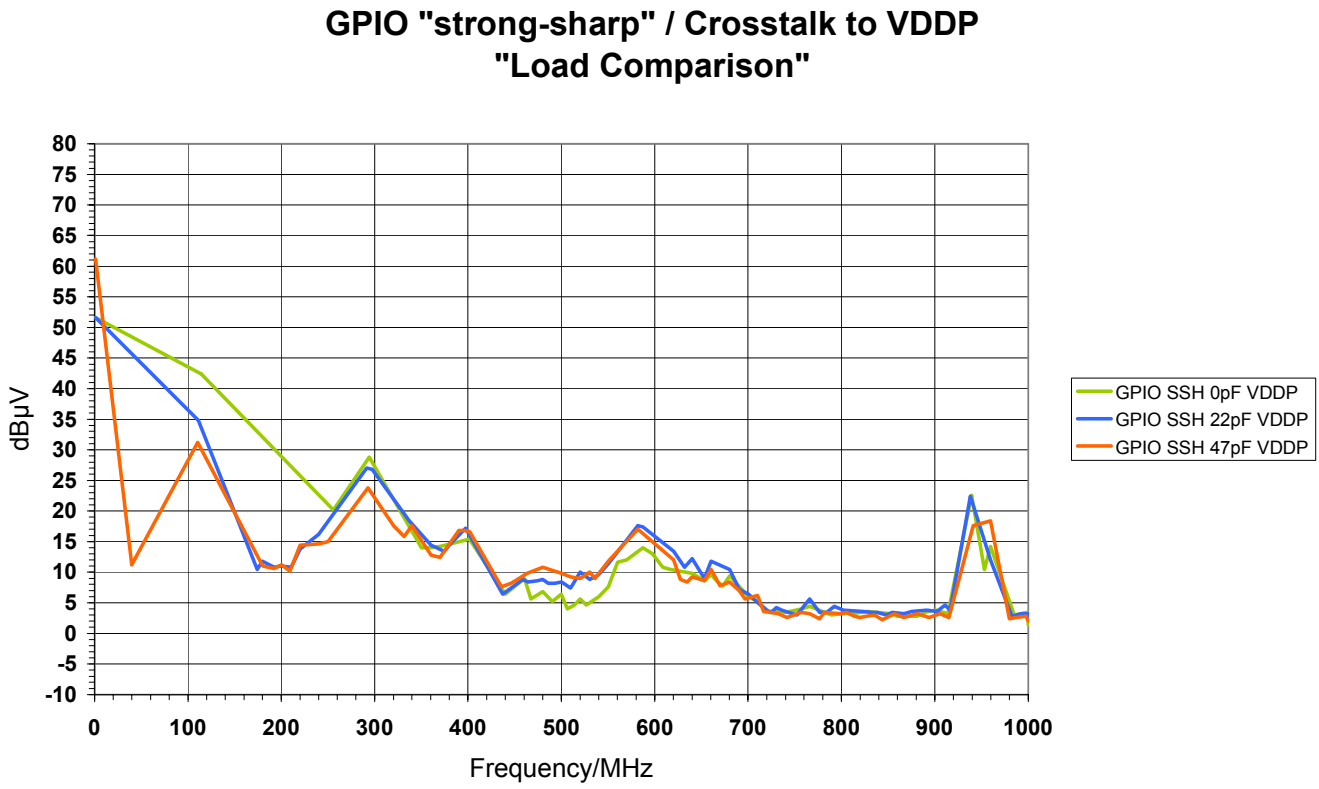


*Figure 160: GPIO “strong-sharp” driver settings at various loads – conducted emission on VDDP*

Emissions in the higher frequency range are comparable. At low frequencies, the minimum load causes maximum emission. This is due to the higher di/dt when charging/discharging of the load starts. Please refer to chapter 2.1.3 for a physical explanation.

## 6.3 Radiated emission

Above 100MHz, using “strong-medium” instead of “strong-sharp” driver for the CLKOUT pin leads to a radiated emission reduction between 6dB and 10dB. Fig. 161 shows the corresponding envelope curves.

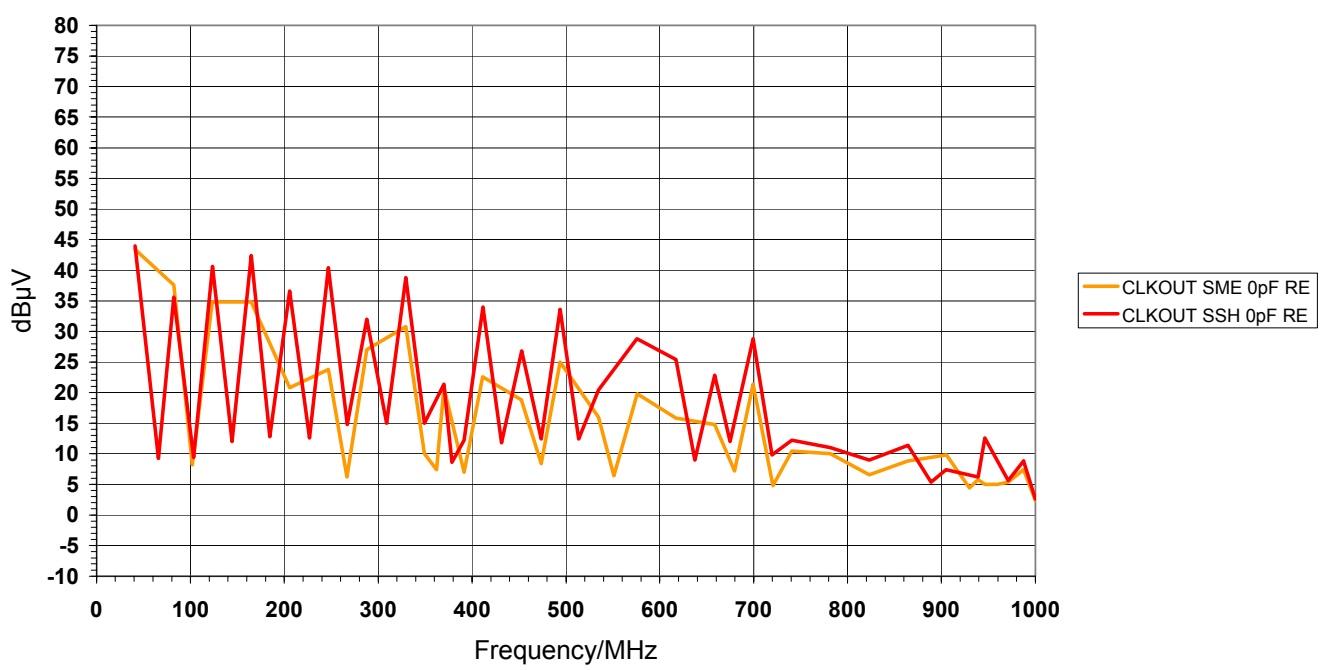


*Figure 161: CLKOUT toggling at 40MHz; various driver settings at no load – radiated emission*

Similar differences appear for bigger capacitive loads. Radiated emission stays ca. 15-20dB below conducted emission observed at VDDP. Please compare with Fig. 151.

If set to “strong-sharp”, the radiated emission of 16 toggling GPIO pins (toggle rate ca. 700kHz) stays more than 15dB below the radiated emission of the 40MHz CLKOUT pin. Weaker driver settings (“strong-medium” and below) reduce radiated emission ca. 10dB further. Fig. 162 shows the corresponding envelope curves.

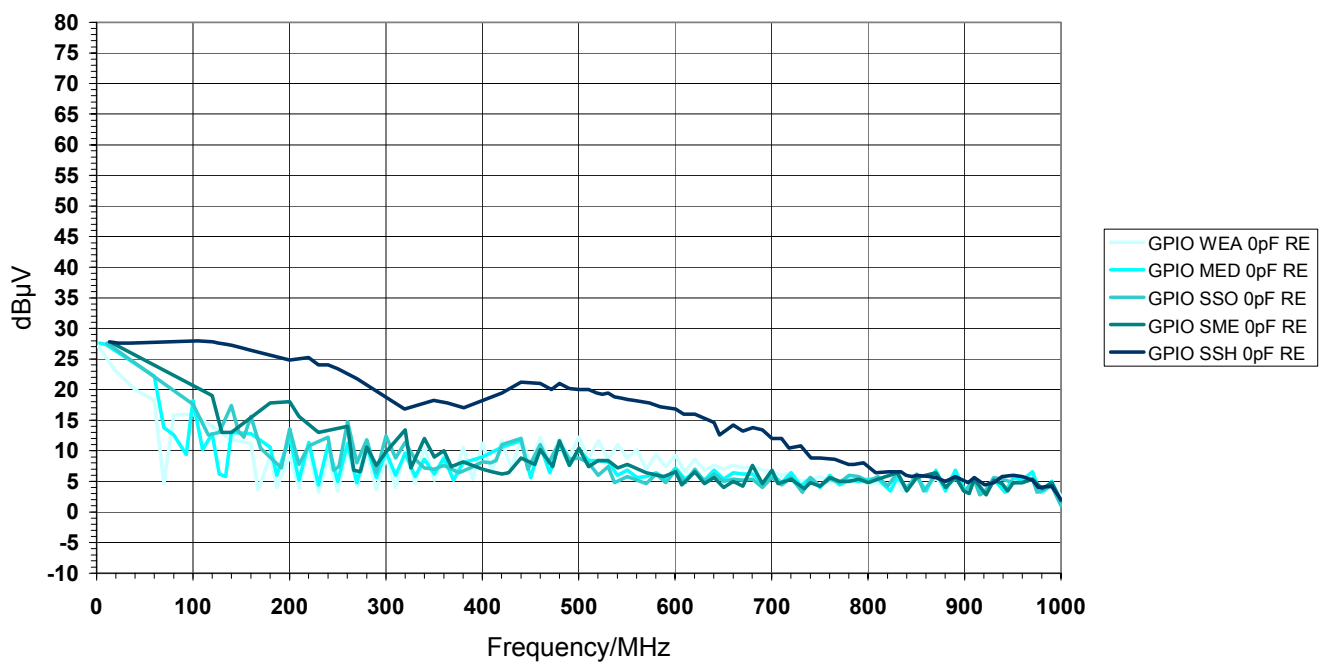


*Figure 162: GPIOs toggling at ca. 700kHz; various driver settings at no load – radiated emission*

Similar differences appear for bigger capacitive loads. Radiated emission stays ca. 10-15dB below conducted emission observed at VDDP. Please compare with Fig. 153.

Whenever using driver settings less than “strong-sharp”, the radiated emission caused by the drivers should not cause any problems and are neglegible against the CLKOUT emission.

# 7 Recommended Settings for Signal Categories

## 7.1 General

In the previous chapters, many detailed data was provided for the impact of driver settings and load capacitance on the resulting rise and fall times as well as on conducted and radiated emission.

Generally, the required signal integrity determines the selection of driver strength and slew rate for a given toggle rate and capacitive load. However, due to the simultaneous impact on electromagnetic emission, the weakest possible driver setting which still meets the signal integrity should be chosen.

To decide for the proper pad driver settings for a signal, its electrical characteristics should be considered. This leads to the definition of signal categories by means of clock or data transfer (AC view) or current driving capability (DC view). According to these views, any signal can be classified as shown in Table 5.

| Signal category | Clock rate | Capacitive load | DC driving capability |
|---|---|---|---|
| System clock | 20 … 40 MHz | 10 … 50 pF | n/a |
| High-speed data line | 5 … 20 MHz | 10 … 50 pF | n/a |
| Low-speed data line | 0.5 … 5 MHz | 10 … 50 pF | n/a |
| Low-speed control line | <1 MHz | <20 pF | n/a |
| High-current control line | n/a | n/a | 10 … 30 mA |
| Medium-current control line | n/a | n/a | 1 … 10 mA |
| Low-current control line | n/a | n/a | <1 mA |

Table 5: Signal categories

The following settings for pad output drivers are available, see also Table 6:

- strong driver / sharp edge (setting 1)
- strong driver / medium edge (setting 2)
- strong driver / soft edge (setting 3)
- medium driver / no edge configuration available (setting 4)
- weak driver / no edge configuration available (setting 5)

| Setting number | Driver configuration | Edge configuration | Signal category | Capacitive Load | DC Current [1)] |
|---|---|---|---|---|---|
| 1 | STRONG | SHARP | System clock | High | 2.5 / 10 mA |
| 2 | STRONG | MEDIUM | System clock<br>High-speed data lines | Low<br>High | |
| 3 | STRONG | SOFT | High-speed data lines<br>High-current control lines | Low<br>All | |
| 4 | MEDIUM | none | Low-speed data lines<br>Medium-current control lines | All<br>All | |
| 5 | WEAK | none | Very low-speed control lines<br>Low-current control line | All<br>All | |

Table 6: Recommended Output Driver Settings

Note 1): Two values are given for the DC current of GPIO pins in the format “nominal / max mA”. The “max mA” value can only be drawn from a pin if maximal 2 other pins in the same 16-bit port group are also driving this maximum current. This restriction is due to danger of electromigration damage.

The following parameters determine the final selection of driver settings:

- signal performance category (AC and DC)
- maximum temperature
- maximum acceptable electromagnetic emission

## 7.2 Decision Tables and Graphs

Following the recommendations given above, the driver setting selection should be based on (1) proper signal integrity and (2) minimal electromagnetic emission. Since electromagnetic emission increases with stronger driver settings, the weakest driver and slew rate settings should be selected that are able to force the rise/fall times required for the desired signal integrity.

This chapter offers decision numbers in table and graphical format for proper driver settings at maximum clock or data rates expected to be driven. The rise/fall times occupy 1/6th of the clock period each, see Fig. 163 on top. Alternatively, the rise/fall times occupy 1/4th of the clock period each, see Fig. 163 on bottom.

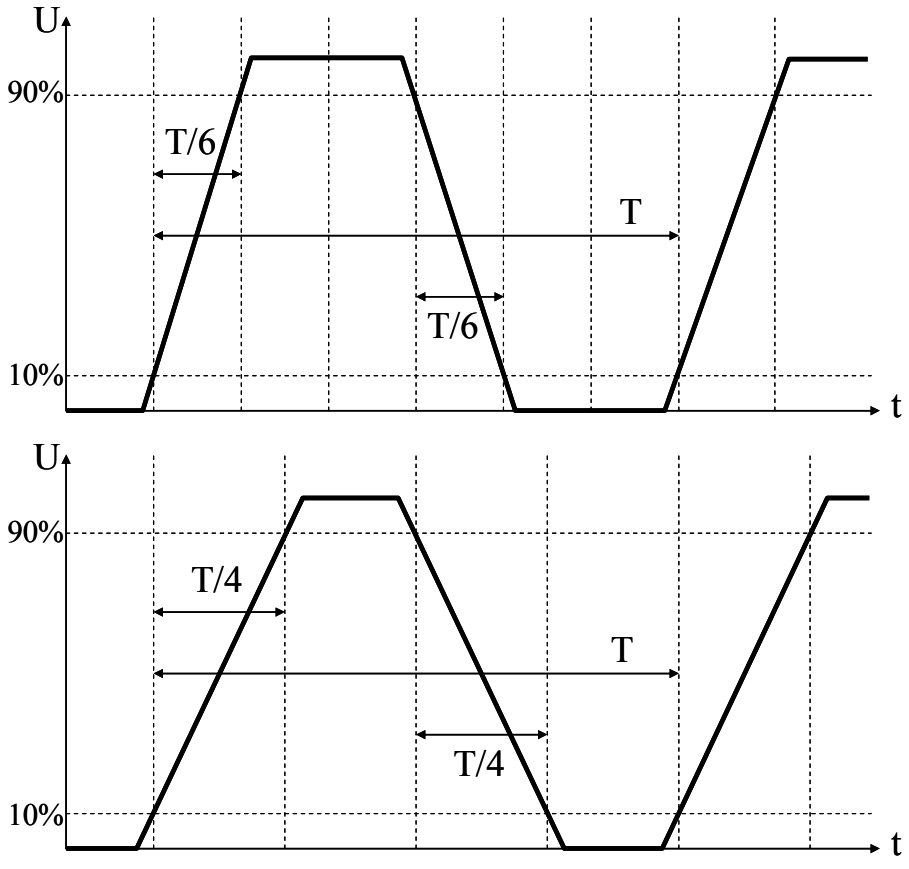


*Figure 163: Assumed rise/fall timing conditions related to signal period*

Please note that all values given in this chapter are proposals for system application designers using Infineon microcontrollers in 0.25µm CMOS technology. They are based on timing measurements performed on center lot devices. Thus all values are subject to approx. 10% offset depending on fabrication process variation. Additionally, pad supply voltages different from nominal conditions impact the resulting timing. The finally selected driver setting should include this offset. It has to be added to all numbers given in the tables and graphs.

Fig. 164 shows an example of a decision graph.

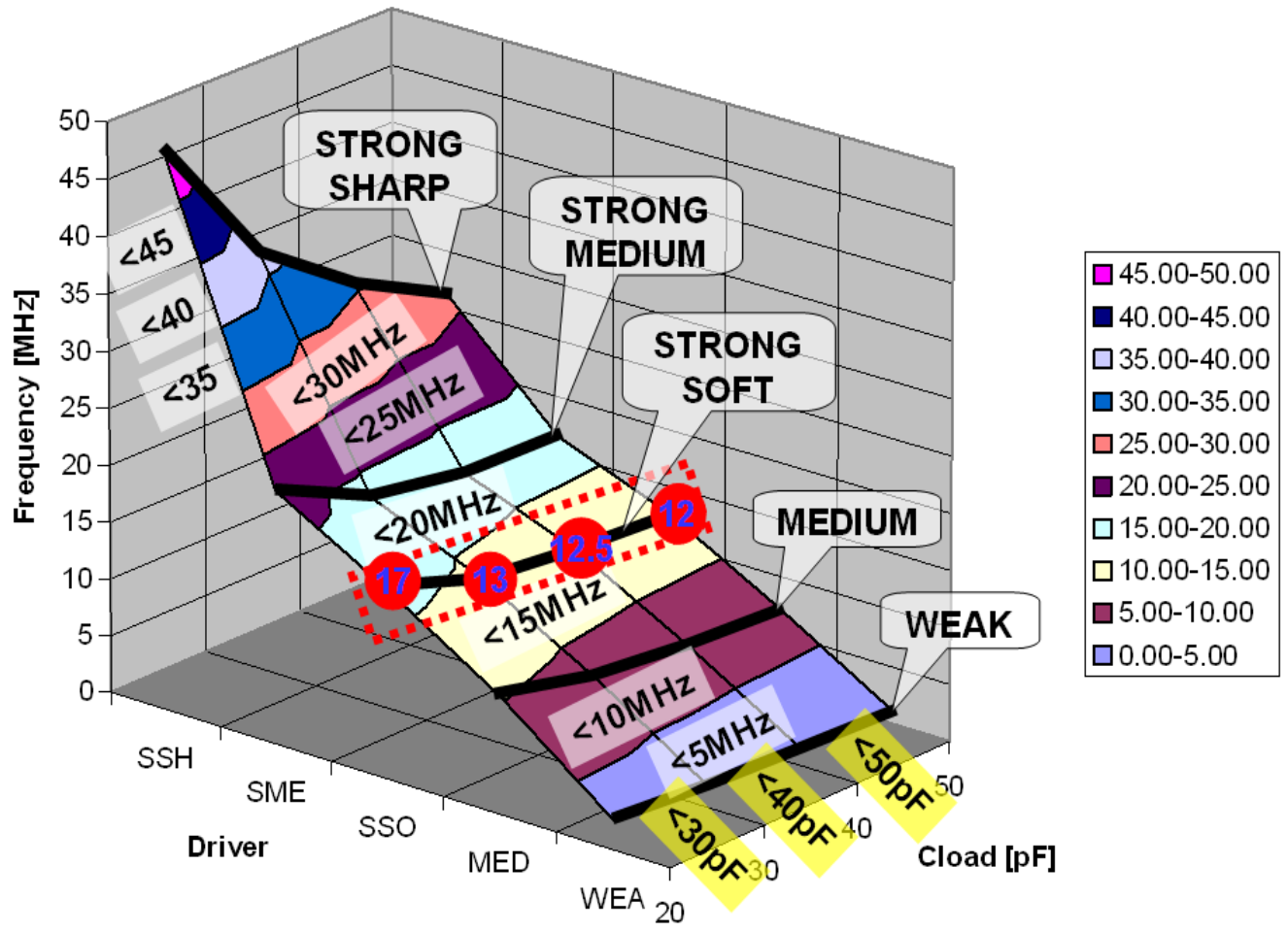


*Figure 164: Assumed rise/fall timing conditions related to signal period*

The clock/data rate is given in [MHz] for capacitive loads of 20, 30, 40, 50 pF and driver selections of weak, medium, strong soft/medium/sharp. In Fig. 164, the resulting maximum data rates are marked with red circles as 17 MHz at 20 pF load, 13 MHz at 30 pF load, 12.5 MHz at 40 pF load, and 12 MHz at 50 pF load. If a pin is intended to toggle a 35 pF load at 15 MHz, the strong-soft setting is not sufficient. Instead strong-medium must be selected. Strong-sharp is, of course, also capable of driving a 35 pF load at 15 MHz, but should be avoided due to unnecessary high electromagnetic emission.

The rise/fall times occupy 1/6th of the clock period each, see Fig. 163 on top. This relation should be acceptable for most interface signals and protocols.

Tables 7 and 8 give an overview of the maximal toggle rates in [MHz] for all driver settings (WEA=weak, MED=medium, SSO=strong-soft, SME=strong-medium, SSH=strong-sharp) connected to capacitive loads of 20, 30, 40, and 50 pF. Each ambient temperature is marked by its own color. According to the microcontroller specification or marking, one of the following maximum temperatures should apply: 125°C, 110°C, 85°C, 70°C. The other temperatures, 25°C and -40°C, are given for reference only.

Since the CLKOUT driver is stronger than the GPIO driver, values for both driver types are provided in Tables 7 and 8. In Table 7, the rise/fall times are assumed to occupy 1/6th of the clock period, in Table 8, the rise/fall times are assumed to occupy 1/4th of the clock period.

Fig. 165-192 show the values of Tables 7 and 8 in the graphical representation explained in Fig. 164, separated by ambient temperatures and driver types. In the respective titles, “16% Edges” stands for rise/fall times occupying 1/6th of the clock period; “25% Edges” stands for rise/fall times occupying 1/4th of the clock period.

| | CLKOUT | | | | | GPIO | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **150°C** | | 20 | 30 | 40 | 50 | | 20 | 30 | 40 | 50 |
| | SSH | 49.02 | 39.22 | 33.33 | 29.66 | SSH | 30.30 | 23.81 | 18.16 | 15.72 |
| | SME | 27.78 | 23.47 | 21.65 | 20.23 | SME | 15.02 | 13.06 | 11.00 | 10.22 |
| | SSO | 11.34 | 10.10 | 9.16 | 8.96 | SSO | 10.82 | 9.36 | 7.88 | 7.58 |
| | MED | 6.83 | 5.56 | 5.05 | 4.80 | MED | 6.97 | 5.77 | 4.69 | 4.31 |
| | WEA | 1.33 | 1.03 | 0.84 | 0.68 | WEA | 1.38 | 1.04 | 0.85 | 0.68 |
| **125°C** | | 20 | 30 | 40 | 50 | | 20 | 30 | 40 | 50 |
| | SSH | 53.76 | 42.80 | 36.30 | 32.08 | SSH | 32.81 | 25.61 | 19.76 | 17.08 |
| | SME | 30.30 | 25.22 | 23.15 | 21.58 | SME | 16.06 | 13.84 | 11.89 | 11.07 |
| | SSO | 12.36 | 10.83 | 9.83 | 9.57 | SSO | 11.65 | 10.08 | 8.56 | 8.23 |
| | MED | 7.50 | 6.03 | 5.45 | 5.14 | MED | 7.45 | 6.15 | 5.08 | 4.67 |
| | WEA | 1.48 | 1.13 | 0.91 | 0.74 | WEA | 1.52 | 1.15 | 0.93 | 0.74 |
| **110°C** | | 20 | 30 | 40 | 50 | | 20 | 30 | 40 | 50 |
| | SSH | 57.08 | 45.28 | 38.34 | 33.73 | SSH | 34.52 | 26.83 | 20.86 | 18.02 |
| | SME | 32.05 | 26.40 | 24.15 | 22.48 | SME | 16.75 | 14.35 | 12.49 | 11.64 |
| | SSO | 13.07 | 11.32 | 10.28 | 9.97 | SSO | 12.19 | 10.57 | 9.03 | 8.68 |
| | MED | 7.97 | 6.36 | 5.72 | 5.37 | MED | 7.78 | 6.40 | 5.33 | 4.93 |
| | WEA | 1.59 | 1.20 | 0.96 | 0.78 | WEA | 1.62 | 1.22 | 0.98 | 0.78 |
| **85°C** | | 20 | 30 | 40 | 50 | | 20 | 30 | 40 | 50 |
| | SSH | 63.61 | 50.13 | 42.31 | 36.89 | SSH | 37.81 | 29.13 | 23.00 | 19.83 |
| | SME | 35.46 | 28.63 | 26.04 | 24.16 | SME | 18.06 | 15.30 | 13.52 | 12.74 |
| | SSO | 14.46 | 12.24 | 11.13 | 10.73 | SSO | 13.21 | 11.47 | 9.94 | 9.55 |
| | MED | 8.90 | 6.98 | 6.23 | 5.80 | MED | 8.38 | 6.87 | 5.83 | 5.41 |
| | WEA | 1.81 | 1.34 | 1.06 | 0.85 | WEA | 1.82 | 1.37 | 1.09 | 0.87 |
| **70°C** | | 20 | 30 | 40 | 50 | | 20 | 30 | 40 | 50 |
| | SSH | 68.31 | 53.58 | 45.11 | 39.09 | SSH | 40.10 | 30.72 | 24.51 | 21.10 |
| | SME | 37.88 | 30.16 | 27.32 | 25.30 | SME | 18.95 | 15.93 | 14.20 | 13.51 |
| | SSO | 15.44 | 12.87 | 11.71 | 11.24 | SSO | 13.91 | 12.00 | 10.57 | 10.16 |
| | MED | 9.57 | 7.42 | 6.58 | 6.10 | MED | 8.78 | 7.18 | 6.18 | 5.76 |
| | WEA | 1.97 | 1.44 | 1.12 | 0.91 | WEA | 1.97 | 1.48 | 1.17 | 0.92 |
| **25°C** | | 20 | 30 | 40 | 50 | | 20 | 30 | 40 | 50 |
| | SSH | 87.72 | 67.20 | 56.31 | 47.62 | SSH | 49.02 | 36.71 | 30.53 | 26.12 |
| | SME | 47.62 | 35.92 | 32.05 | 29.45 | SME | 22.22 | 18.18 | 16.73 | 16.49 |
| | SSO | 19.38 | 15.22 | 13.88 | 13.12 | SSO | 16.55 | 13.92 | 12.92 | 12.58 |
| | MED | 12.35 | 9.13 | 7.94 | 7.18 | MED | 10.29 | 8.33 | 7.51 | 7.10 |
| | WEA | 2.69 | 1.85 | 1.39 | 1.13 | WEA | 2.60 | 1.94 | 1.50 | 1.16 |
| **-40°C** | | 20 | 30 | 40 | 50 | | 20 | 30 | 40 | 50 |
| | SSH | 148.81 | 96.56 | 80.59 | 67.44 | SSH | 69.91 | 51.11 | 45.82 | 39.82 |
| | SME | 75.76 | 49.59 | 42.74 | 38.59 | SME | 29.61 | 22.82 | 22.55 | 23.43 |
| | SSO | 30.08 | 20.67 | 18.91 | 17.30 | SSO | 22.79 | 18.12 | 18.36 | 18.95 |
| | MED | 21.26 | 12.95 | 11.04 | 9.55 | MED | 13.67 | 10.84 | 10.44 | 10.16 |
| | WEA | 5.70 | 3.17 | 2.11 | 1.72 | WEA | 4.85 | 3.51 | 2.51 | 1.82 |

**Table 7: Maximum toggle rates [MHz] for all driver settings at loads 20 … 50 pF; 16% Edges**

| | CLKOUT | | | | | GPIO | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **150°C** | | 20 | 30 | 40 | 50 | | 20 | 30 | 40 | 50 |
| | SSH | 73.53 | 58.82 | 50.00 | 44.48 | SSH | 45.45 | 35.71 | 27.23 | 23.58 |
| | SME | 41.67 | 35.21 | 32.47 | 30.34 | SME | 22.52 | 19.59 | 16.50 | 15.34 |
| | SSO | 17.01 | 15.15 | 13.74 | 13.44 | SSO | 16.23 | 14.04 | 11.82 | 11.36 |
| | MED | 10.25 | 8.33 | 7.58 | 7.20 | MED | 10.46 | 8.65 | 7.04 | 6.46 |
| | WEA | 2.00 | 1.54 | 1.26 | 1.02 | WEA | 2.07 | 1.56 | 1.27 | 1.02 |
| **125°C** | | 20 | 30 | 40 | 50 | | 20 | 30 | 40 | 50 |
| | SSH | 80.65 | 64.20 | 54.44 | 48.11 | SSH | 49.21 | 38.41 | 29.63 | 25.63 |
| | SME | 45.45 | 37.83 | 34.72 | 32.37 | SME | 24.08 | 20.76 | 17.83 | 16.60 |
| | SSO | 18.55 | 16.24 | 14.74 | 14.35 | SSO | 17.47 | 15.12 | 12.84 | 12.35 |
| | MED | 11.25 | 9.04 | 8.17 | 7.72 | MED | 11.18 | 9.22 | 7.61 | 7.01 |
| | WEA | 2.22 | 1.69 | 1.36 | 1.10 | WEA | 2.28 | 1.72 | 1.39 | 1.11 |
| **110°C** | | 20 | 30 | 40 | 50 | | 20 | 30 | 40 | 50 |
| | SSH | 85.62 | 67.93 | 57.51 | 50.59 | SSH | 51.78 | 40.24 | 31.29 | 27.03 |
| | SME | 48.08 | 39.60 | 36.23 | 33.72 | SME | 25.13 | 21.53 | 18.74 | 17.46 |
| | SSO | 19.61 | 16.98 | 15.41 | 14.96 | SSO | 18.28 | 15.85 | 13.55 | 13.02 |
| | MED | 11.95 | 9.53 | 8.57 | 8.06 | MED | 11.66 | 9.60 | 8.00 | 7.39 |
| | WEA | 2.38 | 1.80 | 1.44 | 1.16 | WEA | 2.43 | 1.83 | 1.48 | 1.18 |
| **85°C** | | 20 | 30 | 40 | 50 | | 20 | 30 | 40 | 50 |
| | SSH | 95.42 | 75.20 | 63.46 | 55.34 | SSH | 56.72 | 43.70 | 34.50 | 29.74 |
| | SME | 53.19 | 42.95 | 39.06 | 36.24 | SME | 27.09 | 22.95 | 20.27 | 19.11 |
| | SSO | 21.69 | 18.36 | 16.69 | 16.10 | SSO | 19.82 | 17.21 | 14.91 | 14.33 |
| | MED | 13.35 | 10.48 | 9.34 | 8.70 | MED | 12.57 | 10.30 | 8.75 | 8.12 |
| | WEA | 2.71 | 2.01 | 1.58 | 1.28 | WEA | 2.74 | 2.06 | 1.64 | 1.30 |
| **70°C** | | 20 | 30 | 40 | 50 | | 20 | 30 | 40 | 50 |
| | SSH | 102.46 | 80.37 | 67.67 | 58.64 | SSH | 60.15 | 46.08 | 36.77 | 31.65 |
| | SME | 56.82 | 45.24 | 40.98 | 37.94 | SME | 28.42 | 23.90 | 21.30 | 20.26 |
| | SSO | 23.16 | 19.31 | 17.56 | 16.86 | SSO | 20.87 | 18.00 | 15.86 | 15.24 |
| | MED | 14.35 | 11.14 | 9.87 | 9.14 | MED | 13.18 | 10.78 | 9.26 | 8.63 |
| | WEA | 2.95 | 2.16 | 1.68 | 1.36 | WEA | 2.96 | 2.22 | 1.76 | 1.39 |
| **25°C** | | 20 | 30 | 40 | 50 | | 20 | 30 | 40 | 50 |
| | SSH | 131.58 | 100.81 | 84.46 | 71.43 | SSH | 73.53 | 55.07 | 45.79 | 39.18 |
| | SME | 71.43 | 53.88 | 48.08 | 44.17 | SME | 33.33 | 27.26 | 25.10 | 24.73 |
| | SSO | 29.07 | 22.83 | 20.82 | 19.69 | SSO | 24.83 | 20.89 | 19.38 | 18.87 |
| | MED | 18.52 | 13.70 | 11.90 | 10.78 | MED | 15.43 | 12.50 | 11.26 | 10.65 |
| | WEA | 4.03 | 2.78 | 2.08 | 1.69 | WEA | 3.91 | 2.91 | 2.25 | 1.74 |
| **-40°C** | | 20 | 30 | 40 | 50 | | 20 | 30 | 40 | 50 |
| | SSH | 223.21 | 144.84 | 120.89 | 101.17 | SSH | 104.87 | 76.67 | 68.73 | 59.73 |
| | SME | 113.64 | 74.39 | 64.10 | 57.89 | SME | 44.42 | 34.23 | 33.82 | 35.15 |
| | SSO | 45.13 | 31.00 | 28.37 | 25.96 | SSO | 34.18 | 27.18 | 27.54 | 28.43 |
| | MED | 31.89 | 19.43 | 16.57 | 14.33 | MED | 20.50 | 16.26 | 15.66 | 15.24 |
| | WEA | 8.55 | 4.76 | 3.17 | 2.58 | WEA | 7.28 | 5.26 | 3.77 | 2.73 |

**Table 8: Maximum toggle rates [MHz] for all driver settings at loads 20..50pF; 25% edges**

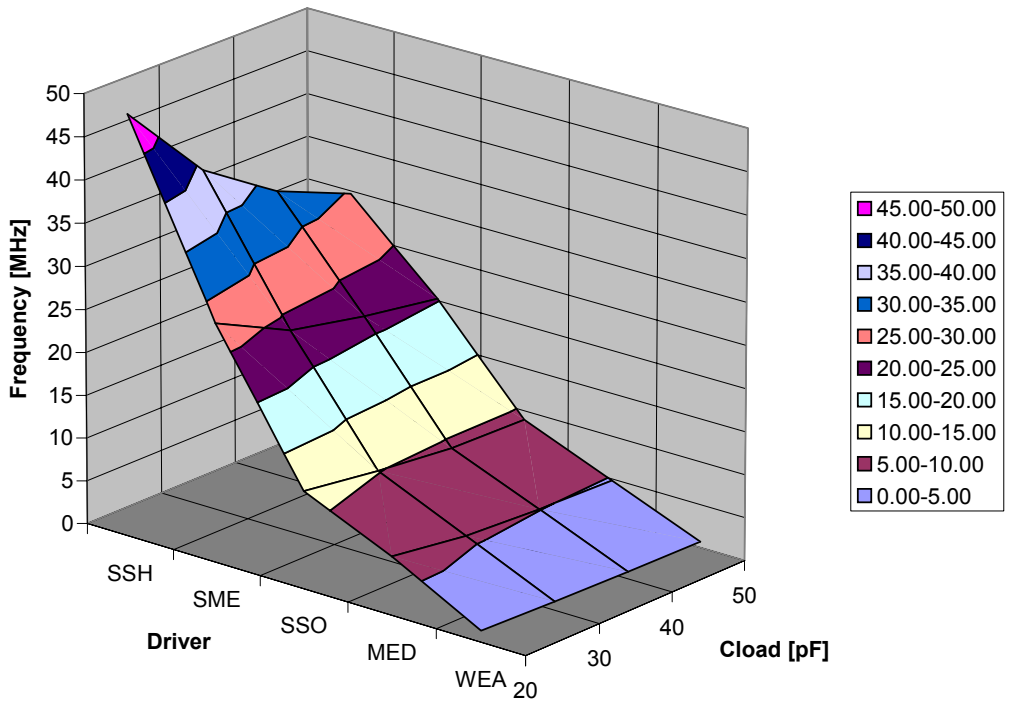


*Figure 165: Driver selection decision graph for CLKOUT at $T_A$=150°C; edges occupy 1/6 period*

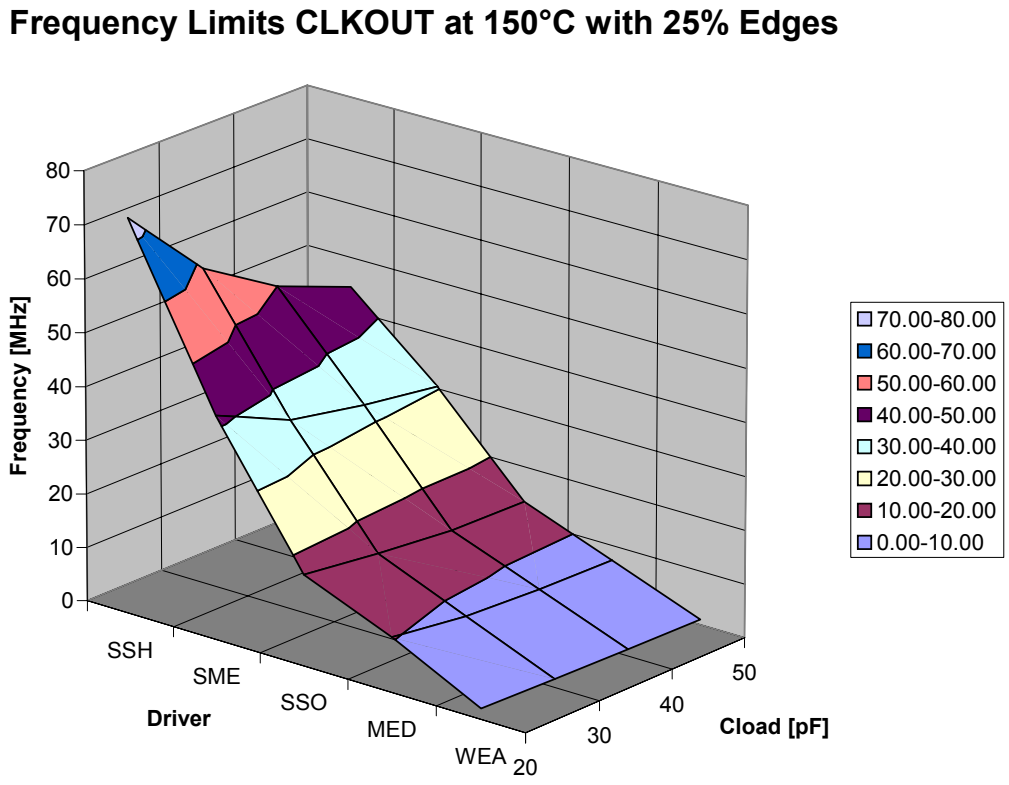


*Figure 166: Driver selection decision graph for CLKOUT at $T_A$=150°C; edges occupy 1/4 period*

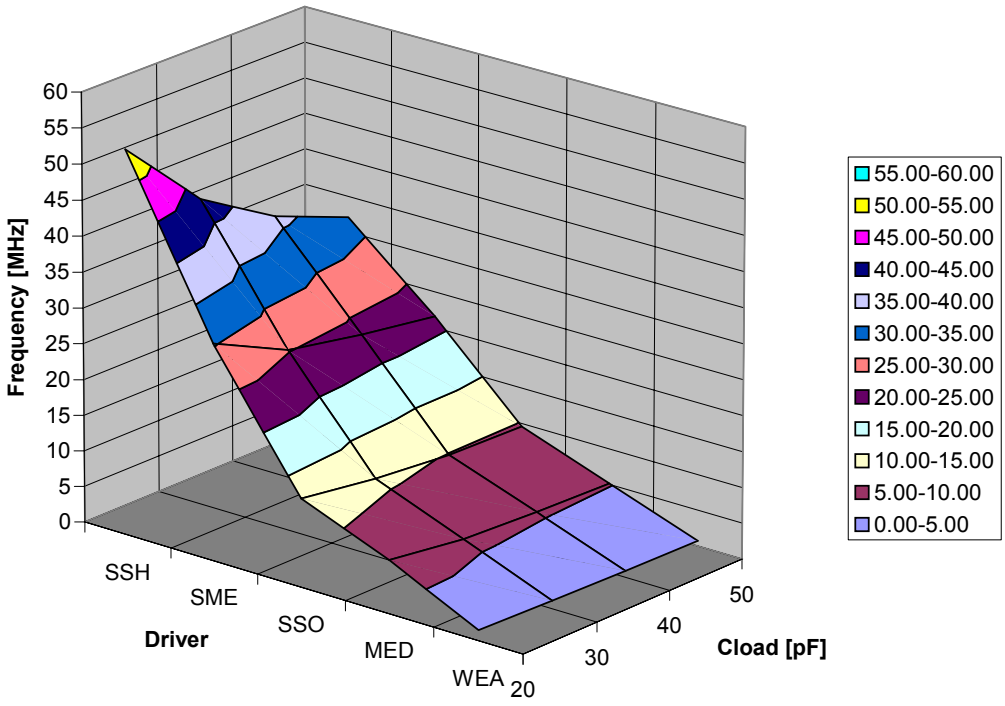


*Figure 167: Driver selection decision graph for CLKOUT at $T_A$=125°C; edges occupy 1/6 period*

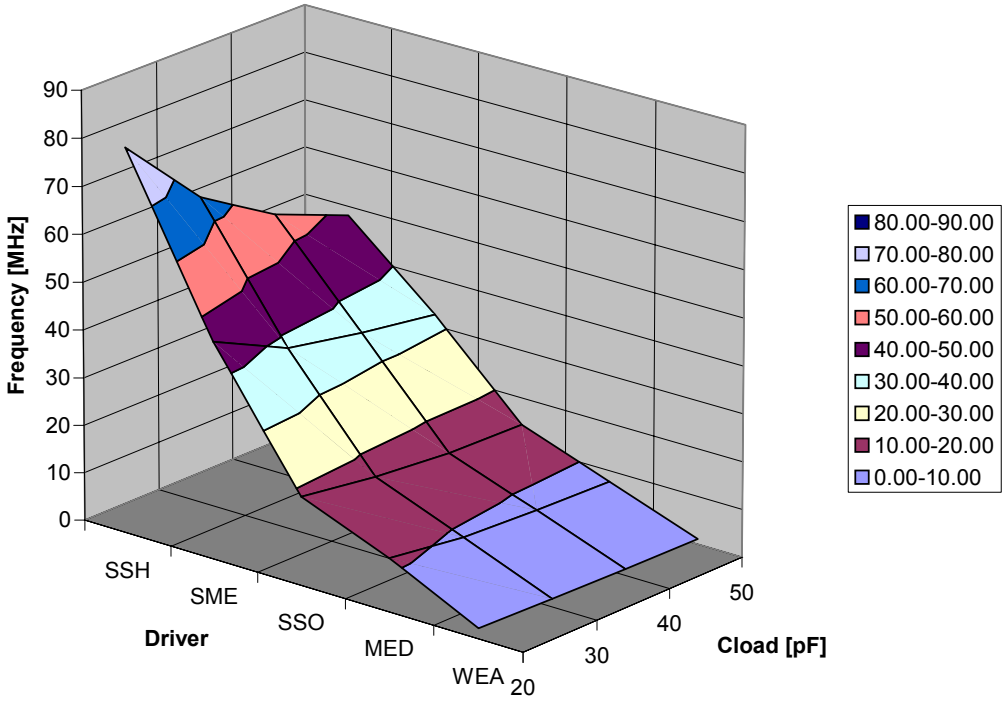


*Figure 168: Driver selection decision graph for CLKOUT at $T_A$=125°C; edges occupy 1/4 period*

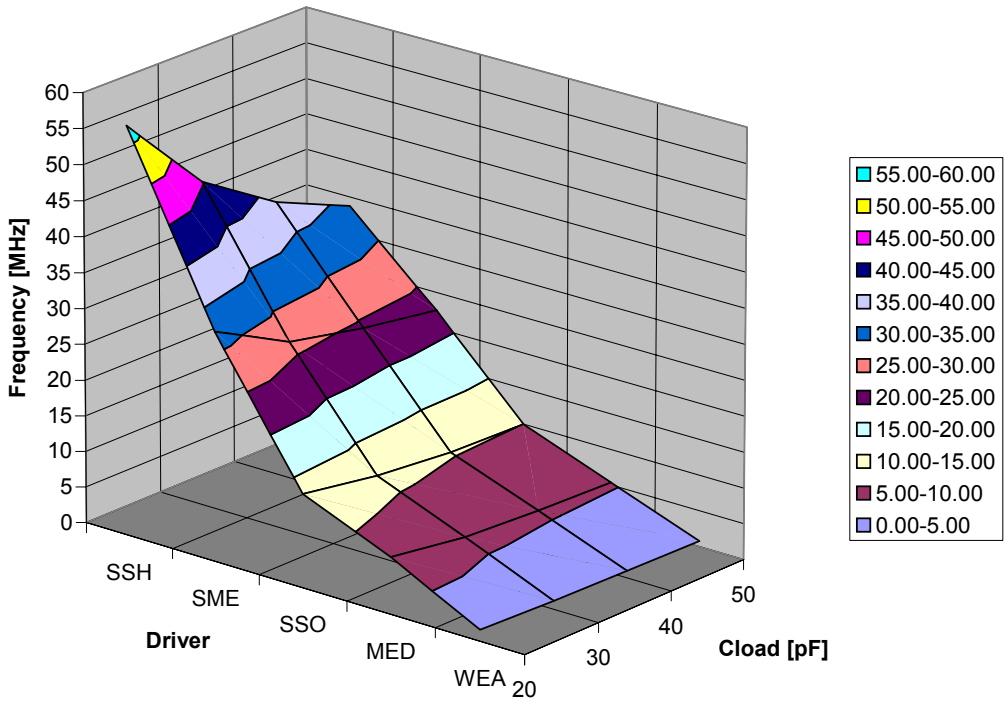


*Figure 169: Driver selection decision graph for CLKOUT at $T_A$=110°C; edges occupy 1/6 period*

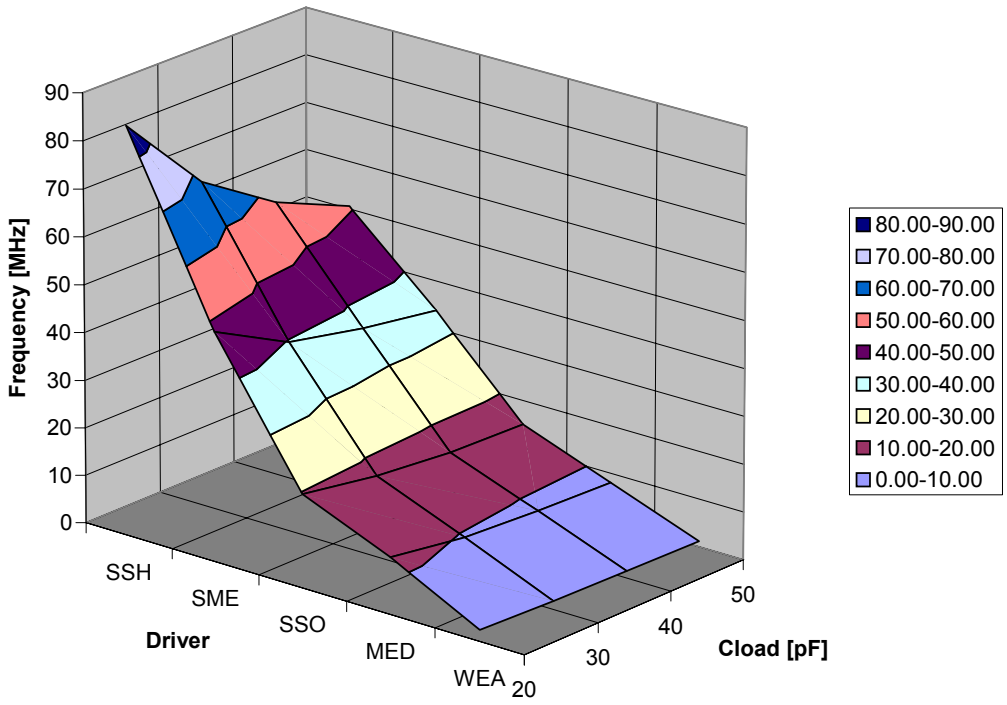


*Figure 170: Driver selection decision graph for CLKOUT at $T_A$=110°C; edges occupy 1/4 period*

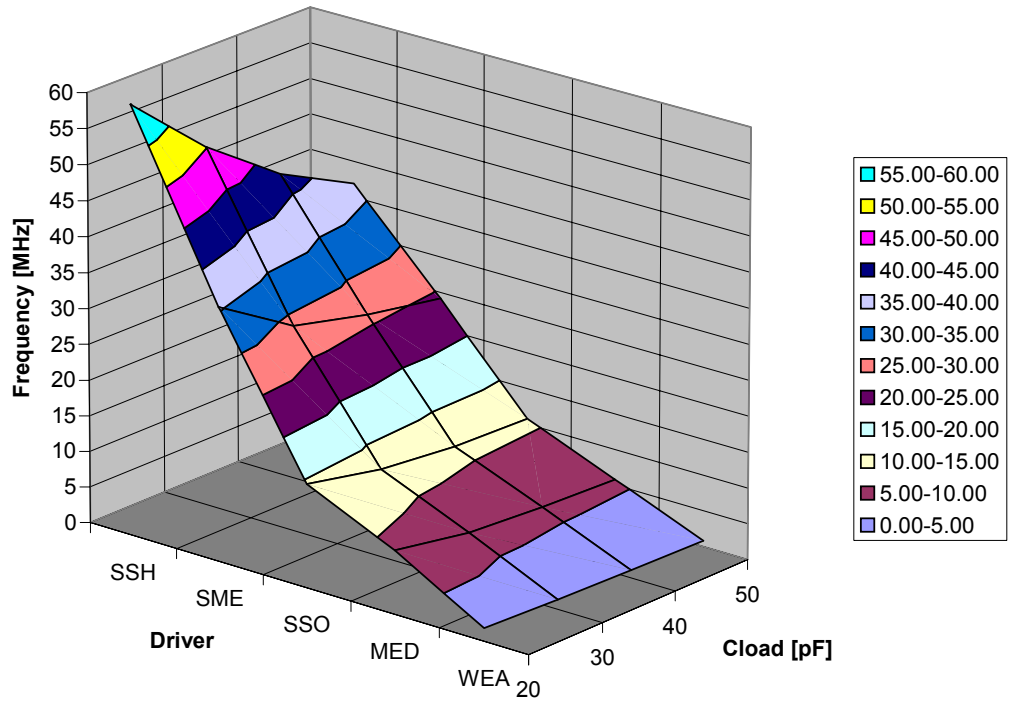


*Figure 171: Driver selection decision graph for CLKOUT at $T_A$=85°C; edges occupy 1/6 period*

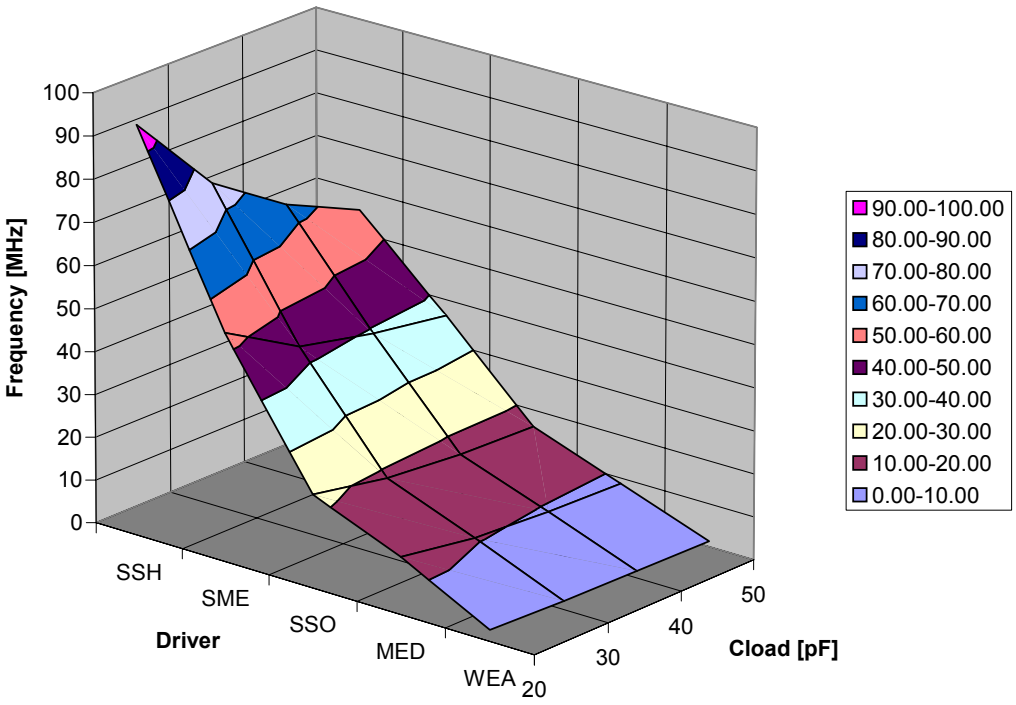


*Figure 172: Driver selection decision graph for CLKOUT at $T_A$=85°C; edges occupy 1/4 period*

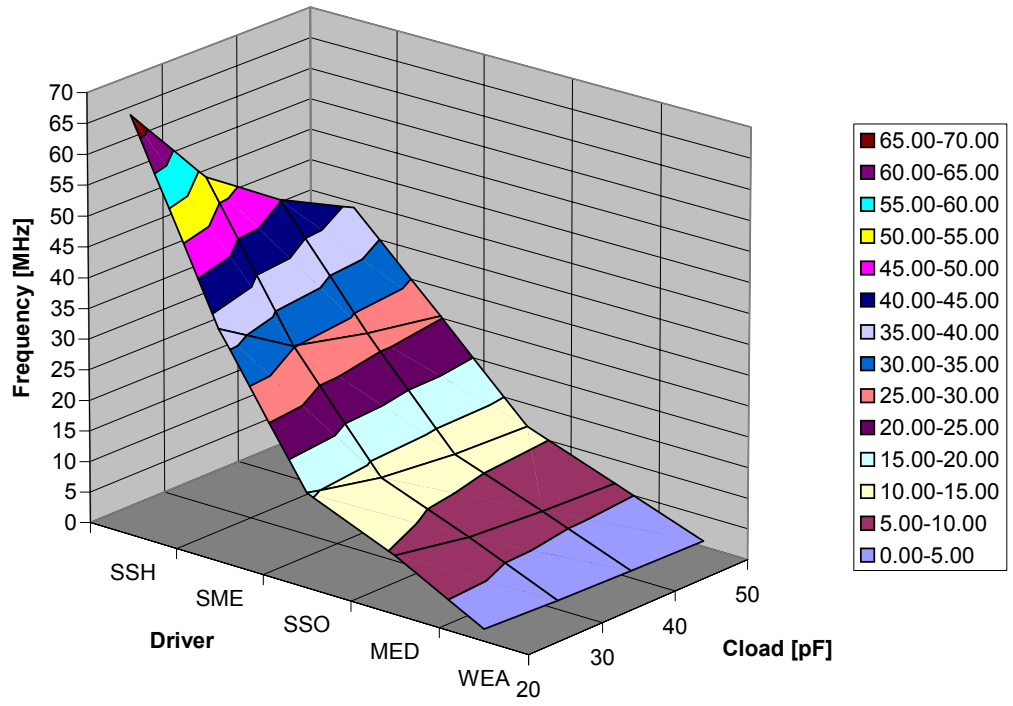


*Figure 173: Driver selection decision graph for CLKOUT at $T_A$=70°C; edges occupy 1/6 period*

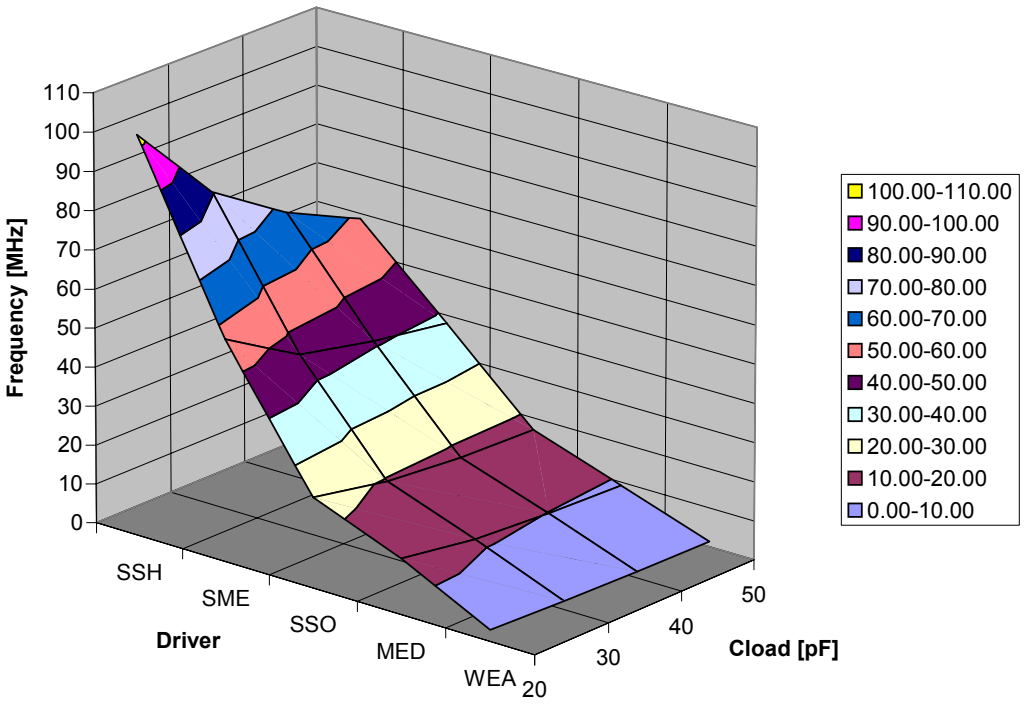


*Figure 174: Driver selection decision graph for CLKOUT at $T_A$=70°C; edges occupy 1/4 period*

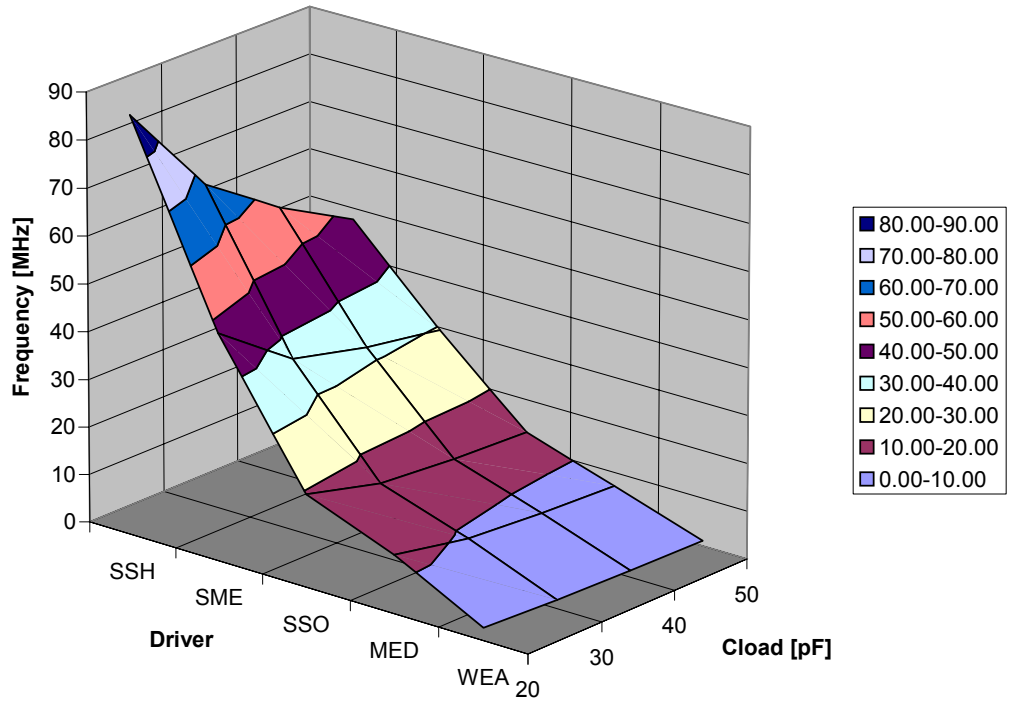


*Figure 175: Driver selection decision graph for CLKOUT at $T_A$=25°C; edges occupy 1/6 period*

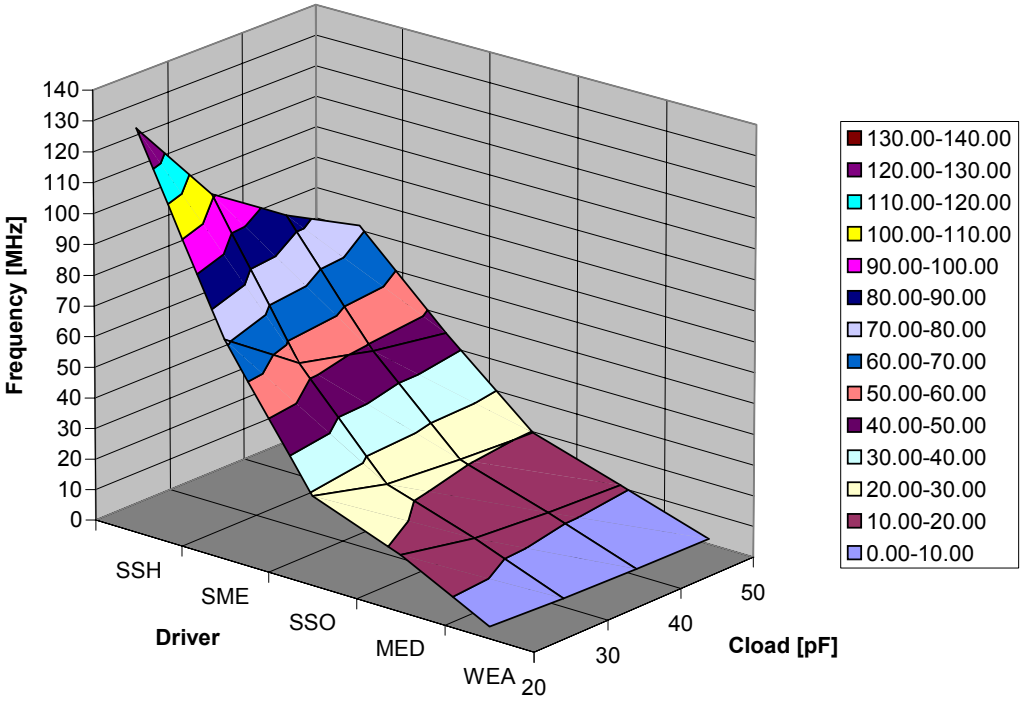


*Figure 176: Driver selection decision graph for CLKOUT at $T_A$=25°C; edges occupy 1/4 period*

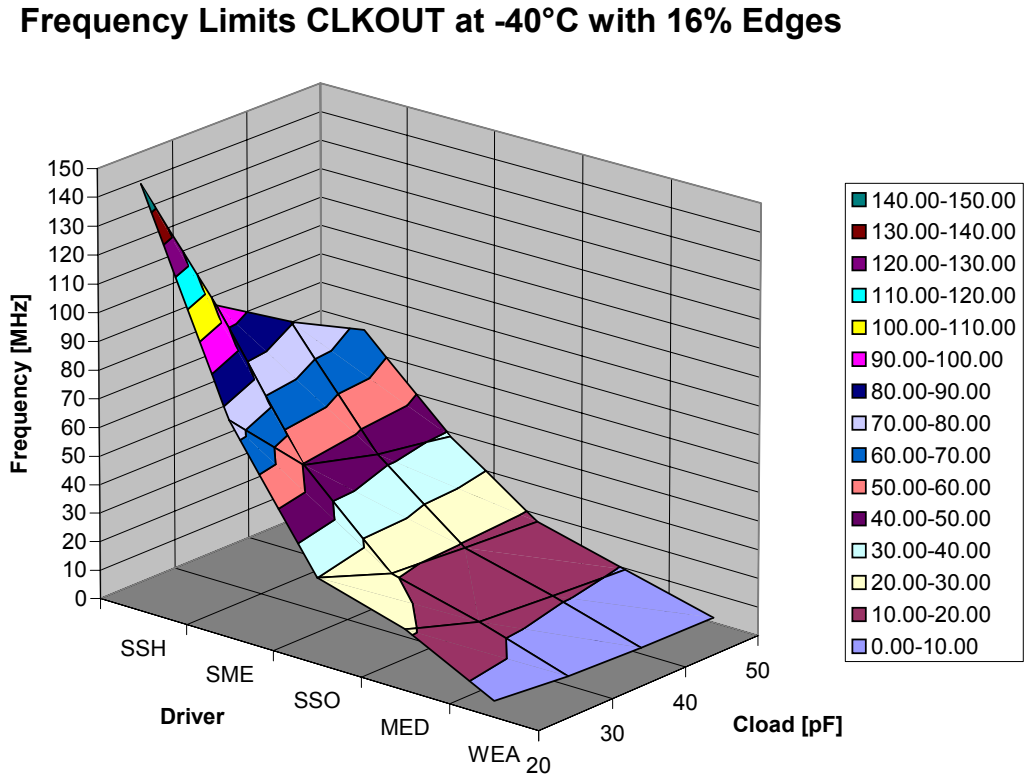


*Figure 177: Driver selection decision graph for CLKOUT at $T_A$=-40°C; edges occupy 1/6 period*

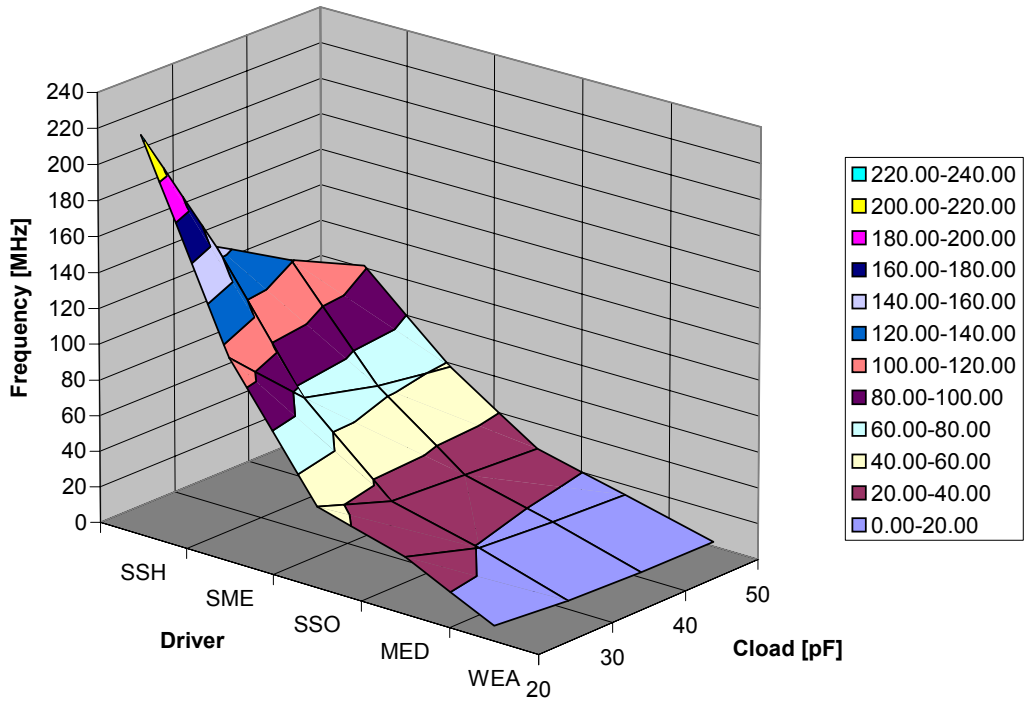


*Figure 178: Driver selection decision graph for CLKOUT at $T_A$=-40°C; edges occupy 1/4 period*

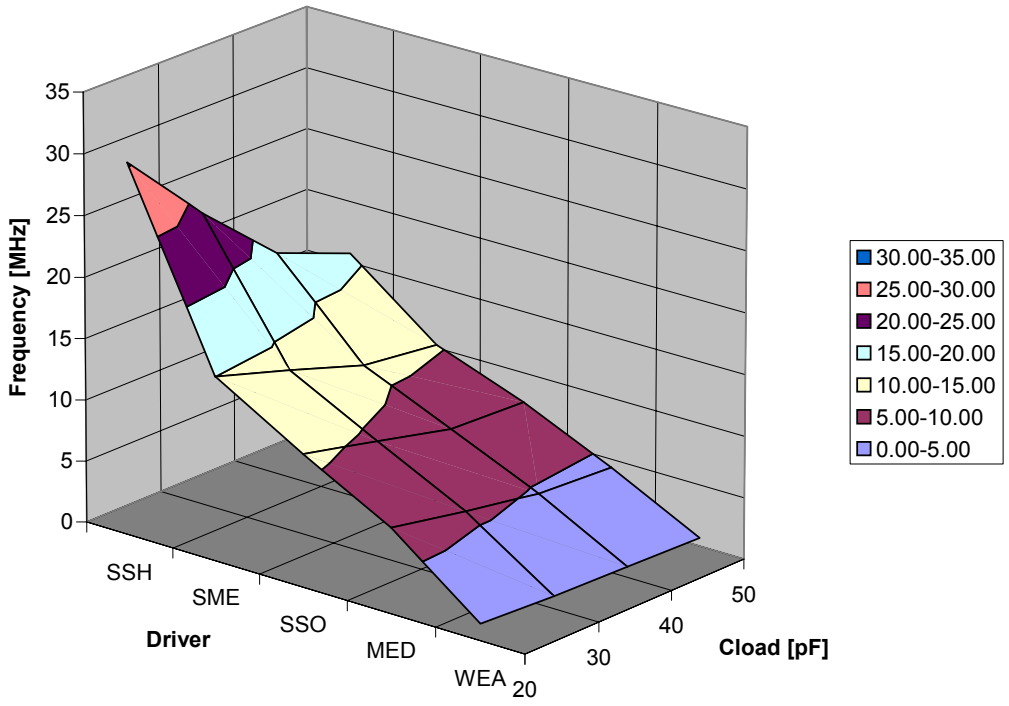


*Figure 179: Driver selection decision graph for GPIO at $T_A$=150°C; edges occupy 1/6 period*

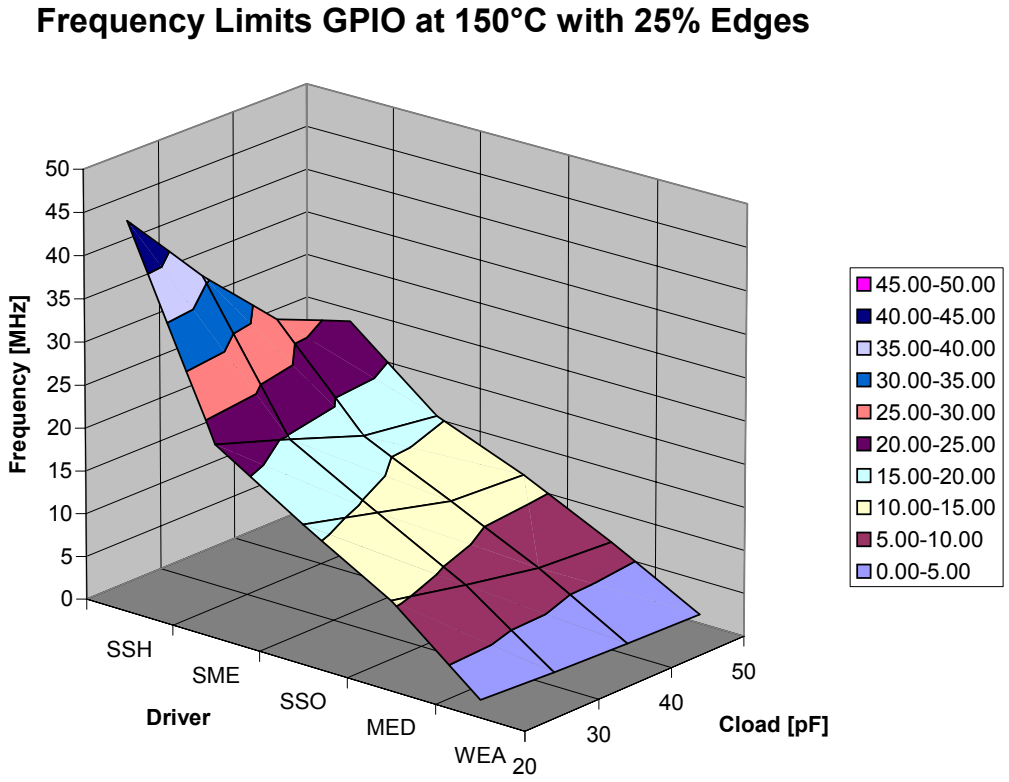


*Figure 180: Driver selection decision graph for GPIO at $T_A$=150°C; edges occupy 1/4 period*

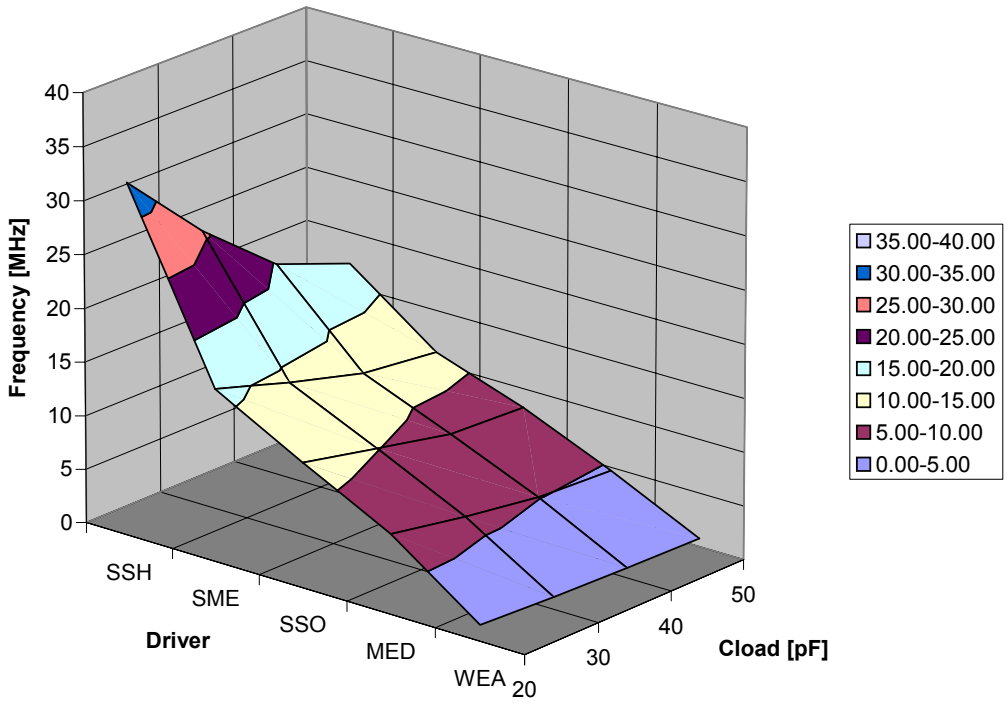


*Figure 181: Driver selection decision graph for GPIO at $T_A$=125°C; edges occupy 1/6 period*

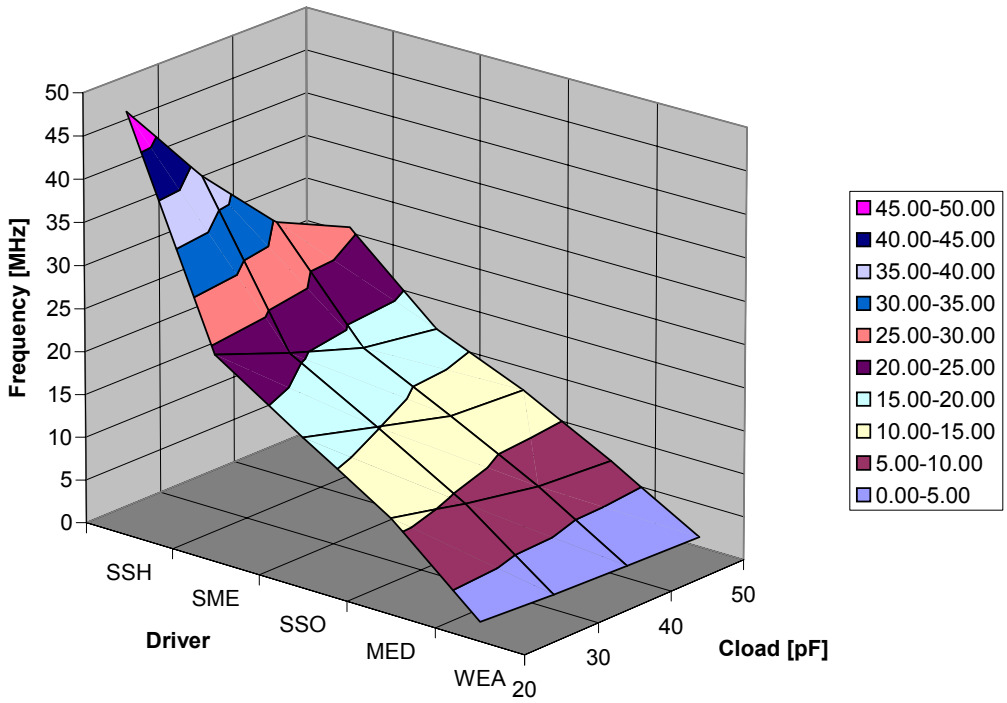


*Figure 182: Driver selection decision graph for GPIO at $T_A$=125°C; edges occupy 1/4 period*

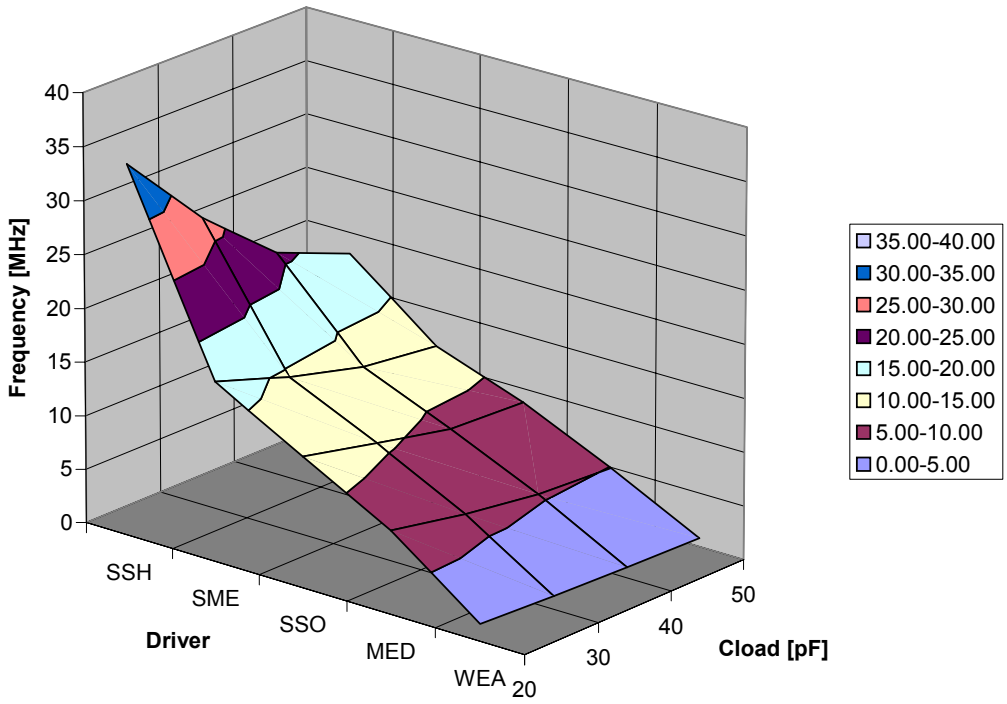


*Figure 183: Driver selection decision graph for GPIO at $T_A$=110°C; edges occupy 1/6 period*

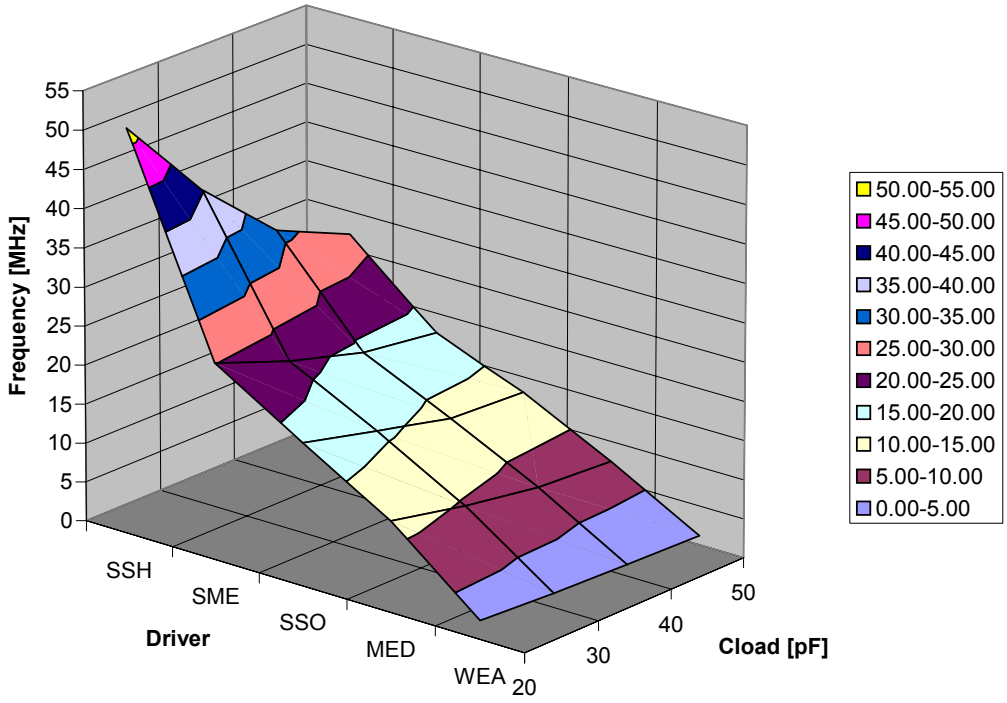


*Figure 184: Driver selection decision graph for GPIO at $T_A$=110°C; edges occupy 1/4 period*

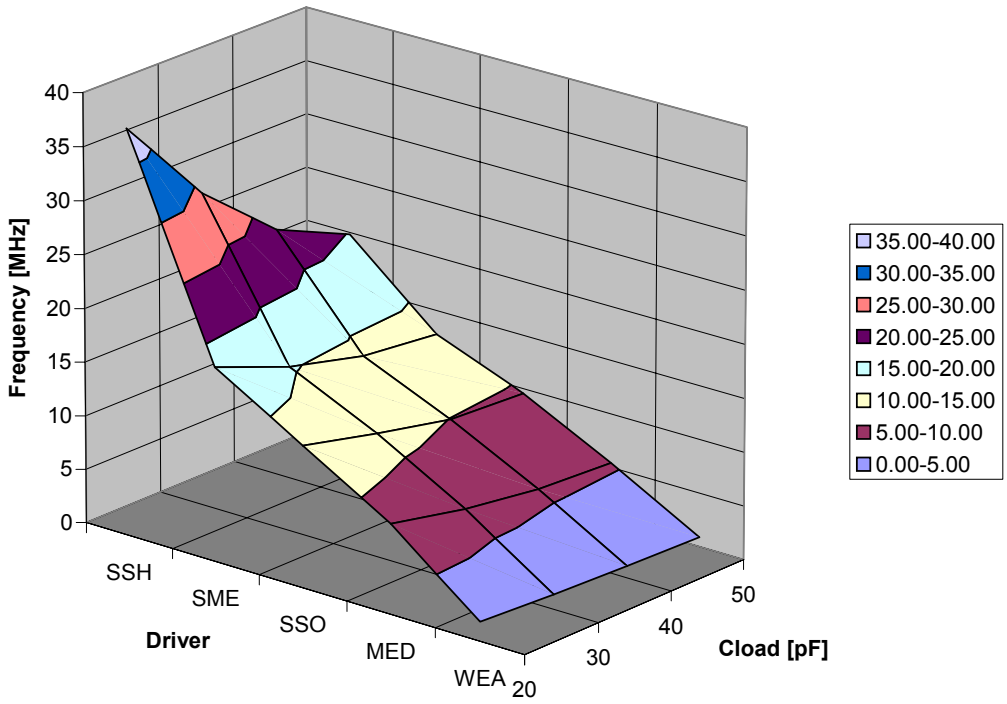


*Figure 185: Driver selection decision graph for GPIO at $T_A$=85°C; edges occupy 1/6 period*

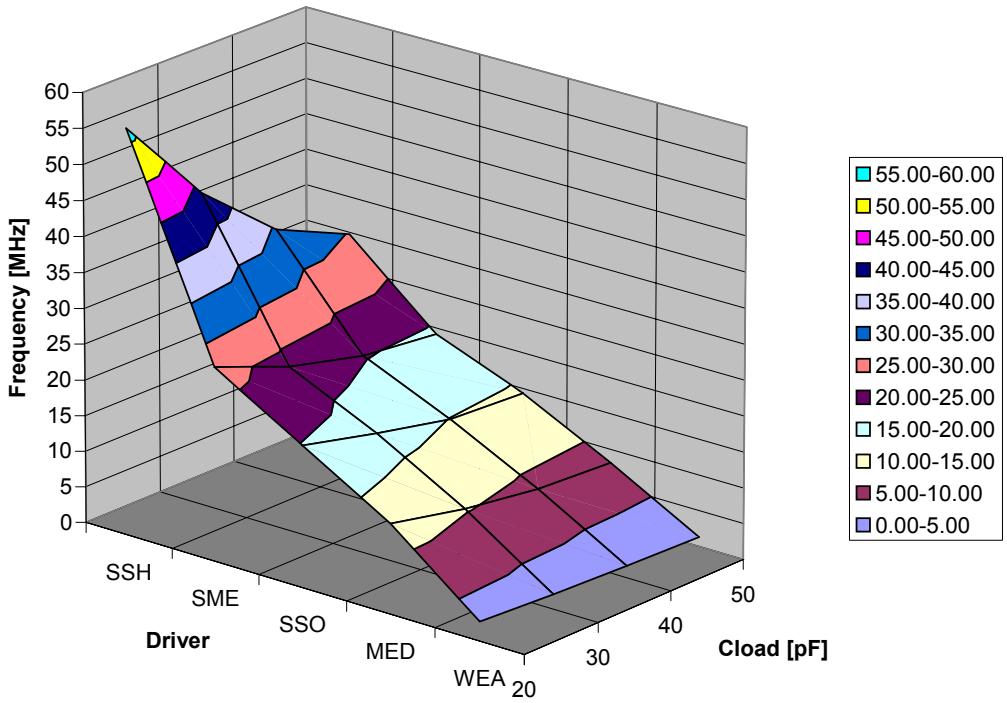


*Figure 186: Driver selection decision graph for GPIO at $T_A$=85°C; edges occupy 1/4 period*

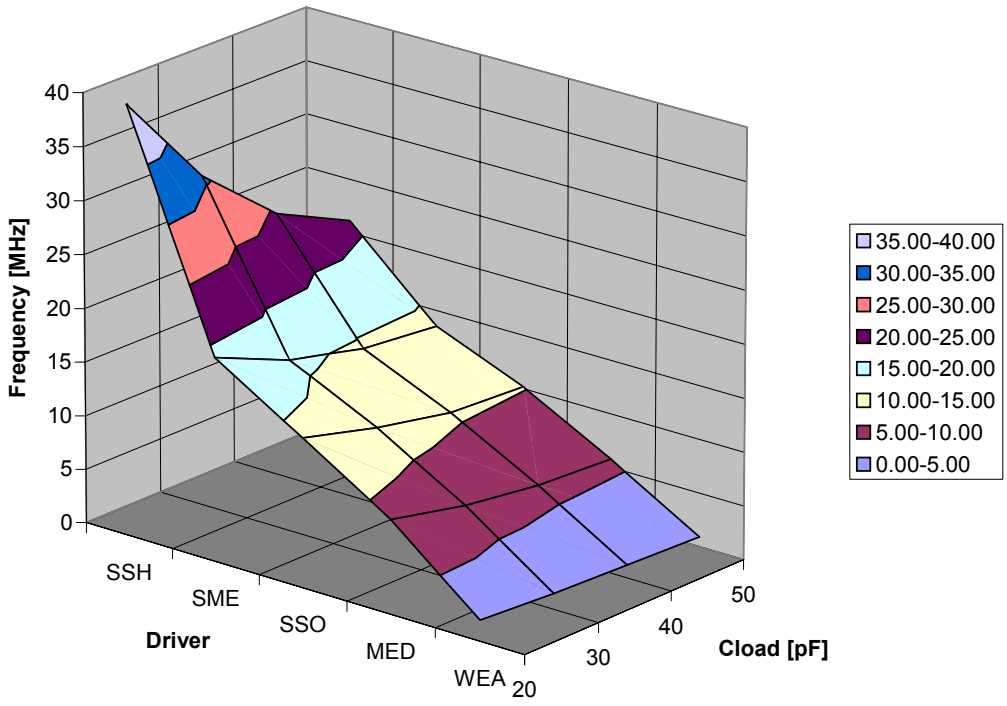


*Figure 187: Driver selection decision graph for GPIO at $T_A$=70°C; edges occupy 1/6 period*

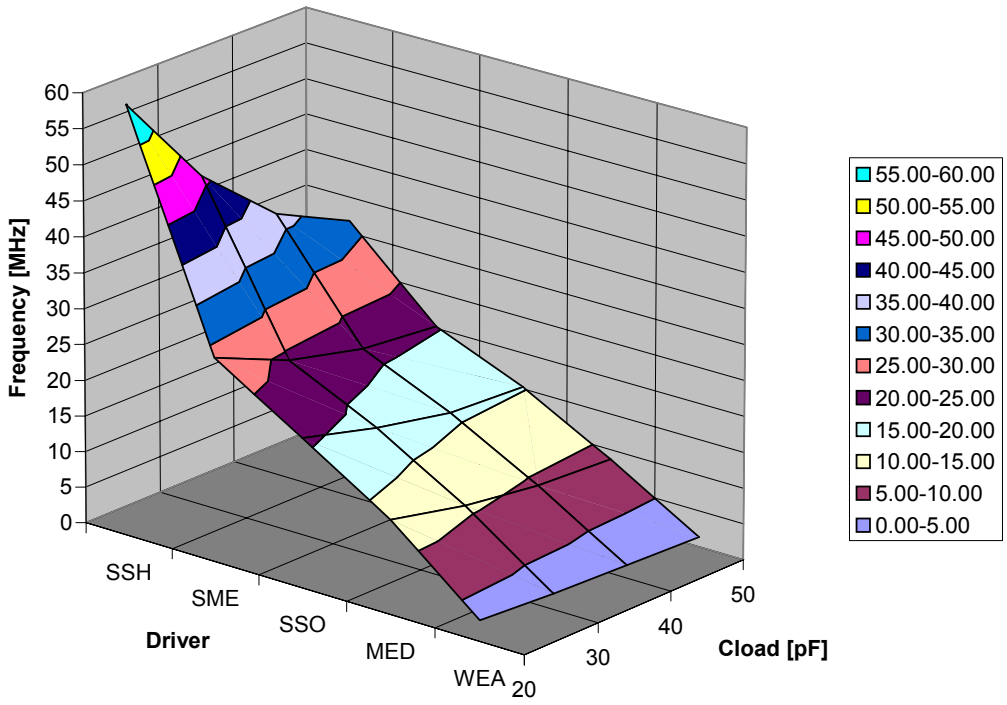


*Figure 188: Driver selection decision graph for GPIO at $T_A$=70°C; edges occupy 1/4 period*

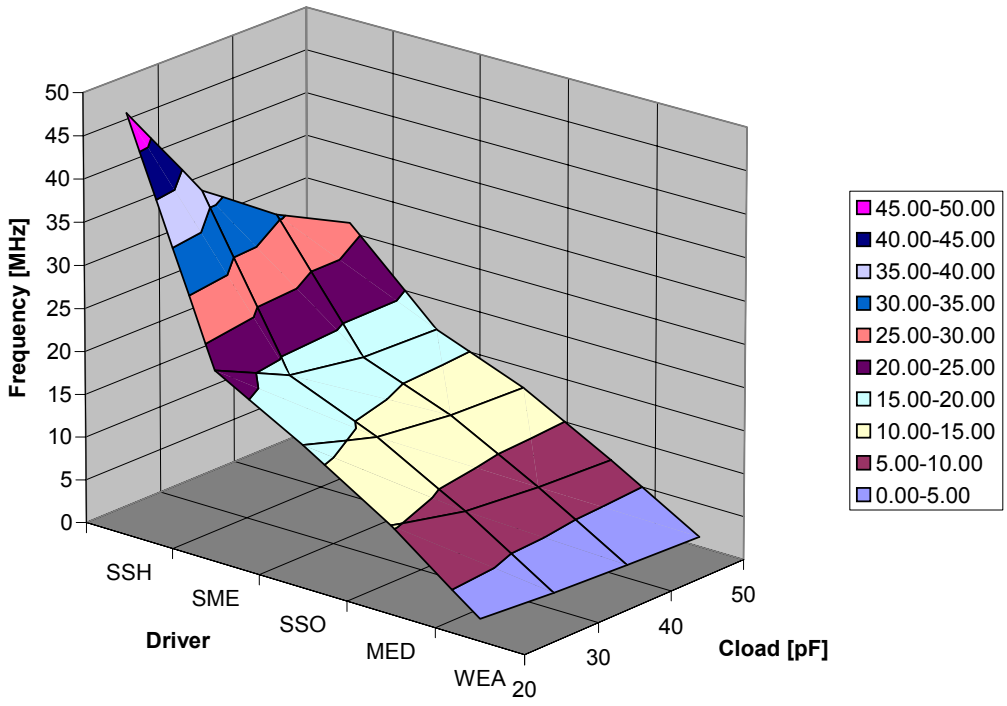


*Figure 189: Driver selection decision graph for GPIO at $T_A$=25°C; edges occupy 1/6 period*

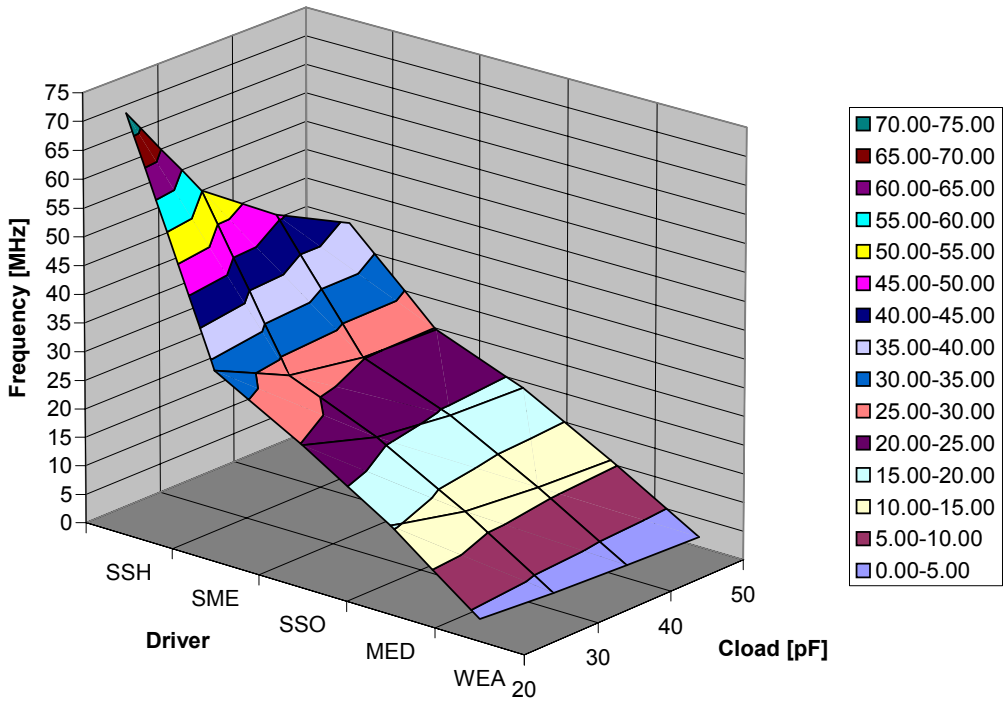


*Figure 190: Driver selection decision graph for GPIO at $T_A$=25°C; edges occupy 1/4 period*

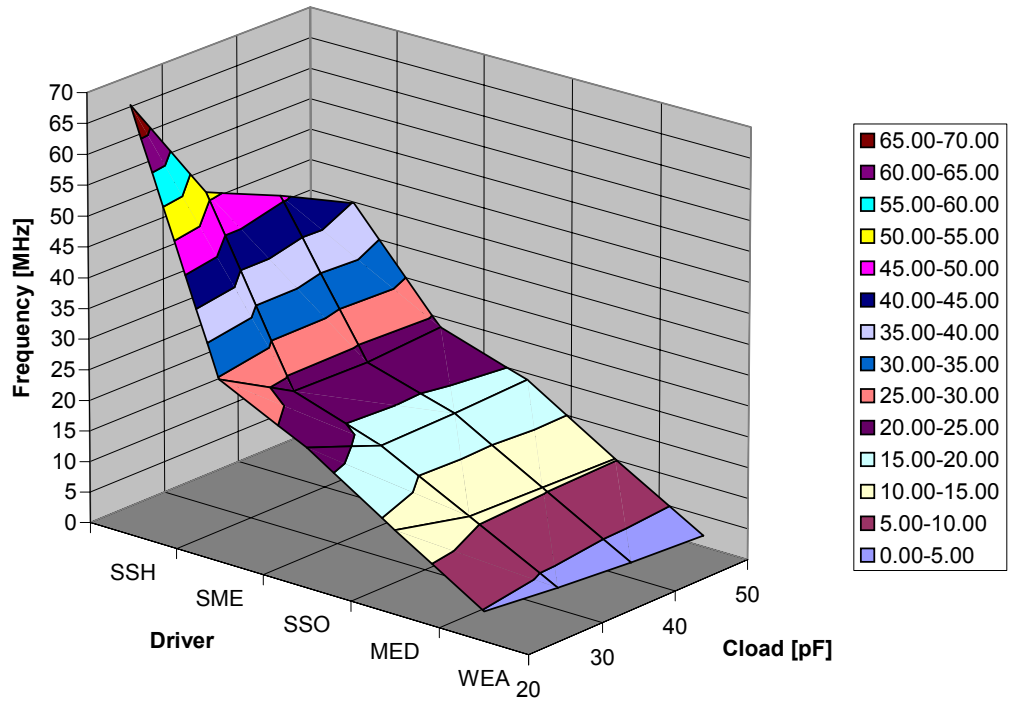


*Figure 191: Driver selection decision graph for GPIO at $T_A$=-40°C; edges occupy 1/6 period*

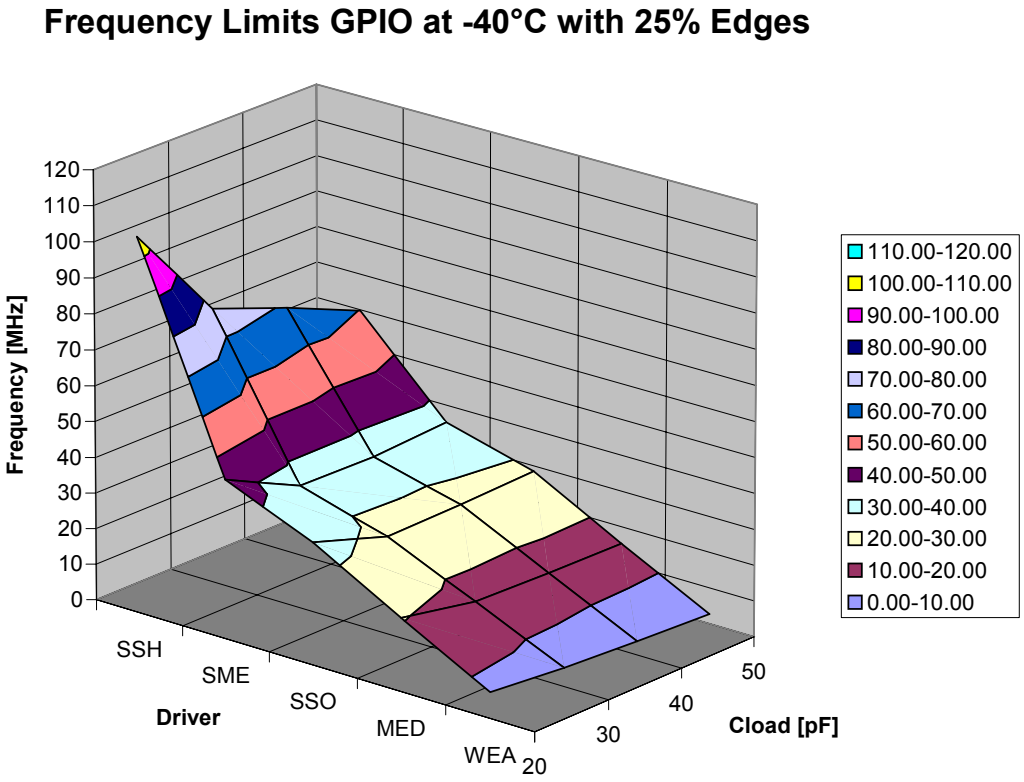


*Figure 192: Driver selection decision graph for GPIO at $T_A$=-40°C; edges occupy 1/4 period*

# 8 Glossary

| | | |
|---|---|---|
| CLKOUT | System Clock Output | Strong output driver for the system clock. |
| $C_{load}$ | Load Capacitor | Ideal capacitive load connected to an output driver. |
| di/dt | | Dynamic current over time |
| EMC | Electromagnetic Compatibility | The ability of an electrical device to function satisfactorily in its electromagnetic environment (“Immunity”) without having an impermissible effect on its environment (“Emission”). |
| EME | Electromagnetic Emission | → EMC |
| GND | Ground | Ground reference of the power supply. |
| GPIO | General Purpose Input/Output | Standard output driver with no special electric specification. |
| PI | Power Integrity | Good PI means a clean power supply system which is not polluted by switching noise. |
| SI | Signal Integrity | Good SI means proper signal waveform to fulfill the required data communication. |
| $T_A$ | Ambient Temperature | Temperature in the direct environment of the IC. |
| VDD | | Power supply voltage in general. |
| VDDC | | Core supply voltage = 2.5V nominal. |
| VDDP | | Pad supply voltage = 5.0V nominal. |
| VSS | | → GND |

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