Application Note

Usage and Limitations of DRAL "Data Rate Acceptance Limitation" Function in TDA5235/TDA5240

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Abstract

- DRAL: Data Rate Acceptance Limitation controlled by CDRDRTHRP and CDRDRTHRN registers)
- In **Self Polling Mode** (SPM) the DRAL function of TDA5235/40 can be used to narrow the acceptance range of the received data rate.
- In **Run Mode Slave** (RMS) the DRAL function shall not be used!
  - But the Valid Pulse Width criterion (x_CDRTOLB and x_CDRTOLC registers) can be used to narrow the accepted range of the received data rate in RMS.
- To achieve rejection of unwanted data rate of an interfering signal:
  - the functional block "DRAL" and "CDRTOL valid pulse width" can be used in SelfPollingMode
  - the functional block "CDRTOL valid pulse width" **ONLY** can be used in RunModeSlave
- However, the Signal Recognition thresholds (SigRec = x_SIGDET0/1, x_NDTHRES, x_SIGDETLO) need to be set properly according to our Application Note "Signal Noise Detector Settings" for both RMS and SPM.

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Limitation of DRAL Function in RunModeSlave

Data Rate Acceptance Limitation (DRAL) function of TDA5235/40, when used in **RunModeSlave (RMS)**:

1. DRAL evaluates the data rate also within the noise and possible unwanted signals (interferer) before the wanted signal, then:
2. Since noise & unwanted signals contain random edges the **accumulated data rate error (DRE)** is a random number, then:
3. If accumulated DRE is outside of the valid range when wanted signal message is received, even this valid message is rejected (this event is random, depends on noise and interferer history before the wanted signal and thus does not depend on the wanted signal power)

- ☐ This yields in an increased Missed Message Rate in RunModeSlave

Keep in mind: **SelfPolling Mode (SPM) does not show this limitation of DRAL function**

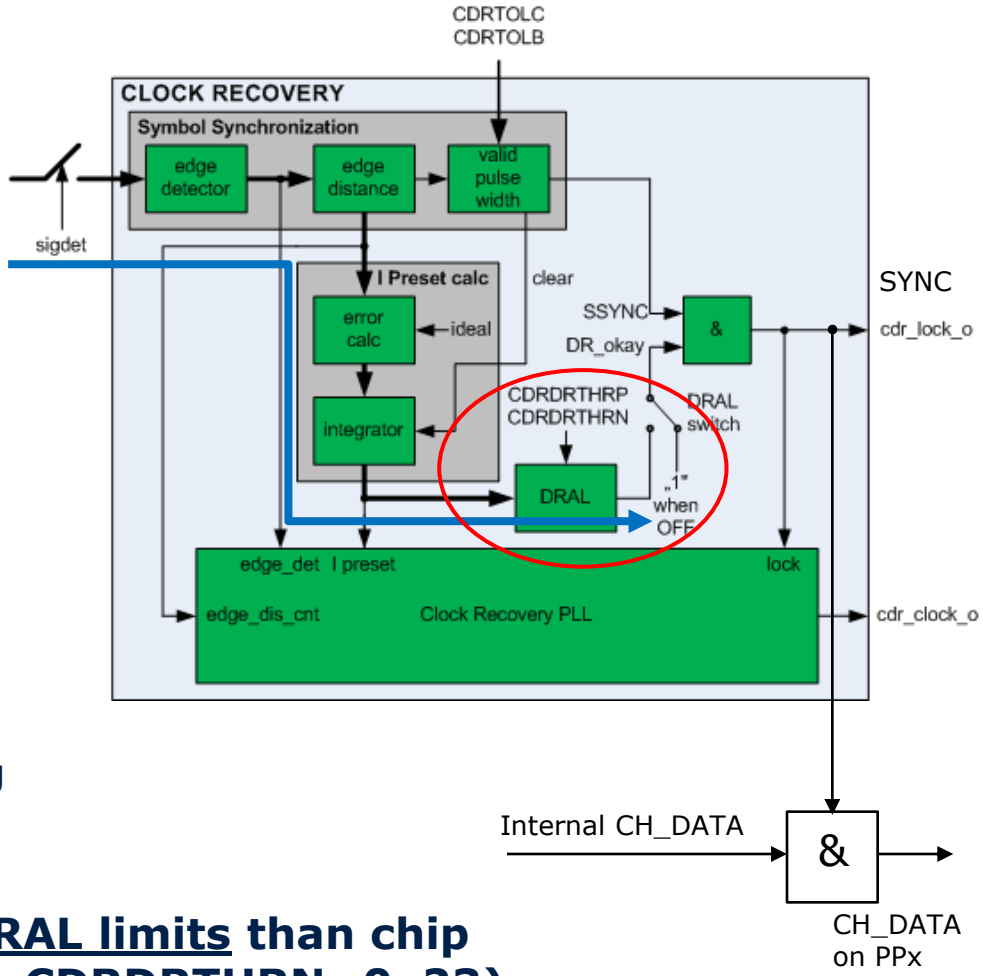
- SEE NEXT SLIDES FOR DETAILS -

Data Rate Acceptance Limitation (DRAL) Block Description

- DRAL is part of clock recovery block

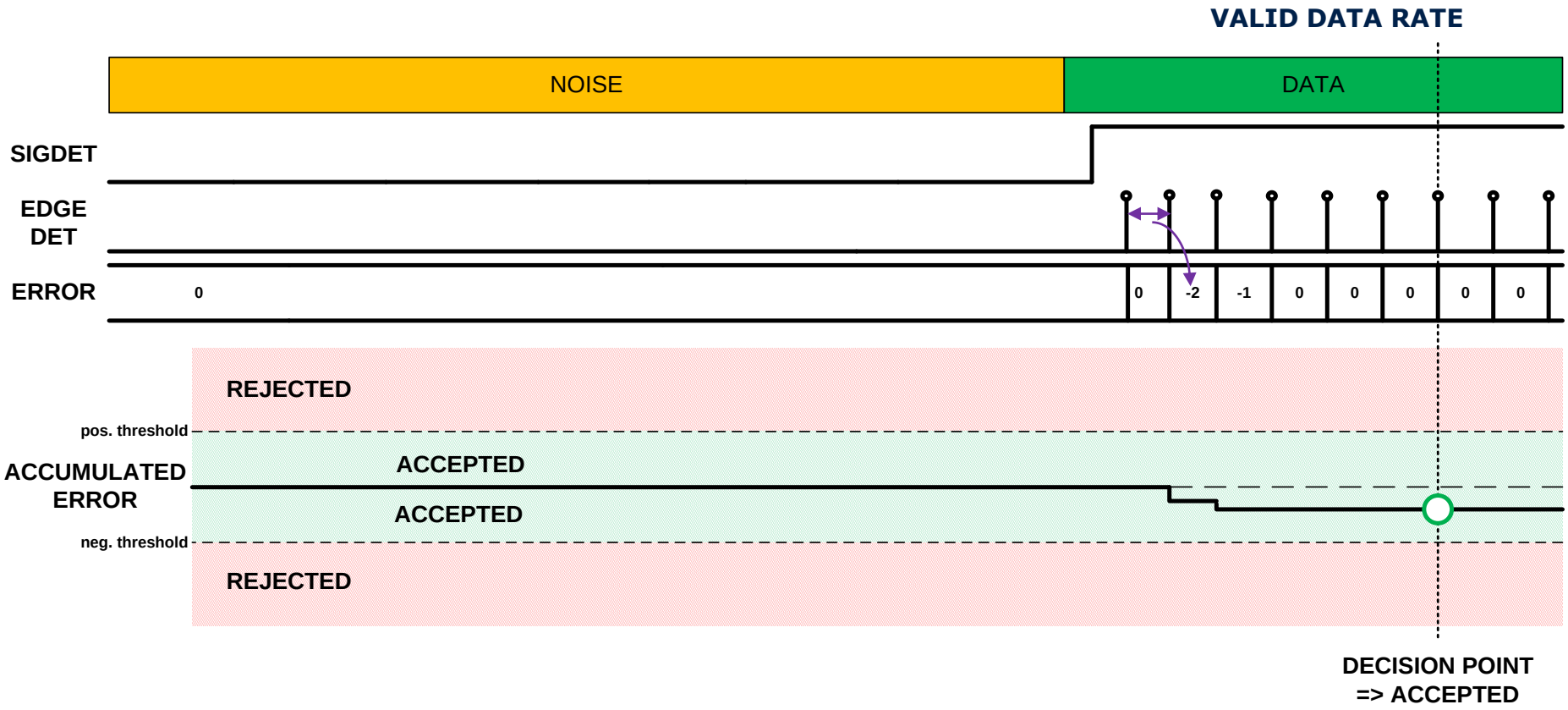
  (see DRAL signal flow ➔ **blue arrow**)

- Integrated error is proportional to the data rate error
- Input data to clock recovery is masked with SIGDET
  - SIGDET can be active also due to noise or interferer
- Integrator accumulates error whenever input signal is detected (SIGDET=1)
  - Cleared with system reset, system init, falling edge of SSYNC or clear signal (last measured edge distance out of "valid pulse width" window)
  - Always cleared when switching to RUN mode (during startup time ➔ at beginning of SelfPollingMode / RunModeSlave)



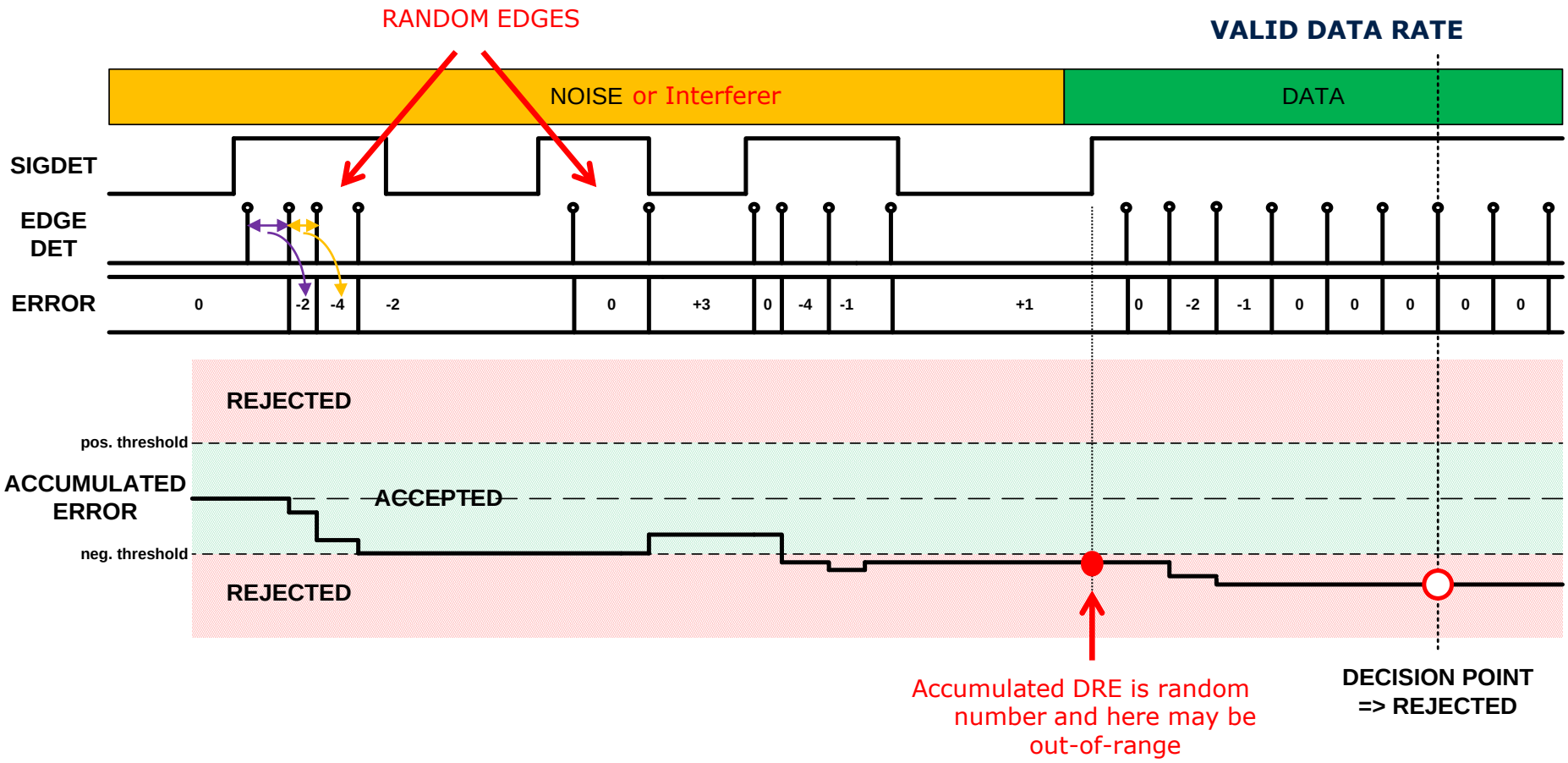
- **General Hint: Do NOT use tighter DRAL limits than chip default values (CDRDRTHRP=0x1E, CDRDRTHRN=0x23)**

Data Rate Acceptance Limitation (DRAL)
Intended Operation



- Unfortunately SIGDET can be active due to noise or interferer and therefore the intended operation cannot be ensured (see next page)

Data Rate Acceptance Limitation (DRAL)
Unintended Operation in RunModeSlave

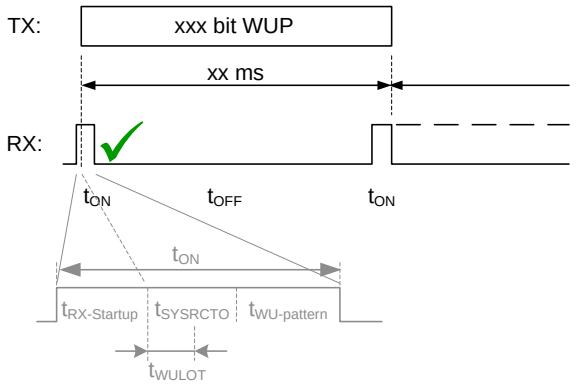


- Even in case (Wanted signal) data rate is valid, the frame will be rejected

  ➔ **DRAL function shall not be used in RunModeSlave**

Data Rate Acceptance Limitation (DRAL) **in Self Polling Mode**

- DRAL functionality was originally developed to reduce the current consumption by not allowing continuous wake-up on interferers with invalid data rate in **Self-Polling-Mode** (SPM)
- The accumulated data rate error is reset again at the beginning of each ON-time (during start-up time)
- In SPM the polling period (t_{ON} + t_{OFF}) needs to be set in a way that a valid signal is available during ON-time

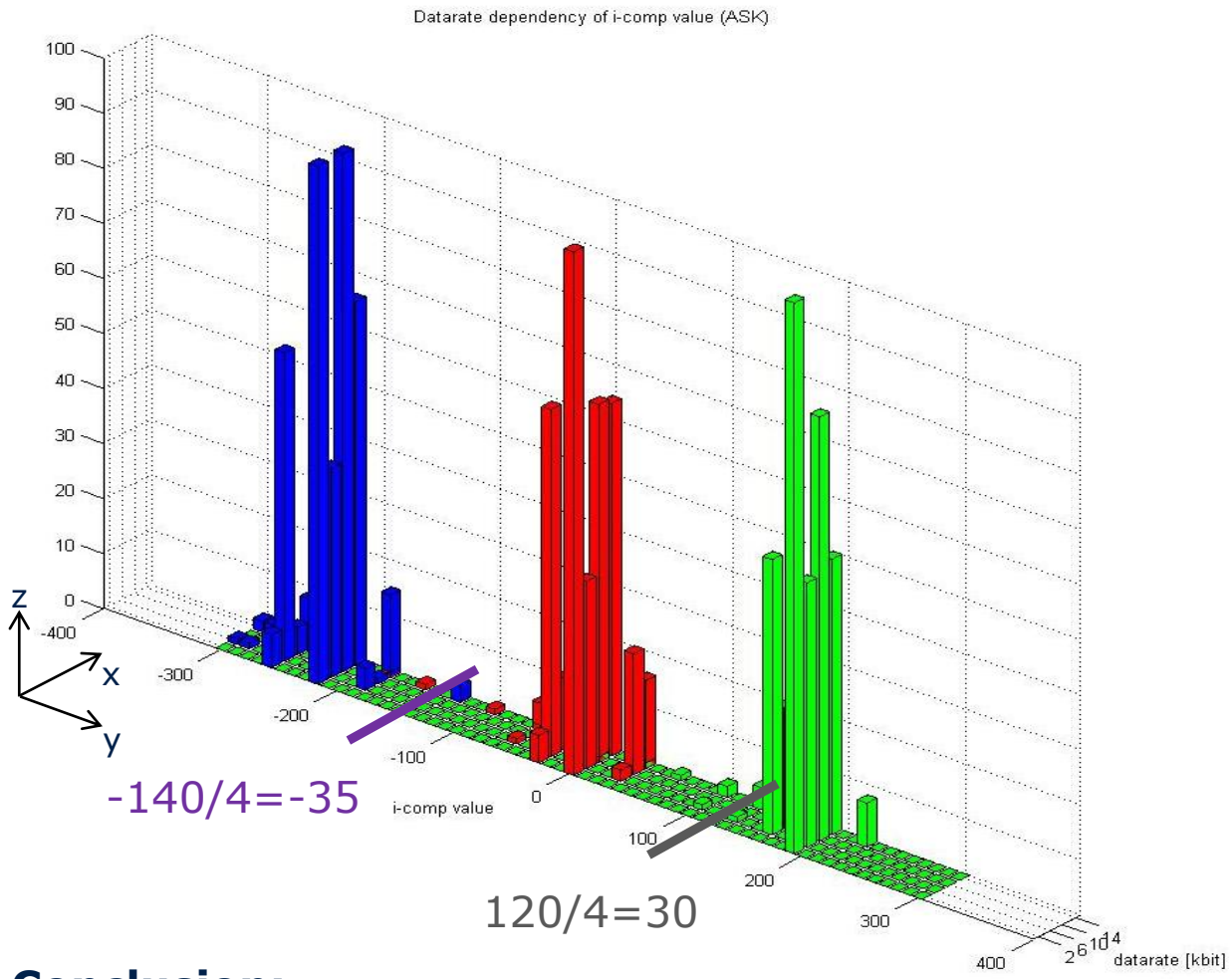


  - Example above shows that WU will be generated already in first ON-time.
  - In case TX is delayed, then WU will NOT be generated in first ON-time, but in second ON-time.

Conclusion:

DRAL function can be used in SelfPollingMode (no limitation in SPM)

Estimation of DRAL Threshold Default Values (CDRDRTHRP + CDRDRTHRN)



X-axis: 4 different nominal datarates are simulated

Y-axis: internal threshold due to 3 datarate variations (-10%, 0%, +10%)

Z-axis: occurance probability for a certail internal threshold
* for each datarate and
* for each datarate variation

12 (=4*3) scenarios
100 simulations per scenario

Formula for selected thresholds CDRDRTHRP and CDRDRTHRN:

Internal_threshold_neg = 4 x CDRDRTHRN

Internal_threshold_pos = 4 x CDRDRTHRP

Conclusion:

CDRDRTHRP and CDRDRTHRN must be estimated empirically based on measurements on the final application

Default values of both CDRDRTHRP and CDRDRTHRN are estimated for a given DRA range of +/-10% of nominal datarate, so that frames with invalid datarate are rejected with high probability.

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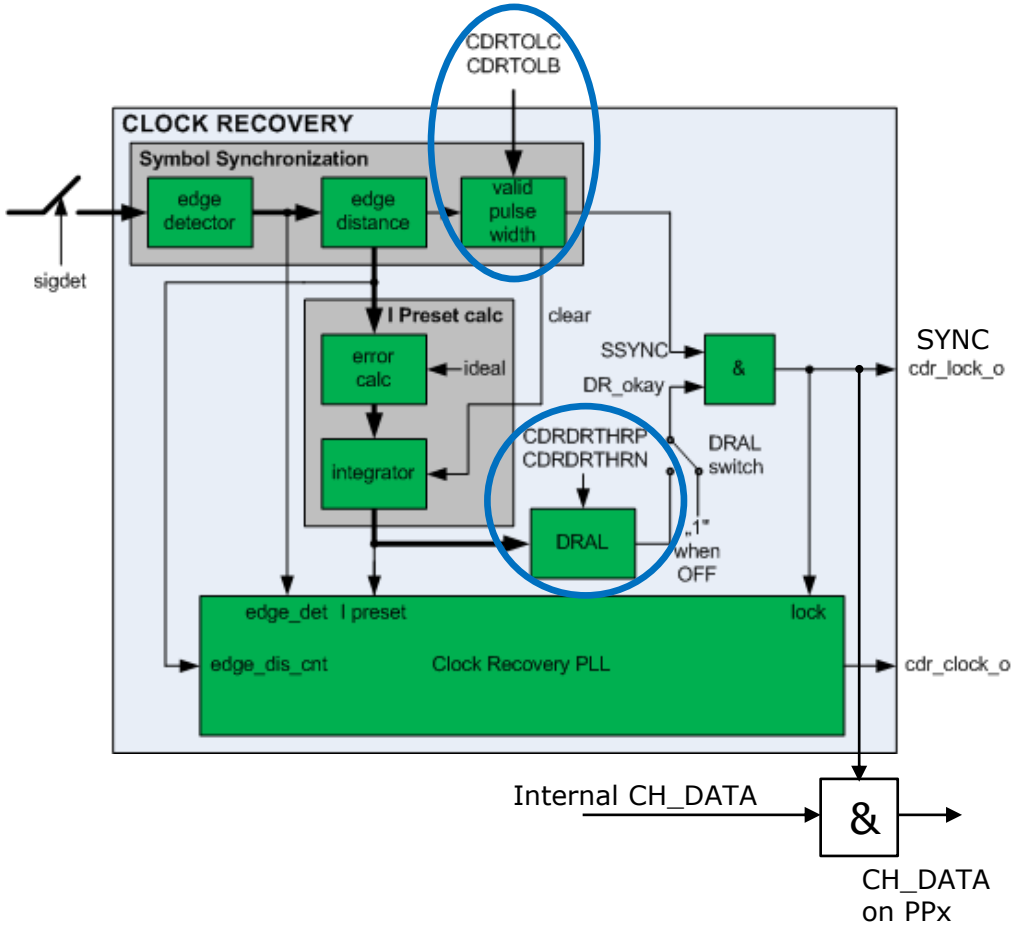
Block diagram of Clock Recovery (CR)

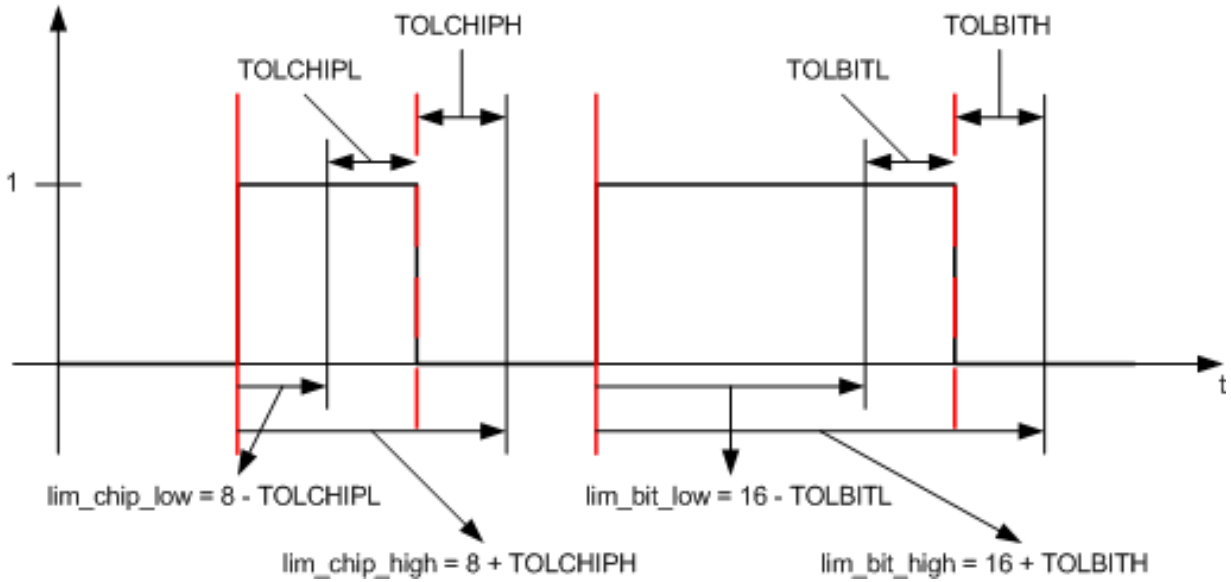
Two blocks can be used for narrowing the acceptance range of the received data rate:

- "**Valid Pulse Width**" function (x_CDRTOLB and x_CDRTOLC registers)
- **DRAL** function (CDRDRTHRP and CDRDRTHRN registers – see also previous pages)



Information: Input to CDR has ideally 8 samples per chip and 16 samples per bit
-> for 0% data rate error, ideal duty cycle and no noise.

Allowed CHIP and BIT Widths Configuration in TDA5235/40 (using "Valid Pulse Width" Function)



Default configuration of CDRTOLC and CDRTOLB registers:

- TOLCHIPL = 4
- TOLCHIPH = 1 → x_CDRTOLC=0x0C
- TOLBITL = 6
- TOLBITH = 3 → x_CDRTOLB=0x1E
- allowed CHIP = 4…9 samples (ideal=8)
- allowed BIT = 10…19 samples (ideal=16)

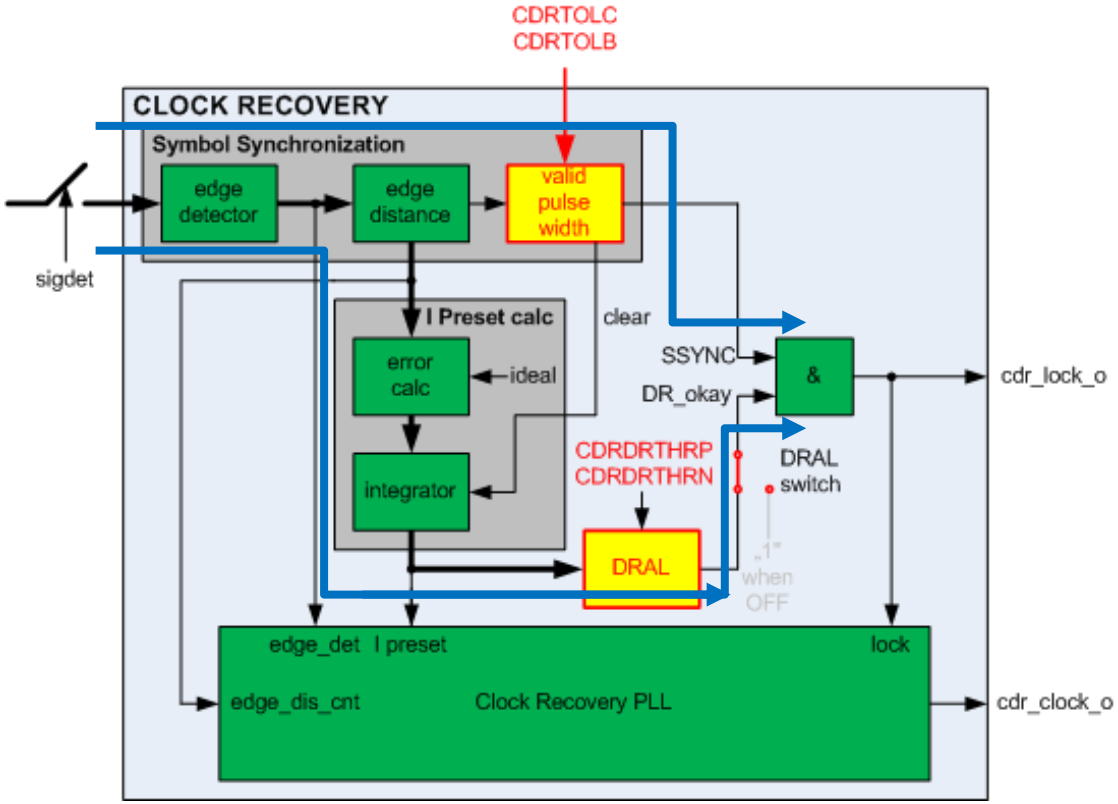
➔ Very **broad** range of accepted datarate(DR) of typical +/-25..30% in case DRAL=OFF

NEW configuration of CDRTOLC and CDRTOLB registers:

- **TOLCHIPL = 2**
- TOLCHIPH = 1 → x_CDRTOLC=0x0A
- **TOLBITL = 3**
- TOLBITH = 3 → x_CDRTOLB=0x1B
- allowed CHIP = **6**…9 samples (ideal=8)
- allowed BIT = **13**…19 samples (ideal=16)

➔ **NARROW** range of accepted datarate(DR) of typical +/-15..20% in case DRAL=OFF

Solution for Self Polling Mode (SPM) **ONLY**



Valid Pulse Width:

x_CDRTOLC=0x0A

x_CDRTOLB=0x1B

DRAL:

x_CDRRI.bit2=1 (**DRAL=ON**)

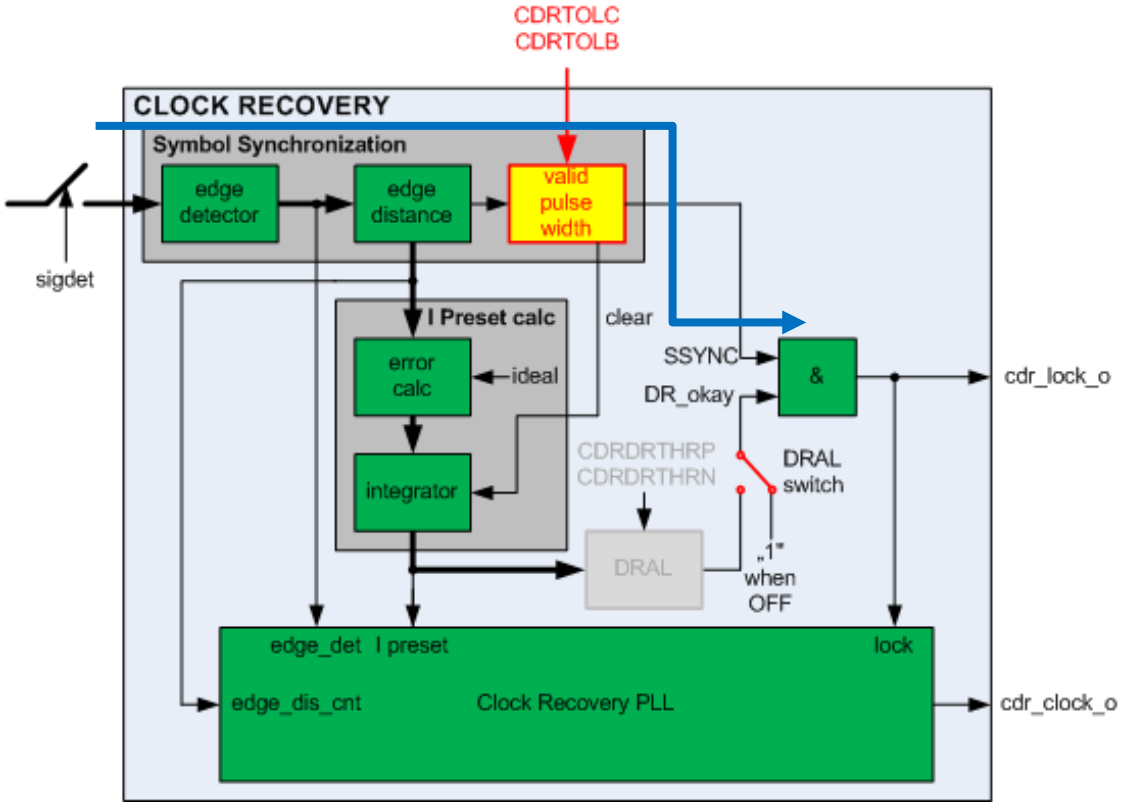
CDRDRTHRP=30dec=0x1E

CDRDRTHRN=35dec=0x23

(Do NOT use tighter DRAL limits than chip default values)

- **CONCLUSION for SPM only:**
  - Both blocks, "CDRTOL pulse width validation" and "DRAL", can be used to achieve required rejection of unwanted data rate
    - NARROW range of accepted data rate of typical +/-8..10% can be achieved in this case

Solution for Run Mode Slave (RMS)



Valid Pulse Width:

x_CDRTOLC=0x0A

x_CDRTOLB=0x1B

DRAL:

x_CDRRI.bit2=0 (**DRAL=OFF**)

CDRDRTHRP=30dec=0x1E

CDRDRTHRN=35dec=0x23

- **CONCLUSION**
  - Only "CDRTOL pulse width validation" block may be used for rejection of unwanted data rate
    - Range of accepted data rate (DR) of typical +/-15..20% can be achieved in this case

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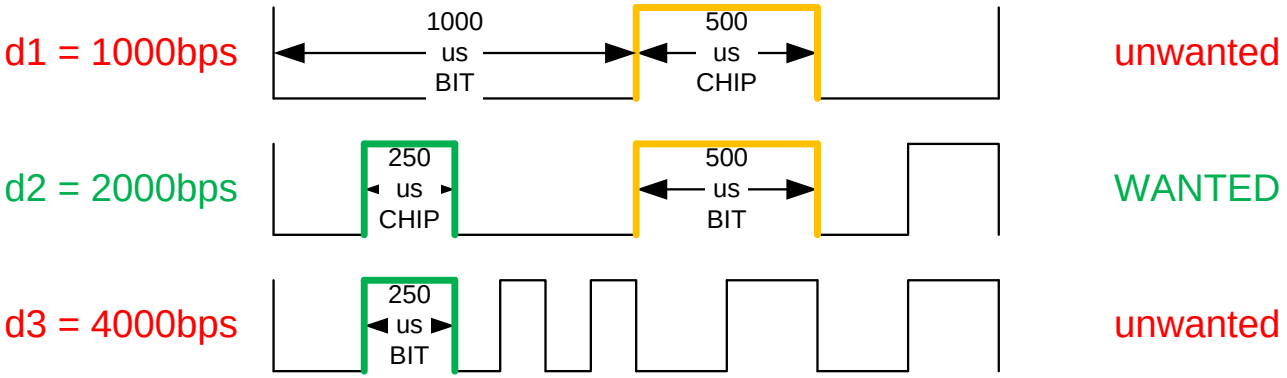
Unavoidable Ambiguity of Datarates with Respect to CDR Tolerances (Datarate/2 and Datarate*2)

Example 2000bps (BiPhase-Space):

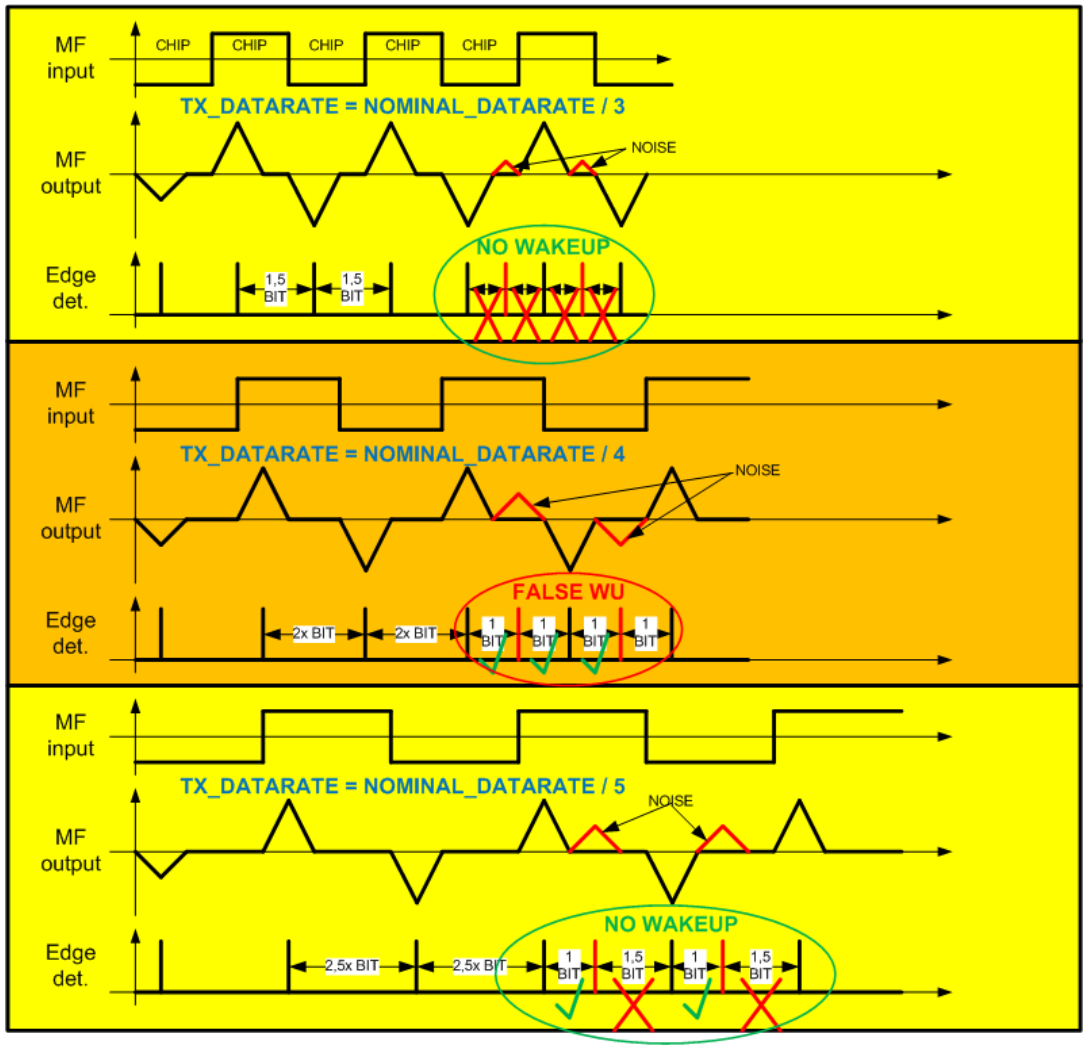


	short pulse length (chip)	long pulse length (bit)
d1 = d2 / 2 = 1000bps	500 us	1000 us
d2 = nominal = 2000bps	250 us	500 us
d3 = d2 * 2 = 4000bps	125 us	250 us

Conclusion

- Chip length of data rate d1 is the same as bit length of nominal data rate d2
- Bit length of data rate d3 is the same as chip length of nominal data rate d2
- **Both cases can pass through CDR tolerance window evaluation**

Avoidable FALSE WU at Sensitivity Level for Datarate / 4 (I)



CONCLUSION

False WU will happen around Nominal_Datarate / 4 close to sensitivity level if only "WU on SYNC" (very weak WU criterion) is used ➔ for solution see next slide

Avoidable FALSE WU at Sensitivity Level for Datarate / 4 (II)

As can be seen from previous page a weak unwanted signal around 250bps + Noise appear most likely like bits of wanted signal, which may cause "WU on SYNC", if "WU on SYNC" is used as only WU criterion.

SOLUTION (important!):

Use a stronger WU criterion ➔ "WU on Random Bits" (or "WU on Equal Bits") must be additionally used to avoid false wakeups

➔ Use "External Data Processing" mode = "No Deactivation of Functional Blocks" (Explorer Wizard page1)

Note: In "External Data Processing" mode "Chip Data" (CH_DATA processed by application controller) the WU criteria "WU on Random/Equal/Pattern" (strong) are automatically mapped to "WU on Sync" (weak).
This weak Wakeup criterion can lead to false alarms (Wakeup interrupt is generated by TDA5240/35 and application controller gets activated) and will increase the average current consumption.

For your information: No FALSE WU will occur at good input power level for Datarate/4, because the strong unwanted signal around 250bps without Noise does not appear like bits of wanted signal.

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Recommendations for Application Verification Tests at the Customer

Following verification tests should be done by the customer on the customer module (typically using an automated test environment):

- Verify all parameters specified by your customer
- Verify sensitivity over all relevant parameter tolerances, e.g.:
  - Datarate
  - FSK deviation / ASK modulation depth
  - RF frequency offset between transmitter (TX) and receiver (RX) unit
  - Temperature
  - Bi-phase duty-cycle
  - Supply voltage
- Apply Missed Message Rate (MMR) tests,
  - where TX frame is sent repeatedly (e.g. 10000-times) at a "good" RF level (e.g. -80dBm) and finally all transmissions must be received correctly
  - This is very helpful for verification of SelfPollingMode (SPM) use-cases
- Apply False Alarm Rate (FAR) tests (especially for SPM use-cases),
  - where no transmission is initiated, and therefore no Wake-up is expected during SPM (e.g. use NINT source Wake-up)
- Verify reception over desired dynamic range of receive RF power level over all relevant parameters (incl. larger RF levels)
- Verify EMC behavior
- Verify fulfillment of regional regulations (FCC, ETSI, ..)
- Verify behavior in presence of interfering signals (also known as "blocker measurements").
  - Source can also be the own application µC or other critical components on the PCB.

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Revision History

- V1.0: Initial Version

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