

# Simulation with PSpice

Automotive MOSFETs and Driver ICs

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Automotive Power



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## 1 Abstract

This Application Note presents a way how to simulate a typical high current EC motor drive power stage using PSpice.

Starting with an explanation how to use the MOSFET and driver IC PSpice models, what they are capable for an example of a simulated EC motor drive will be presented. The simulation is based on common requirements for automotive applications.

As a result, a ready-to-use circuit model is obtained which allows the analysis and the re-design of the power stage later on. The simulation results are compared with measurements performed on an evaluation board.

## 2 Introduction

Powerful electric motors to drive fuel pumps and water pumps, cooling fans and HVAC blowers, deliver steering assist and shift gears find their way into modern cars.

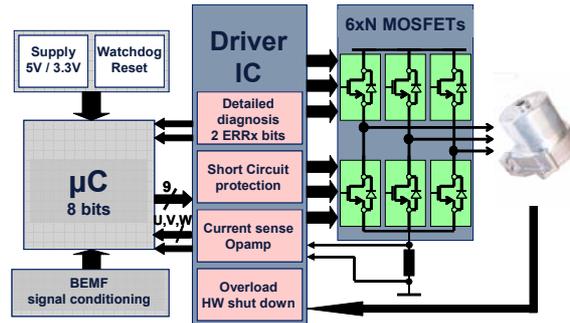
The motivation to move away from belt-driven solutions to electrically actuated solutions may include increased fuel economy, vehicle installation and packaging constraints, increased feature set, safety and/or convenience, simplified assembly and modular testability prior and during vehicle manufacturing.

The electric motors are in most cases DC brush motors or EC motors, which are electronically commutated. Usually, they are operated on the 12 V power net and draw between 0 and 100 Amps – depending on demand, application and OEM. The power electronics of the motor drive consists of a Driver IC, one, two or three MOSFET half bridges and passive components. MOSFETs and Driver ICs are chosen to meet the electrical requirements, primarily the voltage and current levels, package size, reliability targets, thermal and cost constraints etc. But even within one specific application, the operating conditions may vary a lot between customers (model types), e.g. the supply voltage range, the current level, the ambient temperature, acceptable EMI levels etc.

Hence, several hardware setups may be required that have to be designed, assembled, tested, and re-designed. One approach that can help reducing hardware design and test efforts, cost and cycle times during the development process is state-of-the-art circuit modelling and simulation. Especially when a known circuit is already modelled and the model is verified with real measurements the impact of circuit modifications can be analyzed by simple means. These modifications may include replacement of components, component variations, changes of the circuit layout or the boundary conditions, e.g. the supply voltage. Modelling and simulation also helps to get a better understanding of components and circuits. Depending on the models, simulation may even allow to look insight components, to measure circuit properties which are hardly accessible and process this data in a convenient manner. This way, smart predictions of the circuit's behaviour can be obtained as a response to circuit modifications before these changes are implemented.

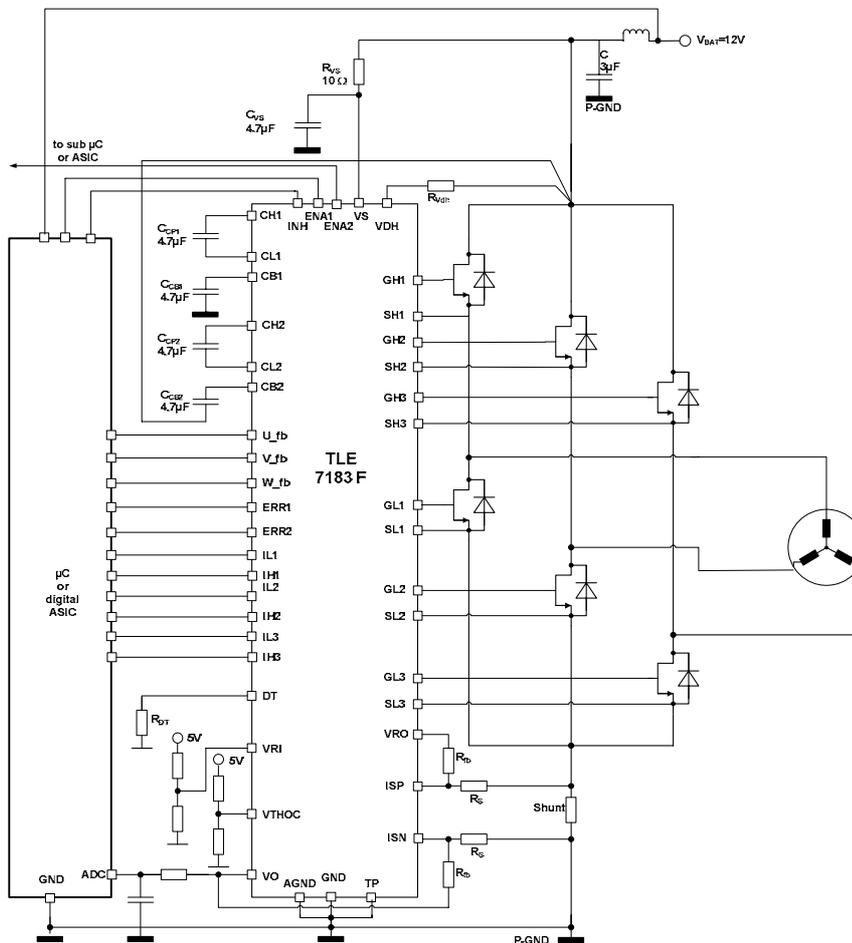
## 3 EC Motor Drive

A simplified block diagram of a 3-Phase Motor Drive is shown in Figure 1. This motor may drive a pump or fan in the car and is in this case an EC motor – the commutation is electronically performed by the 6 N-Channel Power MOSFETs which form the inverter. The MOSFETs are driven by a 3-Phase Driver IC which is controlled by a  $\mu\text{C}$  which generates the PWM patterns for the 3 half bridges. The PWM patterns are chosen in a way that they result in the desired motor current wave forms.



**Figure 1: Simplified block diagram showing EC motor, the power stage and the control**

Besides the power stage a communication interface may be present in the system to exchange status information of the motor drive unit or to receive set-point information, e.g. pressure or speed. In addition, several properties within and / or outside the EC motor drive may be sensed and monitored, e.g. motor current, pressure, rotor position, torque. This requires sensors, voltage supply for the sensors, and conditioning of the sensor signals. A microcontroller is the brain of the system, generates the required PWM patterns to control the motor current and speed. This may be based on rotor position signals, sensorless by monitoring the BEMF or based on more sophisticated methods to accommodate to low speed operation or



brushless motors with sinusoidal flux distribution. The 6 power MOSFETs are key elements of the power stage and form – together with passive components - the inverter, pls. see Figure 2. They are the switches and apply either battery voltage, GND or none of the two to the motor windings. To control the current of the motor windings in an analogue manner (commonly between 0 and 100 Amps), their ON and OFF times or duty cycles are pulse width modulated at about 18 – 23 kHz. That demands for low  $R_{DSon}$  MOSFETs, reasonable low gate charge to facilitate the switching behaviour, high DC current rating as well as low thermal resistance.

The Driver IC, Infineon TLE7183F, level shifts, amplifies, and buffers the control signals coming from the  $\mu C$  to provide the gate charge for the High Side and Low Side MOSFET. The Driver IC incorporates also circuits (charge pumps) that allow operation at low battery voltages or other extreme application conditions, e.g. short or long Duty Cycles.

**Figure 2: Simplified circuit diagram showing close-up of the Driver IC and 6 power MOSFETs**

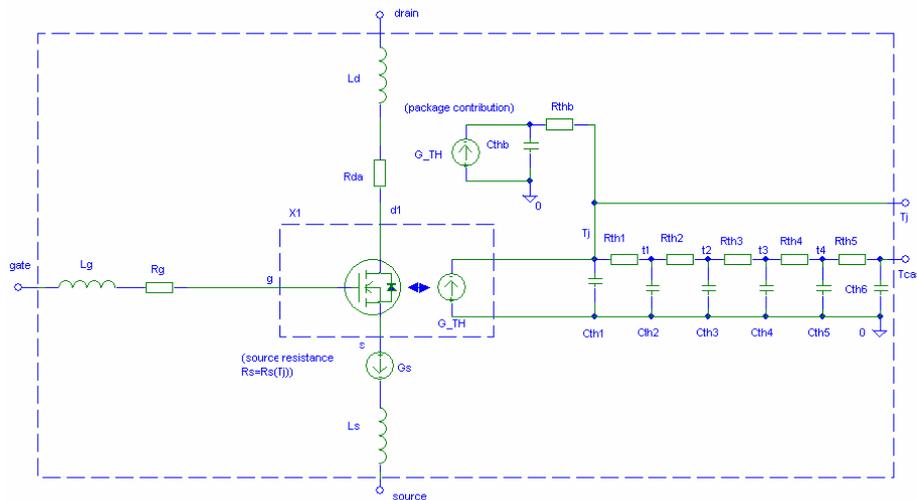
## 4 PSpice Simulation models

PSpice is a commonly used simulation tool. Even the free download version is capable to simulate simple circuits with Infineon MOSFETs, which are available on the Infineon homepage in the Internet. For a first best guess on power losses and junction temperatures good results can be achieved.

### 4.1 MOSFET models

Infineon provides different types of models for MOSFET devices. Level 1 and level 3 types are based on a physical temperature-dependent model of the MOSFET structure and the package. Level 1 models assume a constant device temperature for the entire circuit and during a transient simulation (the temperature is to be given in the Analysis Setup).

In order to be able to compute the self-heating dynamically, the electrical model is coupled with a thermal model of the device in Level 3 models. To do this, the current power dissipation in the transistor is determined permanently, and a current proportional to this power is fed into the thermal equivalent network. The voltage at the Tj node then contains the information about the time-dependent junction temperature which in turn acts directly on the temperature-dependent electrical model.



**Figure 3: Infineon MOSFET model**

Level 3 models have two external thermal nodes: First, there is Tj, where the user can monitor the junction temperature easily. Usually, this node should not be connected. However, when the computation should start with a device junction temperature different to the thermal equilibrium, connecting Tj with a small capacitor (typically 1pF) to ground and stating an initial value (parameter IC) for the initial potential difference (which is used as a measure for the initial temperature in °C) enables these types of simulations. The second thermal pin is Tcase (in TO packages). This pin has to be connected. An external resistor-capacitor-network can be added between the Tcase pin and ground. The right-hand-side terminal of the heatsink RC-network has to be connected to a voltage source which represents the ambient temperature. On the other hand, connecting the ambient temperature source directly to the Tcase pin leads to a network where optimum heat transfer is modelled.

Figure 3 shows the equivalent circuit diagram on a Level 3 model of an Infineon MOSFET. The inductances and resistors connected to the MOSFET die itself represent the impedance of the interconnects of the die to the package (e.g. bond wires). The R/C network models the thermal impedance of the device which is coupled via current sources to the MOSFET and the package. With that approach selfheating effects can be simulated and a precise estimation of the junction temperature could be achieved.

The Infineon MOSFET PSpice models can be found in the Internet: [www.infineon.com](http://www.infineon.com)

### 4.2 Driver IC model

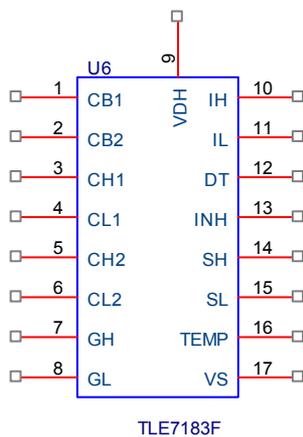
In addition to the MOSFET models, a driver IC model is needed to be capable to simulate the power stage of a motor drive circuit.

Infineon is offering a broad spectrum of driver ICs. Out of that portfolio the TLE7183F, a commonly used, state of the art 3 phase driver IC especially in Electrical Power Steering applications, was chosen for the simulation. To simplify the simulation, the behavioural PSPICE model is stripped down to one half bridge only,

Following properties are implemented in the simulation model:

- Control inputs for the MOSFETs (pins 10, 11) and propagation delays
- Shoot through + dead time function (pin 12)
- Charge Pump 1 and 2 (pins 1 to 6)
- Output stages for one high side (pins 7, 14) and one low side MOSFET (pins 8, 15)
- INHhibit function (pin 13)
- Temperature setting (pin 16)

For the detailed specification of the driver IC please refer to the data sheet published on the Infineon homepage.



As one highlight of the driver IC the integrated charge pump will be investigated in the following in more detail. The motivation of integrating two charge pumps base on the unstable battery voltage in an automotive surrounding. Yet, the EC motor drive could operate at low battery voltages, e.g.  $V_s = 5.5\text{ V}$  for instance in a fuel pump system. While it is demanding to operate the Driver IC at 5.5 V, it is even harder to drive the MOSFETs at this low voltage as Standard level MOSFETs are commonly used which require at least 7 ... 8 V Gate-Source Voltage  $V_{GS}$ . Hence, the Driver IC boosts the battery voltage  $V_s$  to generate it. This is done by a regulated charge pump which is integrated into the Driver IC; the output voltage of this first charge pump is  $V_{CB1}$  (pls. see also Figure 2). A second regulated charge pump is daisy chained to generate an even higher voltage to drive the High Side MOSFETs (its output is  $V_{CB2}$ ) – at almost all battery voltages and extreme Duty cycles, e.g. several tens of seconds on-time of the High Side MOSFET. This gives full freedom in terms of PWM patterns and operating range when driving the EC motor.

Figure 4: Infineon Driver IC model

Figure 5 shows the available Gate-Source-Voltage on the MOSFETs – provided by the Driver IC - as a function of the Supply voltage  $V_s$  (battery).

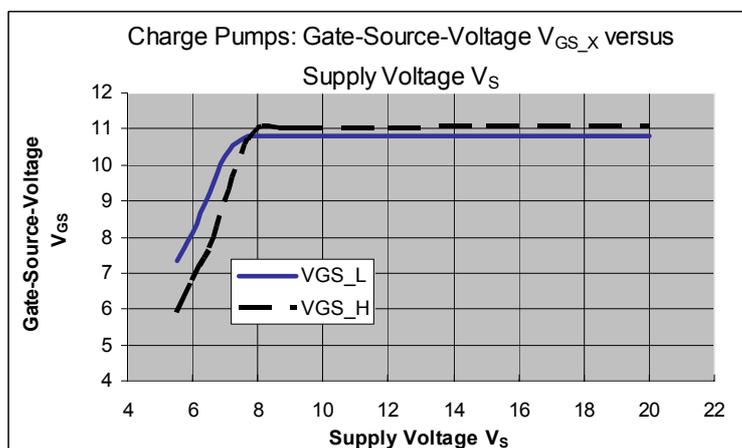
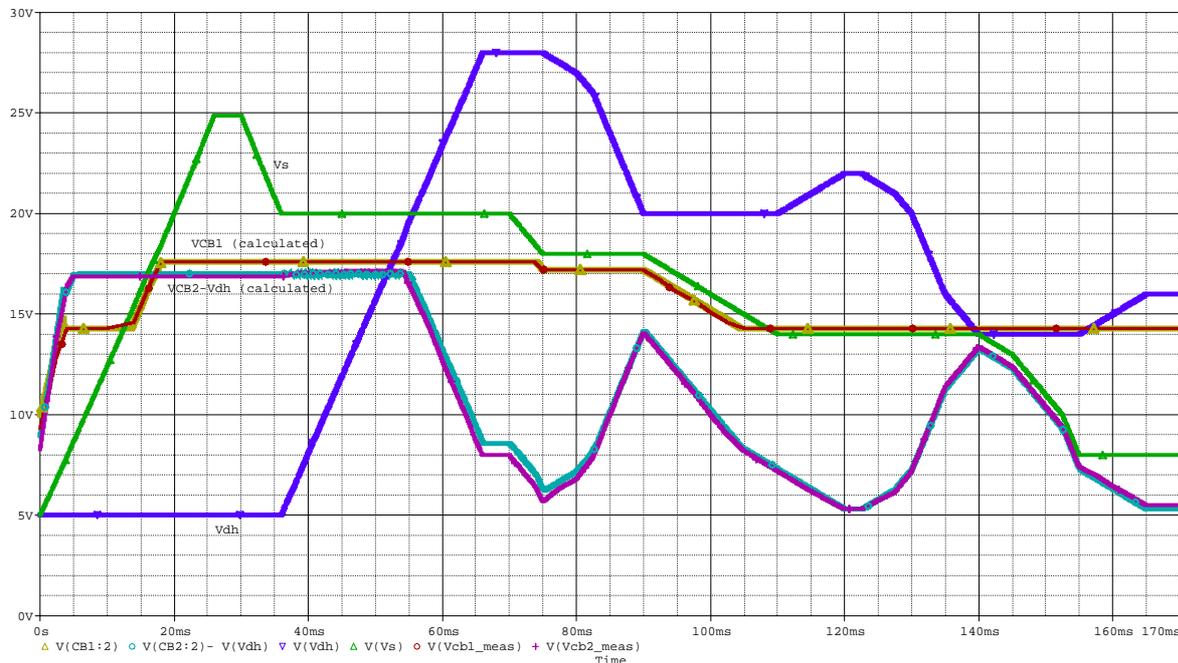


Figure 5: Gate-Source-Voltage delivered by the Driver IC TLE7183F versus supply voltage  $V_s$

In order to verify the essential function of the charge pumps in the model, the Driver IC was exposed to a sweep of the supply voltage  $V_S$  and the voltage  $V_{DH}$  (= voltage on the drain of the high side MOSFETs, pls. see Figure 2) and the output voltages of the two charge pumps – CB1 and CB2 - were measured. The voltage  $V_{DH}$  was varied independently from  $V_S$  as the voltage across the three half bridges may sometimes differ from the supply voltage  $V_S$  applied to the Driver IC. The MOSFETs were not switched during this measurement; the result is depicted in Figure 6.

Supply voltage  $V_S$  (green) and voltage  $V_{DH}$  (blue) are plotted versus time to improve the readability (although the nature of the manual voltage sweep is in fact a DC measurement). The resulting output voltages of charge pump 1 (red, ref. to GND) and 2 (pink, ref. to voltage  $V_{DH}$ ) is plotted versus time, too. These two charge pump voltages are the 'supply voltages' of the Driver IC's output stages which drive the MOSFETs.

The Driver IC model was simulated under the same boundary conditions; the simulated charge pump 1 voltage (yellow, ref. to GND) and charge pump 2 voltage (light blue, ref to  $V_{DH}$ ) are appended to the measurement results in Figure 6.



**Figure 6: Comparison of simulation and measurement - voltages of the charge pumps versus  $V_S$  and  $V_{dh}$**

The results are almost identical. It can be concluded that the model of the charge pumps behaves like the ones of the real component. Furthermore, the Driver IC delivers a proper Gate-Source-voltage under varying supply conditions.

With that short introduction of the driver IC model the next step would be to combine that model with the MOSFET models and investigate the behaviour of the complete power stage.

## 5 EC Motor Drive: Modelling of the power stage

The simulation of the power stage is based on an existing 3 phase demonstration board as shown in Figure 7. Main challenge of a simulation on ECU level is to consider not only the physical components itself (meaning the MOSFETs, the capacitors, inductors etc) but focus as well on the parasitic components of the board and its components, e.g. parasitic capacitances and inductances.

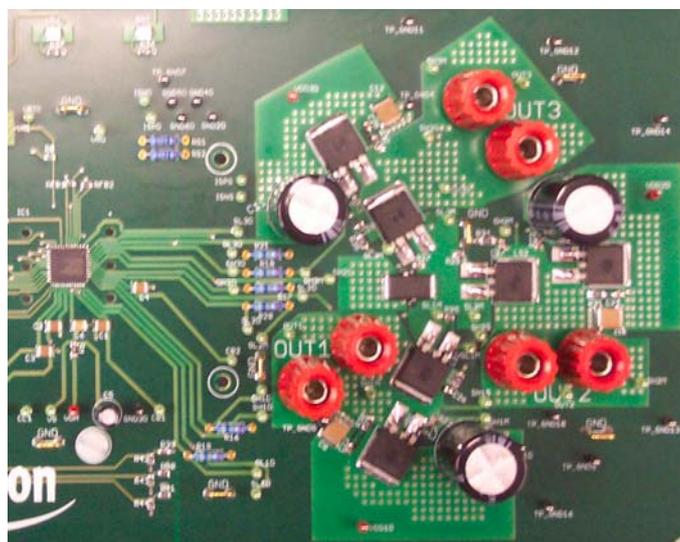
Any capacitor should be modelled with its capacitance value  $C$ , its equivalent series resistance ESR, and the equivalent series inductance ESL – the three components should be placed in series; the insulation resistance and the dielectric absorption can be neglected in most cases.

The resistors of the power stage can be represented by the resistance value  $R$  and a series inductance; the inductance value increases with size and physical construction and can be neglected for small SMD resistors.

One more “component” should be accounted for when modelling a high current ( $> 10\text{ A}$ ) and low voltage ( $12\text{ V}$ ) application: The parasitic stray inductances within the wiring of the PCB / ceramic substrat. Although, these stray inductances are not implemented by physical components they are still present in the real circuit. Stray inductances must be considered in any current path in which the rate of change of the current is high, namely in the commutation loop of the current where  $di/dt$  exceeds  $100\text{ A}/\mu\text{s}$ ; stray inductances of the high current path going to the motor winding can be neglected as the much larger motor winding’s inductance is in series. The values may range between several nH to several tens of nH.

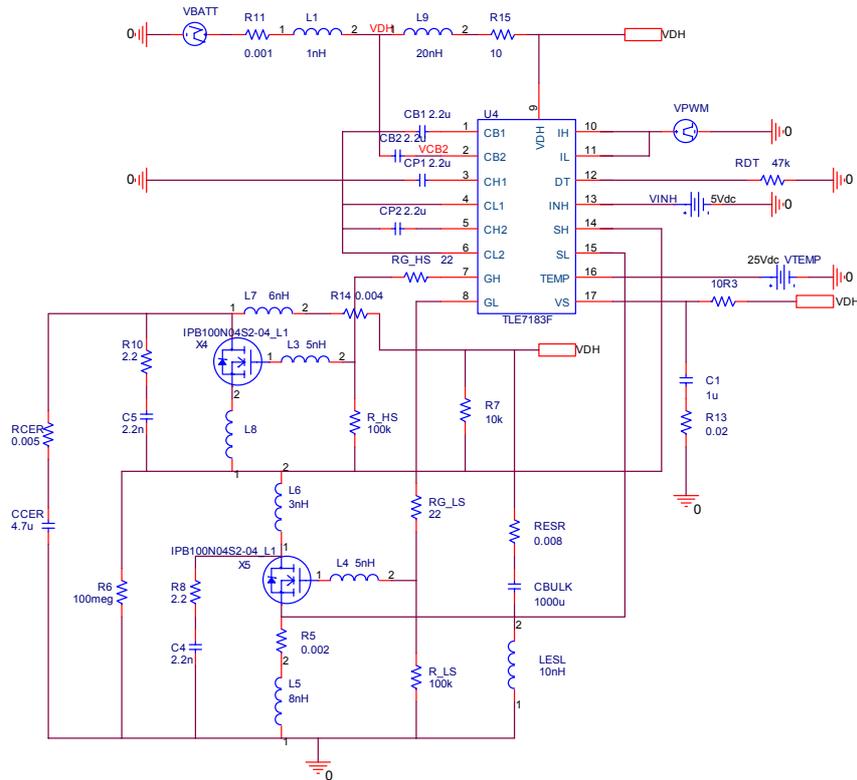
One way to estimate the stray inductances of an existing circuit is the measurement of voltage drops across the pcb track of interest; the measurement requires very fast differential voltage probes and must be performed while the current commutates from high side to low side MOSFET or vice versa ( $L=V*dt/di$ ). Alternatively, the oscillation frequency of the voltage on the MOSFETs right after the switching event can be evaluated to conclude the sum of the stray inductances within the commutation loop (based on the MOSFETs output capacitance at the operating point). In addition, smart guesses based on previous designs or estimations based on track length and width plus rule of thumb may help. Most promising is a combination of the several techniques.

On the other hand, the simulation model of the power stage of the 3 phase demonstration board, shown in Figure 7, can be simplified: The 3 half bridges use the same components and the same component values. Furthermore, the layout of the 3 half bridges is very similar. Hence, the parasitics of one half bridge is very similar to the parasitics in the other onse. This means, modelling and simulating one half bridge is sufficient in order to analyze behaviour that is common to all three half bridges, e.g. current or voltage waveforms, power loss etc. Therefore, rather than modelling 3 half bridges only a one half-bridge-Driver IC and one half bridge (2 MOSFETs, including passive and parasitics) is modelled. This saves not only time during the modelling, but also reduces time and amount of simulation data during the simulation and the analysis of the results.



**Figure 7: 3 phase demonstration board**

The entire PSPICE model of the power stage is given in Figure 8.



**Figure 8: PSpice model of one leg of the demoboard**

The circuit model can be simulated now and the results can be compared to measurements performed on the evaluation board shown. The initial simulation results are used to verify the circuit model; if there the simulation results significantly differ from the measured results, the model needs to be adjusted.

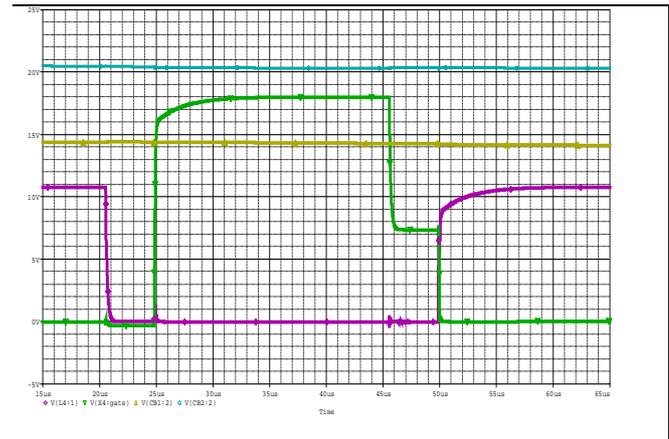
The initial PSPICE simulation settings are as follows:

- Transient analysis  $t_t = 50 \mu s$
- Step size  $t_s = 20 ns$
- Several 'Options' settings to facilitate convergence (ITL1, 2, 4 = 150; RELTOL = 0.01, ABSTOL = 1 nA, CHGTOL = 1 pC)

For this measurement and simulation the operating conditions are:

- Supply voltage  $V_s = 14 V$
- Frequency = 20 kHz
- Load current = 17.5 A with R-L-load (current flow from load into half bridge)
- Temperature = 25 °C
- 'Typical' MOSFET parameters
- Gate resistors  $R_g = 22 \Omega$
- Dead time setting about 700 ns (high side and low side MOSFET controlled by a single PWM signal)

The result of the first simulation allows the verification of the charge pump voltages (DC voltages), CB1 and CB2, as well as basic transient voltages (Gate-Voltages); it shows one simulated switching period in Figure 9 (right) and is compared to a result of a measurement (left).



**Figure 9: DT pin open (max. dead time),  $R_g=4.7\Omega$ ,  $V_s = 8\text{ V}$  (left: measurement, right: simulation)**

Figure 9 depicts the output voltage of charge pump 2 (blue, ref. to GND), the output voltage of charge pump 1 (yellow, ref. to GND), the Gate-Source-voltage of the low side MOSFET (pink), and the Gate-voltage of the high side MOSFET (green, ref. to GND).

A comparison of the 2 simulated output voltages of the charge pumps, blue and yellow, with the two measured output voltages of the charge pump voltages reveal, that the voltage levels are very similar and the modelling of the charge pumps is satisfying. The Gate-voltage wave forms (green and pink) of the simulation match also the measured ones in terms of level and timing. This indicates that the dead time between high side and low side was properly modelled for long dead times ( $4.5\text{ }\mu\text{s}$  typ. when the dead time pin DT is open) and that the output stages in the model deliver the correct Gate-voltage level.

The first measurement and simulation has been performed without load current so far. The next step is a check by applying a load to the half bridge, in this case an R-L-load. Measurement and simulation results need to be compared again. A significant mismatch of the results under load is unlikely to occur, except during fast switching transients. If this is the case, the distribution and values of the stray inductances in the power stage model or the MOSFET model (capacitances, inductances) need to be adjusted.

For this measurement and simulation the operating conditions are:

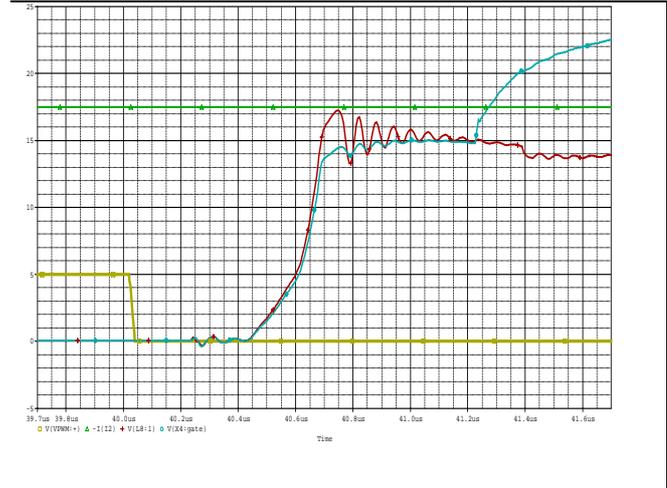
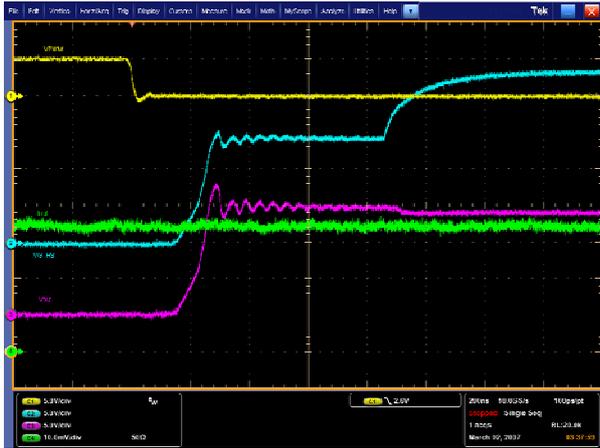
- Supply voltage  $V_s = 14\text{ V}$
- Frequency =  $20\text{ kHz}$
- Load current =  $17.5\text{ A}$  with R-L-load (current flow from load into half bridge)
- Temperature =  $25\text{ }^\circ\text{C}$
- 'Typical' MOSFET parameters
- Gate resistors  $R_g = 22\text{ }\Omega$
- Dead time setting about  $700\text{ ns}$  (high side and low side MOSFET controlled by a single PWM signal)

Figure 10 shows the PWM input signal (yellow), the output voltage (blue, measured on the Source of the high side MOSFET, ref. to GND), the Gate voltage of the high side MOSFET (pink, ref. to GND), and the load current (green,  $5\text{ A / div}$ ).

The voltage levels, the timing of the high side MOSFET's gate voltage, and the amplitude and frequency of the oscillations on the output voltage (= source of the high side MOSFET) are within acceptable tolerances. Out of the voltage over shoot and the oscillation characteristic (amplitude and frequency) one can conclude that the stray inductances and capacitances of the commutation loop are in the right range.

However, it can be seen that the propagation delay is not correctly modelled. It needs to be decrease by approx.  $250\text{ ns}$ ; this is done within the model of the Driver IC.

After adjusting the propagation delay of the Driver IC, the model is ready to use for investigating and optimizing the circuit.



**Figure 10: Comparison of simulation and measurement – Gate and output voltage at 17.5 A load current**

## 6 Conclusion

This application note gave an introduction into the applications and requirements of EC motor drives in automotive environments. The power stage components of an EC motor drive have been presented and an overview of their PSpice simulation models has been given. A sample power stage model was presented and verified and its usage was demonstrated.

**Edition 2008-03-26**

**Published by Infineon Technologies AG,  
Am Campeon 1-12,  
85579 Neubiberg, Germany**

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