ESD101-B1 / ESD103-B1

Bi-directional Ultra Low Capacitance Transient Voltage Suppression Diodes for High Power RF Applications

Application Note AN327

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RF and Protection Devices

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Table of Content

List of Figures

List of Tables

1 Introduction

1.1 Basics of Transient Voltage Suppression (TVS) Diodes

ESD protection devices are strongly nonlinear. Their characteristic is split into a working area, where devices act as “open” or “isolator”, and a protection area, where devices act as a “short” or “conductor”. Basic characteristic of a uni-directional ESD protection device including snap-back is shown in Figure 3 with some abbreviations in common use.

Physical principle of silicon based TVS diodes is the Zener or avalanche process wich drives the diode from an open into a short state, when operating voltage exceeds diode breakdown / trigger voltage V_{Trig}. Silicon based TVS diodes offer following advantages over other approaches (MOV, MLV, polymer-based devices):

- Both uni-directional (Figure 1) and bi-directional (Figure 2)structures are available
- R_{dyn} can be kept very low even at low device capacitance
- Low trigger voltage, low “first overshoot” lasting only about 1ns
- Performance stable device, no degradation in leakage current performance even after multiple ESD strikes
- Best ESD protection performance for high speed applications in the GHz range as well as for low frequency applications

A single uni-directional TVS diode structure is designed for a wanted signal between ~0V and “maximum working voltage” specified for the TVS diode. In case of a negative signal is applied between signal line and GND, the device will become conductive if the signal level exceeds about minus 0.5V (see Figure 3). Such a device can i.e. be used to protect a unipolar digital data signal (Figure 1).

In order to protect bipolar signals, i.e. signals providing both positive and negative voltage values, a bi-directional TVS device is needed (Figure 2). The V-I curve of such device is symmetrical with respect to the origin (Figure 4), and the ESD protection capability is granted for a positive AND a negative ESD strike in the same way. A bi-directional TVS diode can be created by using two identical uni-directional TVS diodes connected in series, as shown in Figure 6, or by integrating the bi-directional functionality in one die.

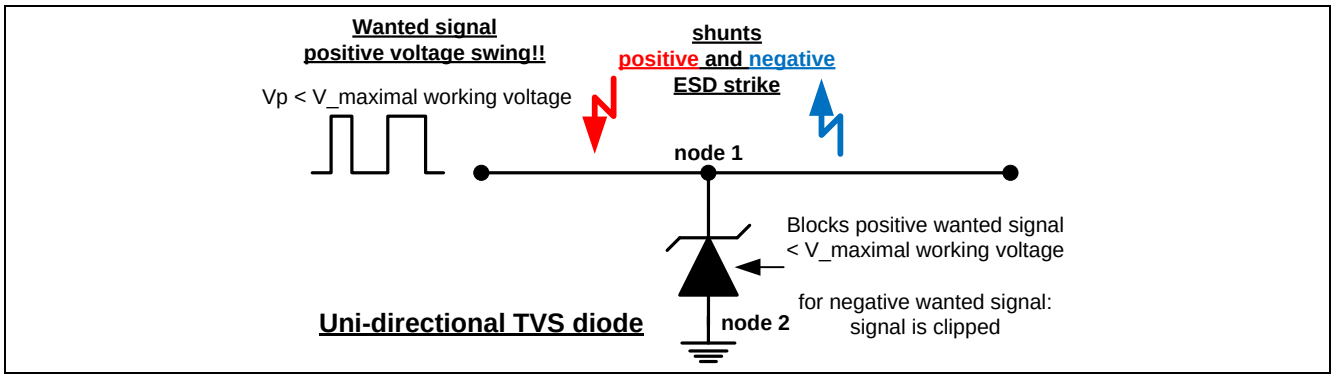

Figure 1 Typical application of the uni-directional ESD diode

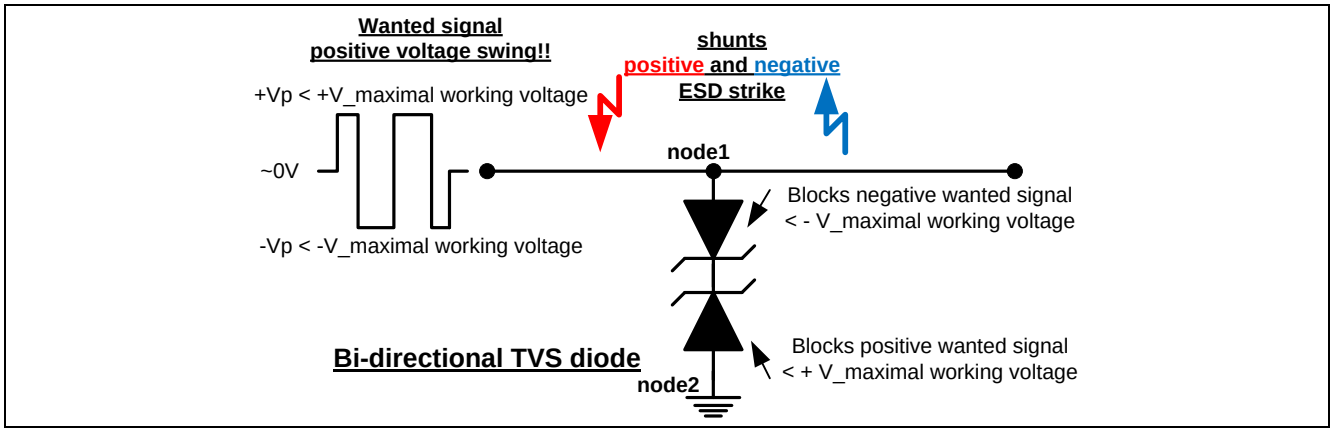

Figure 2 Typical application of the bi-directional ESD diode

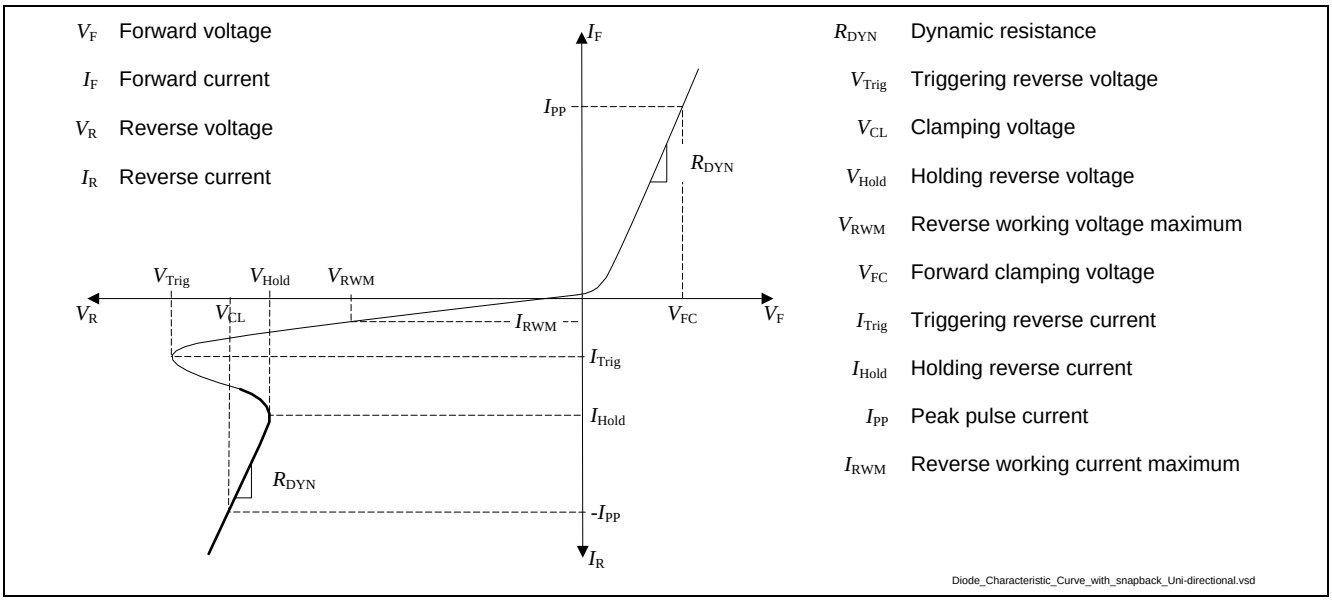

Figure 3 Principal characteristic of a uni-directional ESD protection device including snap-back

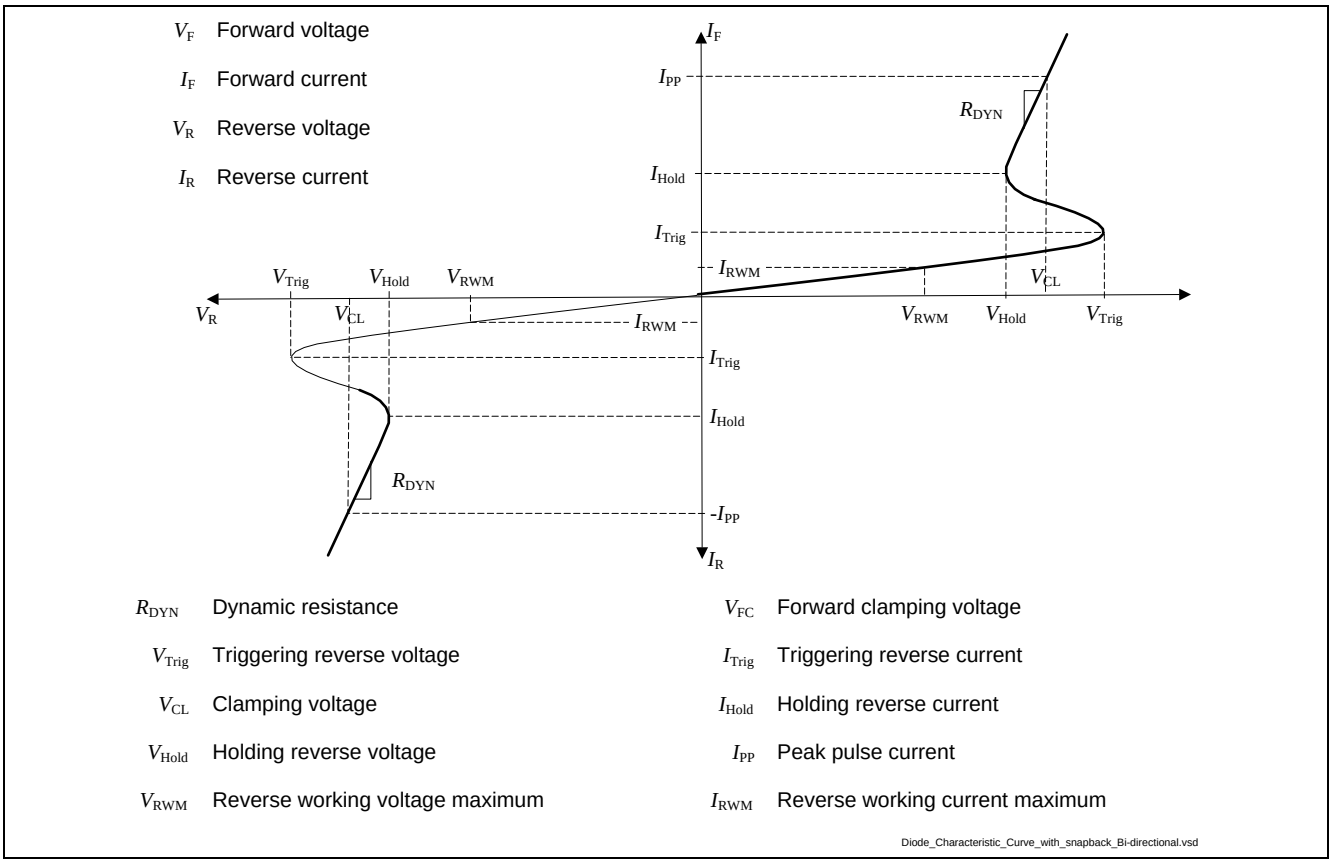

Figure 4 Principal characteristic of a bi-directional ESD protection device including snap-back

For ESD protection in RF application it is mandatory to keep the ESD diode capacitance as small as possible. This avoids a de-tuning of input matching structure and the protection device will create less harmonic distortion.The principle of minimizing the ESD diode´s capacitance is explained for a unidirectional diode (Figure 5) and extrapolated to the bi-directional type (Figure 6)

To control the overall device capacitance a low capacitance PIN diode (PIN1) is used in series to the avalanche (Zener) diode. When signal voltage is between 0V and V_{RWM} (positive), Zener diode is driven in reverse direction and is not conducting.Voltage drop across the PIN1 diode is about 0V or very little positive, diode is forward driven. Under this condition capacitance of the PIN1 diode depends on the diffusion current in forward direction which is equal to the leakage current of the Zener diode.This is also a reason the leakage current of the TVS diode must be kept as low as possible.

The described structure can handle a positive ESD strike only, because the PIN1 diode (serial to the Zener diode) can only hande the ESD current in forward direction. Driving the PIN1 diode in reverse breakthrough results in its damage. To make the ESD diode safe for the negative ESD strike as well, another PIN diode (PIN2) is added. In case a negative voltage, caused by an ESD strike or by an other reason, is applied to the signal line, PIN2 becomes conductive and shunt the negative voltage to ground (bypassing PIN1 and the Zener diode).

This kind of low-capacitance ESD diode construction can handle positive and negative ESD strikes, but is only suited for positive wanted signals. To handle positive and negative signals (e.g. a bias free RF signal) without distortion, the unidirectional ESD diode structure has to be expanded to a bi-directional structure. This can be done by adding the same structure serial in a flipped way. This approach is used in ESD101 and ESD103 design. 2 chips are placed in one package and connedcted by a chip to chip bond. To ensure linearity, both chips are matched in characteristic.

1.2 Requirements for Electrostatic Discharge Protection at RF

To protect a non-biased RF signal showing both positive and negative voltage swing, a bi-directional TVS diode is mandatory, as explained above. As for its other characteristics, at the radio frequencies the most important are parasitic parameters and linearity, as they influence strongly performance of the whole system.

In order to maintain device linearity at RF the “positive” and the “negative” diodes has to be identical in characteristic (good diode matching). Poor matching would lead to generation of even order harmonics (2, 4, 6…). However, even with good diode matching TVS diode still remains nonlinear device. Effects like nonlinear V-I characteristic, and even more importantly voltage dependent capacitance lead to harmonics generation and to intermodulation distortions.

The requirements to ESD protection diodes suitable for RF applications can be summarized as follows:

- Bi-directionality

- Low parasitics
  - Minimal capacitance
  - Absence of (self)resonanse, or resonance frequency much higher than working frequency
  - Low Insertion Loss

- High linearity in working frequency range
  - Even order harmonics (*H2,H4, ...*) as low as possible
  - Odd order harmonics (*H3, H5, ...*) as low as possible
    - Maximum harmonic generation is specified in various national/international standatds about electromagnetic compliance e.g. EN 300 328
    - By a rule of thumb maximum harmonic power at >1GHz of -30dBm must not be exceeded. Oftens customers have their own - more stringent - specifications based on dedicated requirements.

  - Low intermodulation distortion of 3-rd order (IMD3), especially in full-duplex systems (CDMA, UMTS, LTE)

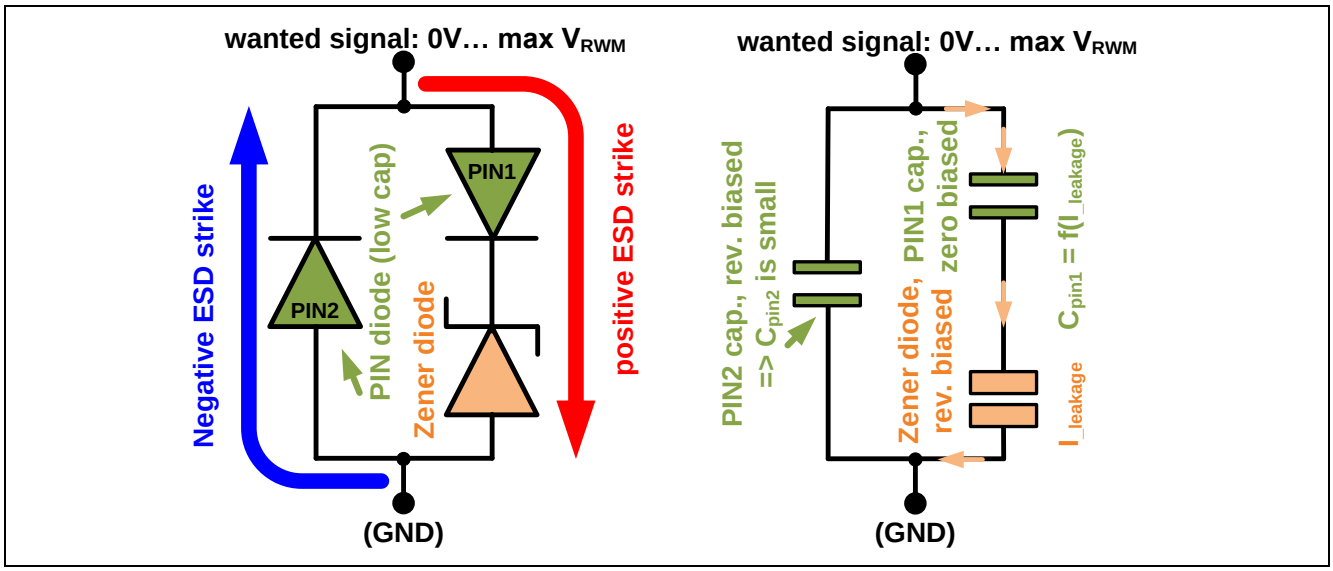

Figure 5 Operating principle of a low capacitance uni-directional ESD diode

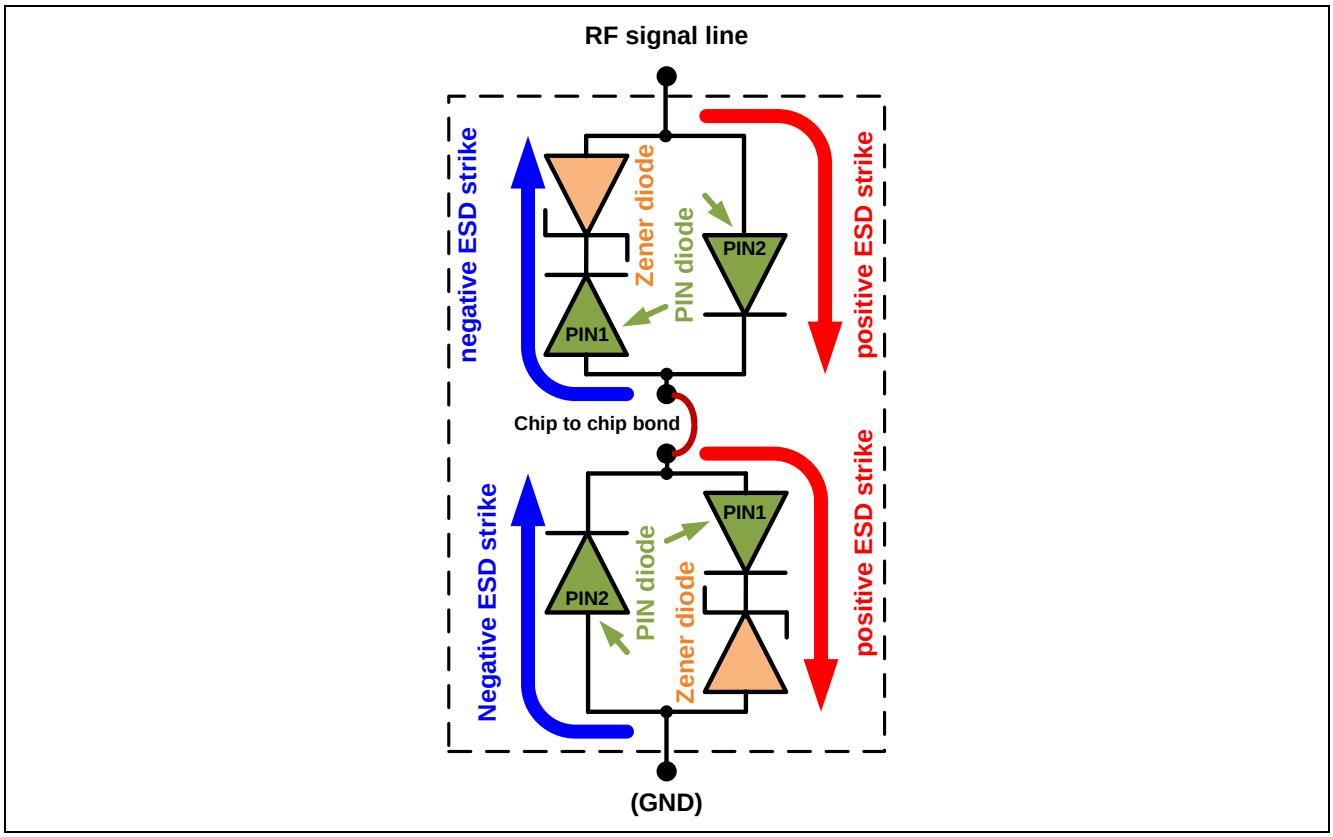

Figure 6 Bi-directional ESD diode, dedicated to protect RF lines

2 ESD101-B1 / ESD103-B1 Overview

2.1 Features

Table 1 Feature overview of ESD101-B1 / ESD103-B1

Feature	ESD101-B1	ESD103-B1
Maximum working voltage	V_{RWM} = ±5.5 V	V_{RWM} = ±15 V
ESD protection of RF signal lines according to **IEC61000-4-2**	**±12 kV** (contact), **±14 kV** (air)	**±10 kV** (contact)
Extremely low capacitance	C_L = **0.1 pF** (typical)[1)]	C_L = **0.09 pF** (typical) [1)]
Very low reverse current	I_R < **0.1 nA**	I_R < **0.1 nA**
Extremely small form factor down to 0.62 x 0.32 x 0.31 mm²	Yes	Yes
Pb-free package (RoHS compliant)	RoHS HAL	RoHS HAL

1) at f = 1 GHz

2.2 Key Applications of ESD101-B1 / ESD103-B1

- WLAN, GPS antenna, DVB T/H, Bluetooth Class 1 and 2
- RF antenna
- Super high speed interfaces
- Connectivity applications
- Automated Meter Reading

2.3 Description

Devices ESD101-B1 / ESD103-B1 consist of two identical chips, connected in series in opposite directions (see Figure 7b). The device structure and the manufacturing process have been specifically optimized to fulfill requirements stated above.

The devices belong to the same family, and differ primarily in their operating voltage range. Both devices are available in the TSSLP-2 package (ESD101/103-B1-**02ELS**) with dimensions of 0.62 mm x 0.32 mm x 0.31 mm (EIA case size 0201) and later on as well in TSLP-2 (ESD101/103-B1-**02EL**) with dimensions of 1.0 mm x 0.6 mm x 0.39 mm (EIA case size 0402).

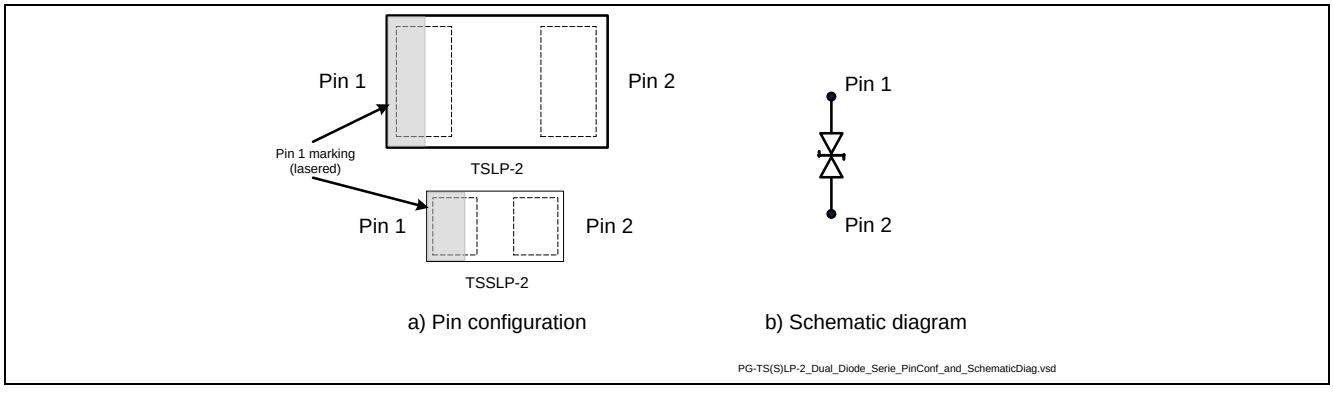

Figure 7 Pin configuration and schematic diagram of ESD101-B1 / ESD103-B1

3 Application Circuit and Performance Overview

3.1 Schematic Diagram

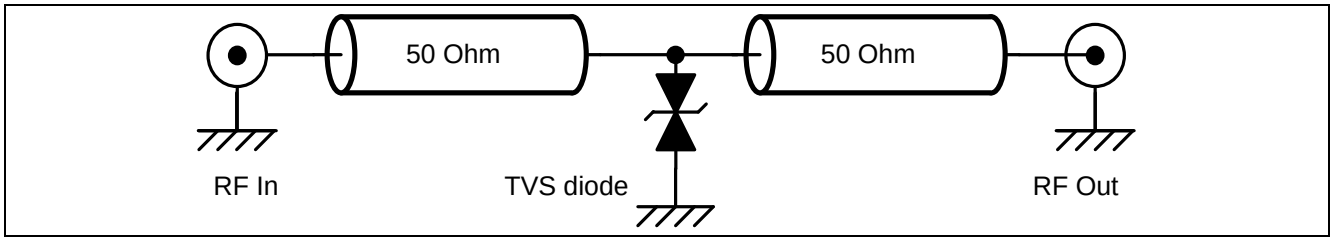

Figure 8 Schematics of the ESD101-B1 / ESD103-B1 Application Circuit

3.2 Linear and NON-linear measurement Setups

In order to measure insertion and return loss, devices were connected to a network analyzer as shown in Figure 8 without any additional modules in between. To minimize parasitic effects caused by PCB discontinuities, the full 2-port calibrated measurement was done with RF probes direct on the device pads. Insertion (IL) and return (RL) loss was calculated from measured data as follows:

$$IL = -20\log|S_{21}|$$

$$RL = -20\log|S_{11}|$$

Non linear characterization of the ESD101/103-B1 is done via harmonic measurement P(H2), P(H3) at given fundamental power P(H1) and by the intermodulation distortion measurement for a given blocker and interferer constellation. Setups for nonlinearity measurements (harmonics and intermodulation distortion) are shown on Figure 9 and Figure 10 respectively. Mesurement results for the harmonics P(H2), P(H3) vs. fundamental power P(H1) are included in chapter 4.2.

Intermodulation distortion (IMD) measurement reproduces more the scenario of real application. In this scenario (e.g. in all kind of full duplex systems like CDMA, UMTS, LTE) the high power transmission signal (Tx, e.g. P_{TX} =20 dBm) and a received Jammer signal (e.g. P_I =-15 dBm) are both entering the TVS diode. Special combinations of Tx and Jammer signals produce 2nd and 3rd order intermodulation products, which can fall in the Rx band and interfere with the wanted Rx signal.

With the help of the phase shifter, matching conditions for the interfering signal can be adapted to simulate various matching scenario. Lowest intermodulation is expected at the ESD diode providing a low load impedance load for the blocker.

Test conditions for intermodulation measurements are summarized in paper from Nokia titled „Antenna Switch Linearity Requirements for GSM/WCDMA Mobile Phone Front-Ends" presented at the "Wireless Technolgies 2005 - 8th European Conference on Wireless Technology".

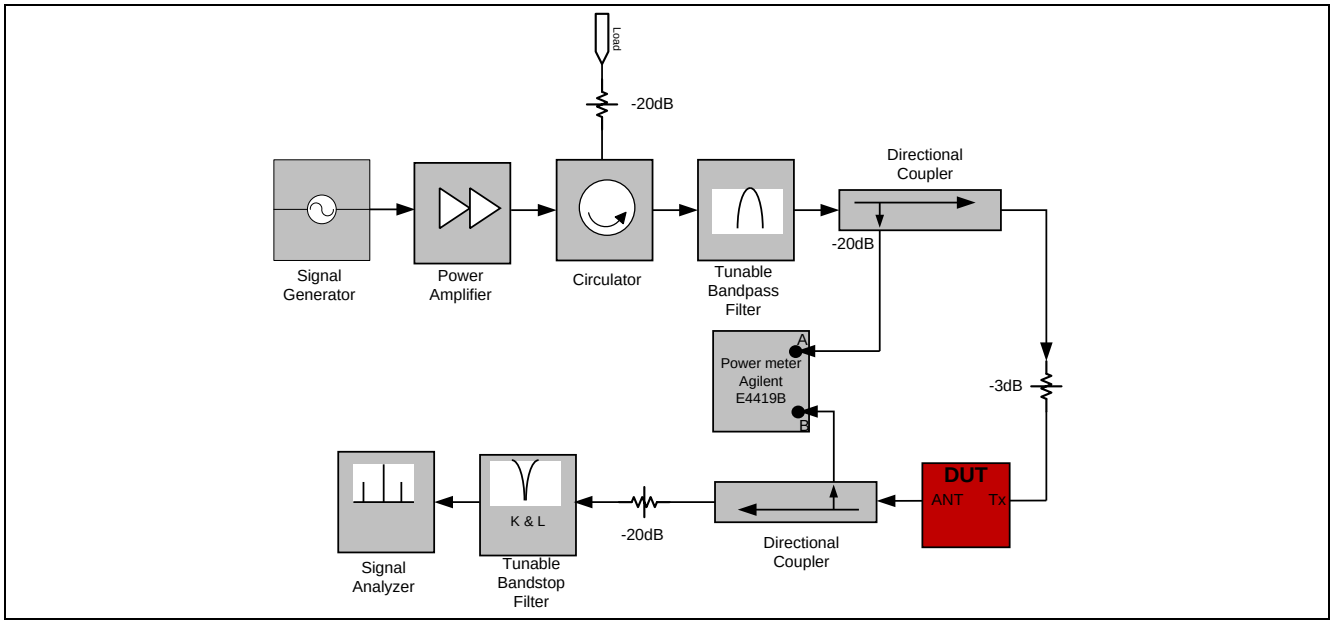

Figure 9 Set-Up for Harmonics Measurement

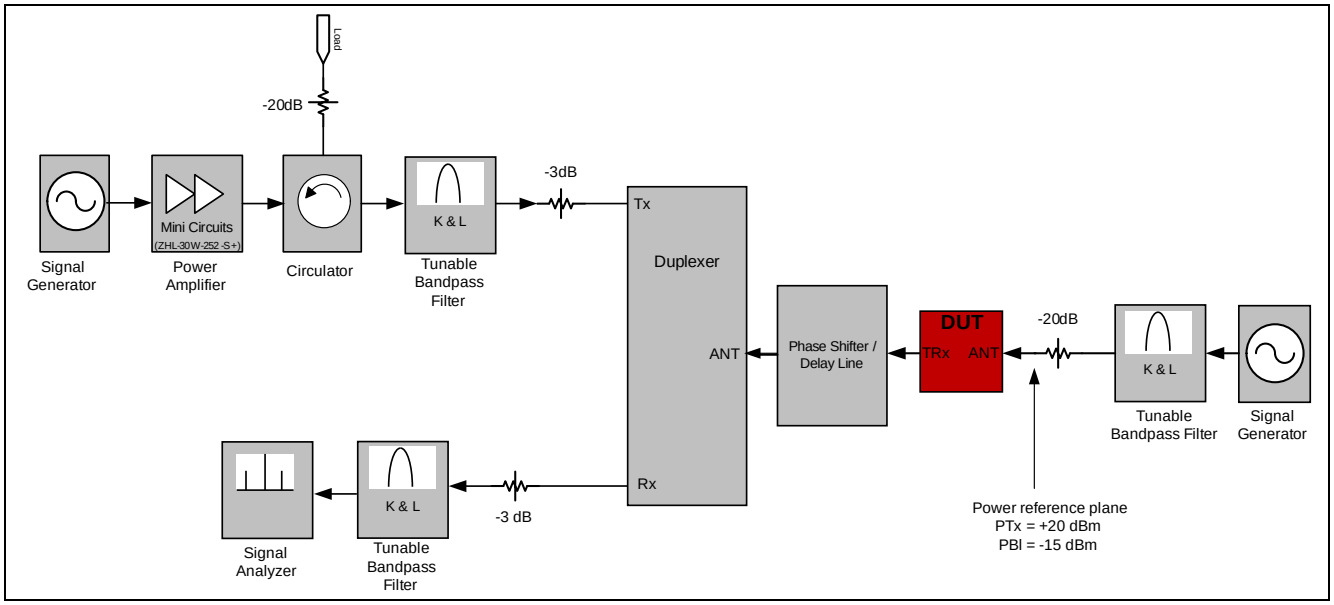

Figure 10 Test Set-Up for IMD Measurements

Table 2 Test Conditions for IMD Measurements

Band (MHz)	Tx Freq. (MHz)	Rx Freq. (MHz)	IMD2 Low Jammer 1 (MHz)	IMD3 Jammer 2 (MHz)	IMD2 High Jammer 3 (MHz)
850	836.5	881.5	45	791.5	1718
1900	1880	1960	80	1800	3840
2100	1950	2140	190	1760	4090

P_{TX} = +20dBm, P_I = -15dBm, frequencies in MHz @25°C

3.3 Summary of Measurement Results

Table 3 Electrical Characteristics (at room temperature)

Parameter	Symbol	Value		Unit	Comment/Test condition
		ESD101-B1	ESD103-B1		
Insertion Loss	IL	-0.1 -0.1	-0.1 -0.1	dB	f=2 GHz f=6 GHz
Return Loss	RL	-35.6 -27.3	-38.7 -29.7	dB	f=2 GHz f=6 GHz

Table 4 Harmonics generation

Harmonic	Low Band, f_0=824MHz		High Band, f_0=1800MHz		Unit	Comment/Test condition
	ESD101-B1 Pin=26 dBm	ESD103-B1 Pin=35 dBm	ESD101-B1 Pin=27 dBm	ESD103-B1 Pin=32 dBm		
$2f_0$	-71.6	-66.3	-70.9	-63.6	dBm	
$3f_0$	-54.0	-44.4	-51.2	-46.5	dBm	

Table 5 Intermodulation distortion ESD101-B1

Band	Tx, MHz	Rx, MHz	Blocker, MHz	IMD Product level, dBm		IMD Generation
				Min	Max	
I	1950	2140	190	-124	-96	TX+Blocker
			1760	-102	-87	2*TX-Blocker
			4090	-139	-122	Blocker-TX
V	836.5	881.5	45	-110	-93	TX+Blocker
			791.5	-101	-85	2*TX-Blocker
			1718	-122	-113	Blocker-TX

Table 6 Intermodulation distortion ESD103-B1

Band	Tx, MHz	Rx, MHz	Blocker, MHz	IMD Product level, dBm		IMD Generation
				Min	Max	
I	1950	2140	190	-116	-93	TX+Blocker
			1760	-103	-86	2*TX-Blocker
			4090	-123	-109	Blocker-TX
V	836.5	881.5	45	-109	-92	TX+Blocker
			791.5	-101	-85	2*TX-Blocker
			1718	-113	-106	Blocker-TX

4 Measurement Graphs

4.1 Linear RF characteristic

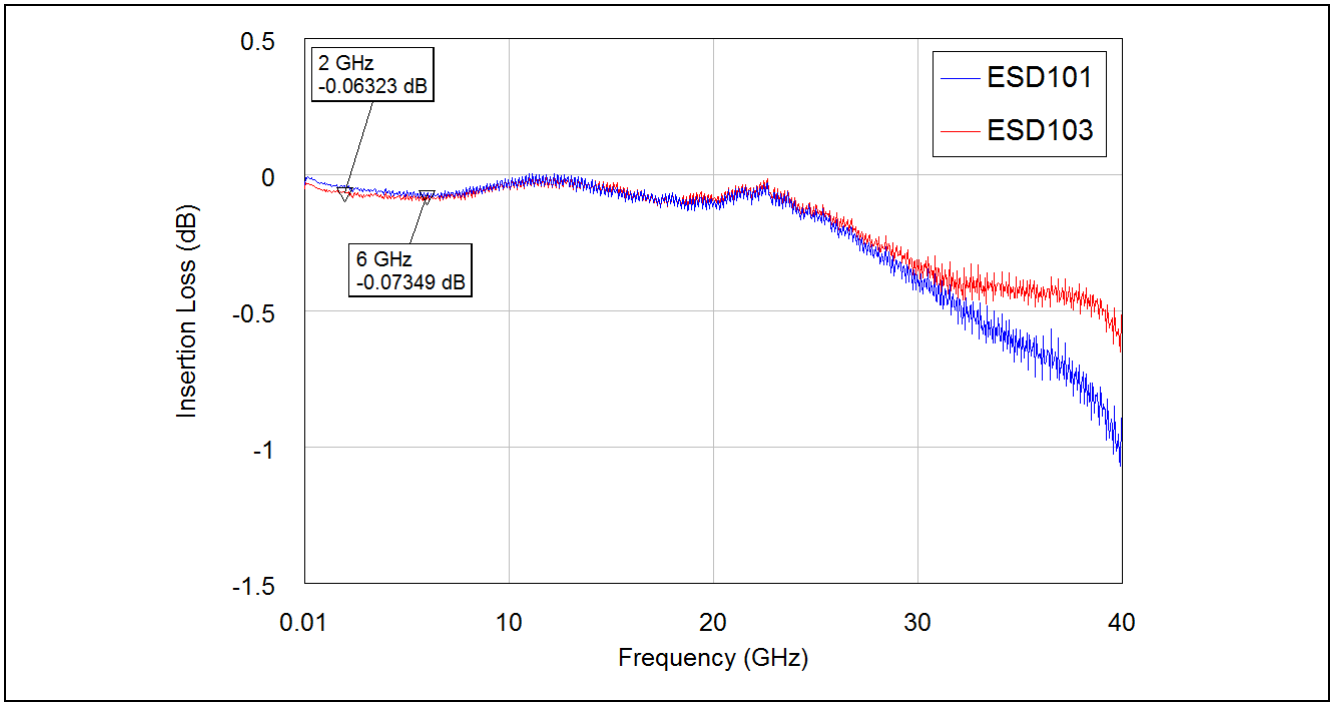

Figure 11 Insertion Loss: ESD101 vs. ESD103 @ 0V bias

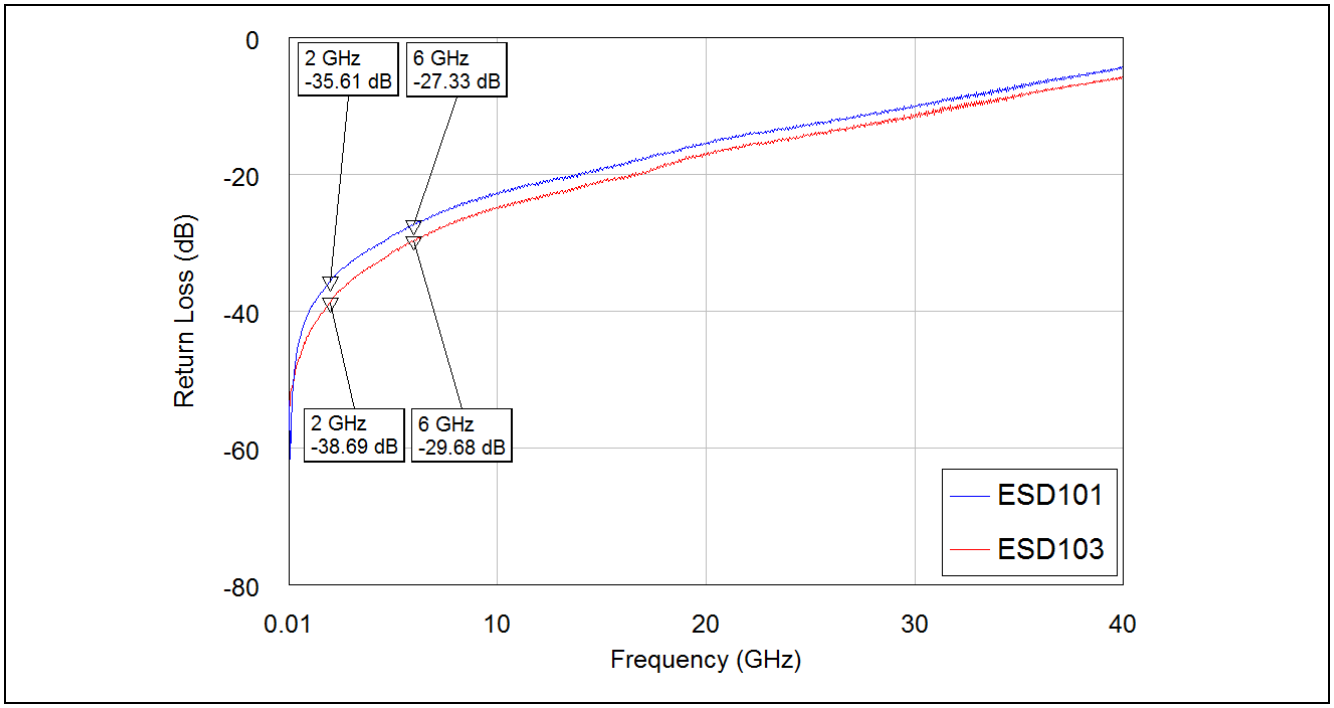

Figure 12 Return Loss: ESD101 vs. ESD103 @ 0V bias

Comparing the RF characteristic (S-parameter) between the ESD101/103-B1-**02ELS** in TSSLP-2 (SMD size 0201) with the slightly larger ESD101/103-B1-**02EL** in TSLP-2 (SMD size 0402) we have to take the longer internal chip to chip bond into account. This results in a shift of the self-resonance frequency of about 45GHz for the ESD101/103-B1-**02ELS**, down to ca. 35GHz.

4.2 Non-linear RF characteristic

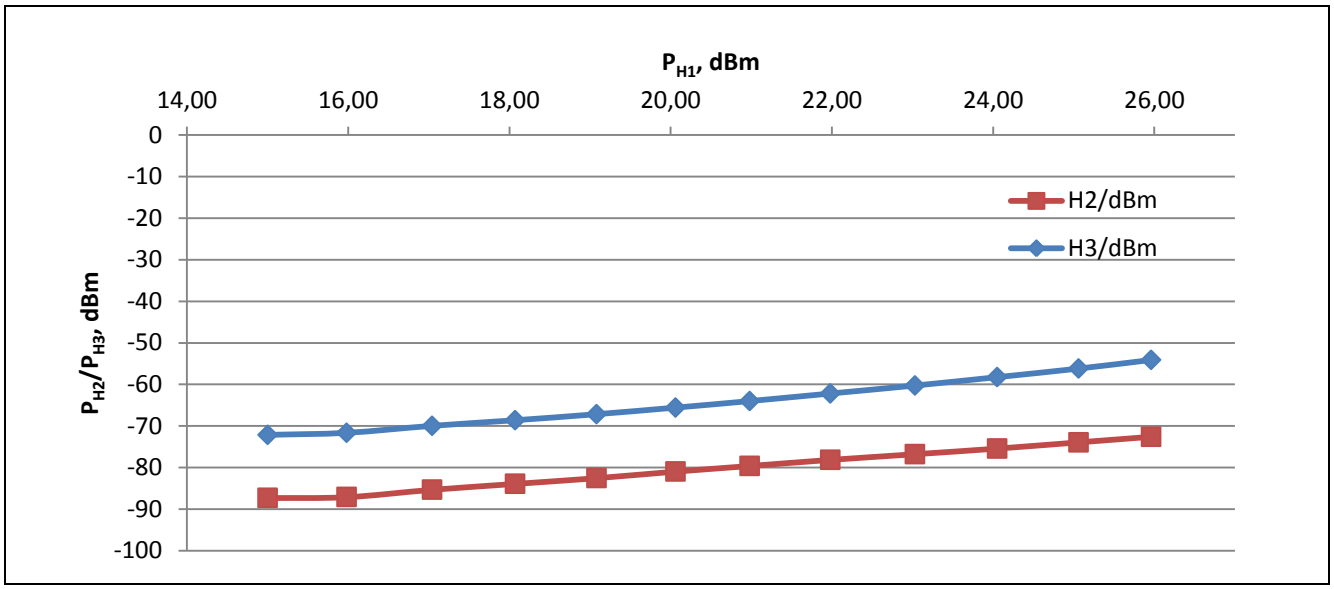

Figure 13 Harmonics Generation in Low Band (f_0=824MHz), ESD101-B1

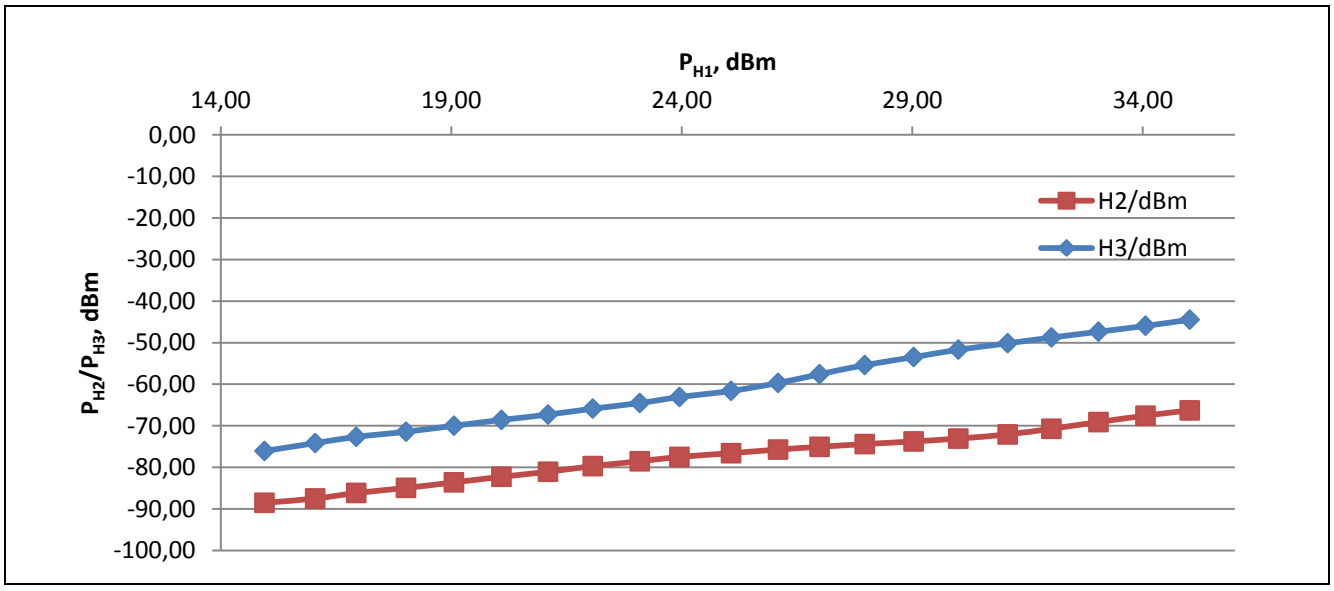

Figure 14 Harmonics Generation in Low Band (f_0=824MHz), ESD103-B1

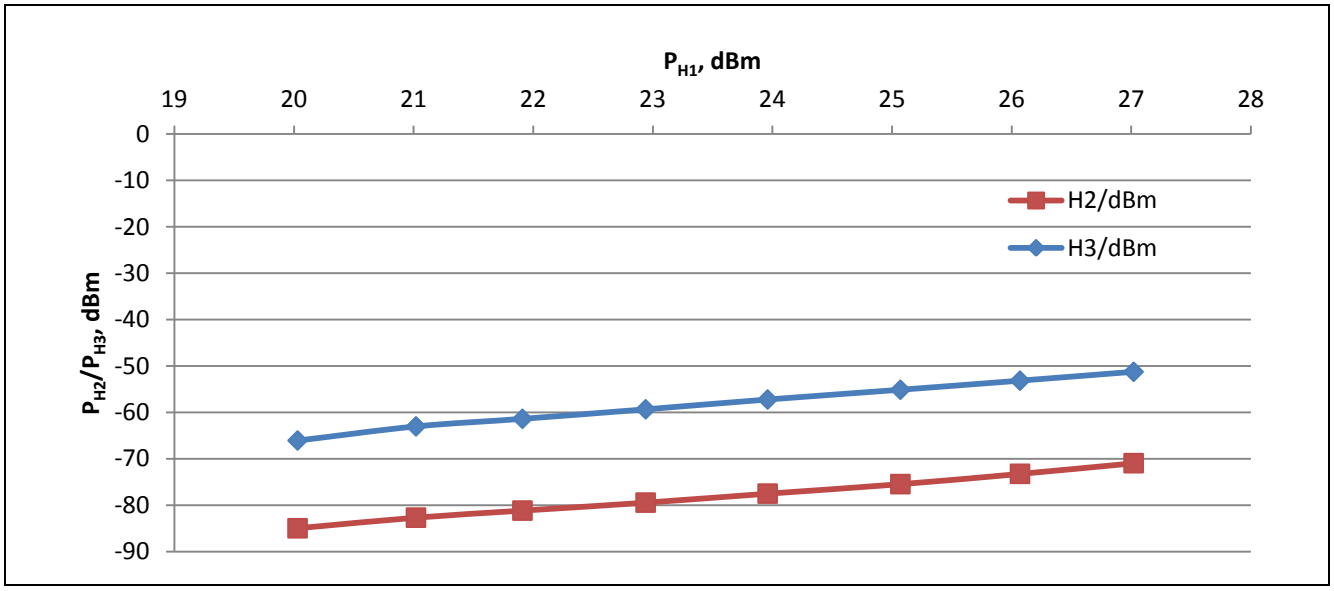

Figure 15 Harmonics Generation in High Band (f_0=1800MHz), ESD101-B1

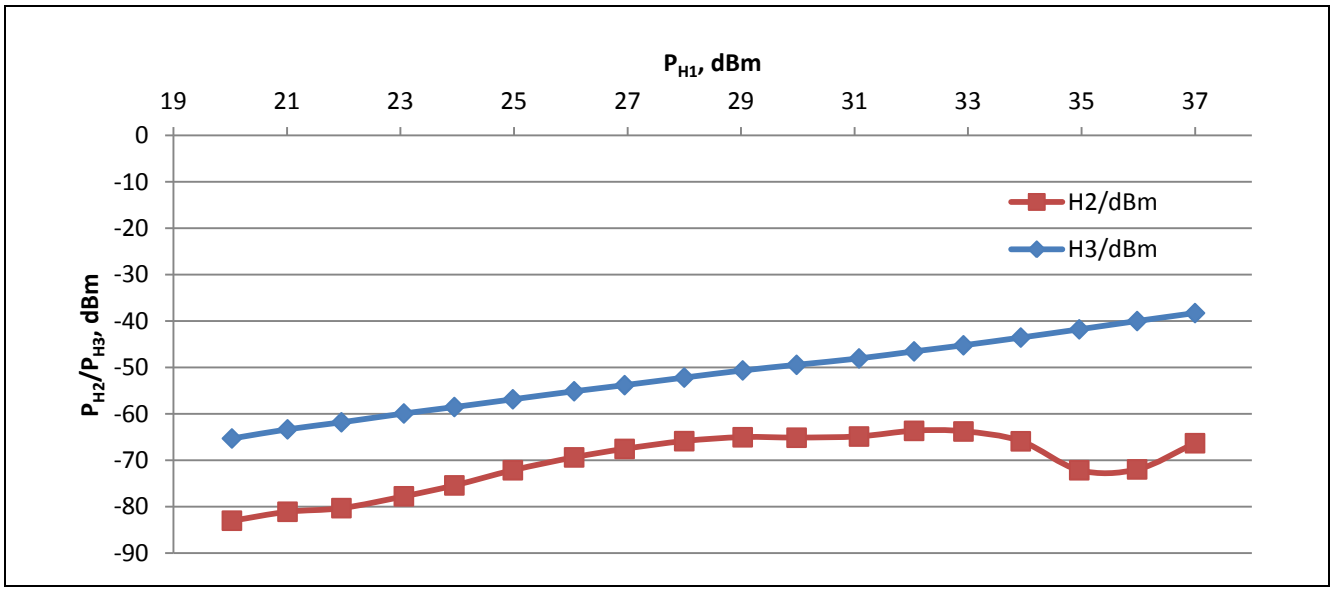

Figure 16 Harmonics Generation in High Band (f_0=1800MHz), ESD103-B1

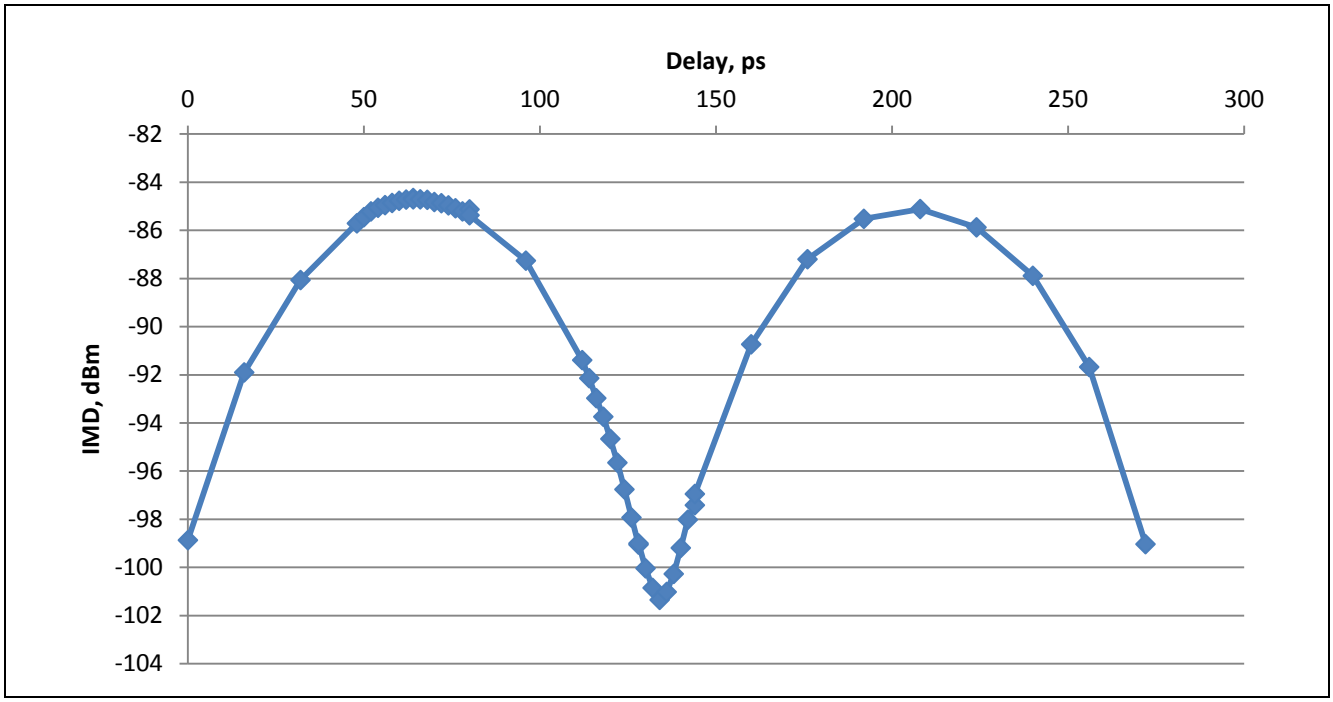

Figure 17 Example of Intermodulation Measurement Data (ESD103-B1, Band V, f_{Block}=791.5 MHz) depending on the phase shifter adjustment

As mentioned in chapter 3.2, Intermodulation Distortion 3rd order depends significant on the phase shifter (delay). There are dedicated matching conditions resulting into a low IM 3rd order product.

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