Realizing small inductor values on a PCB by using microstrip lines

As needed for e.g. BGA915N7

Application Note AN258

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Page	**Subjects (major changes since last revision)**
12 – 13	Chapter on via inductance added

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1 Introduction

The use of distributed microstrip circuit elements is very common at microwave frequencies. At those high frequencies convertional lumped SMD-elements can not work anymore as their desired performance as an inductor or capacitor is outweighed by the unavoidable parasitic of such a device.

The principles of microstrip circuit design with distributed elements apply also to lower frequencies where lumped elements still work as they are supposed. Microstrip elements can become quite big at those frequencies and therefore use up a lot of PCB space. Despite this they still can be very useful, especially **to realize small inductance values which are not available as SMD elements**, as most suppliers offer 1 nH coils as the smallest value in their line-up.

The inductance values presented in this application note were derived from simulations using frequencies around 1575 MHz.

2 Microstrip lines used as shunt inductors

A microstrip transmission line involves inductance associated with the flow of current in the conductor and capacitance associated with the strip separated from ground by the dielectric substrate. This distributed inductance and capacitance is the basis of the classic L-C model for a transmission line and it accounts for the term “distributed”. If the line is narrow, the capacitance is small. A narrow, high impedance line behaves like an inductor if it is less than 90 degrees in electrical length. A wide, low-impedance line looks capacitive.

The impedance, Z_S, at the input of a transmission line of characteristic impedance Z_0 and length θ terminated in a load, Z_L, is given by:

$$Z_S = Z_0 \frac{Z_L - jZ_0 \tan\theta}{Z_0 + jZ_L \tan\theta}$$

Considering the case where Z_L is a short. Then

$$Z_S = jZ_0 \tan\theta$$

Since the input impedance of a shorted inductor is jX_L,

$$X_L = Z_0 \tan\theta$$

This means that the reactance of an inductor in a network may be replaced with a transmission line of characteristic impedance Z_0 and length θ. This equivalence is exact only at the design frequency. The reactance of an inductor increases linearly with increasing frequency while the reactance of a shorted line increases as tan θ. If the line is short, that is $\theta << 90°$, then $\tan\theta \approx \theta$ and the input reactance of a shorted line increases linearly with frequency. Therefore, a shorted line behaves like an inductor over a range of frequencies where the line is much less than 90° long, preferably less than 30°.

Generally, the equivalence is better with higher impedance and shorter length lines for inductors, and with lower impedance and shorter length lines for capacitors.

To realize a shorted microstrip transmission line it is necessary to use one or more vias to connect the line to the GND plane. These vias possess a parasitic inductance that has to be considered to get the total inductance of the microstrip line under examination.

2.1 Characteristic impedance of microstrip lines

As seen in the previous section it is necessary to know the length and characteristic impedance of a line to determine its equivalent inductance.

The closed-form expression for the characteristic impedance, Z_0, of a microstrip line as shown in Figure 1, assuming zero strip thickness (t = 0), is given as[1]:

$$Z_o = \frac{60}{\sqrt{\varepsilon_{\mathrm{eff}}}} \ln\left[\frac{h}{W}A + \sqrt{1+\left(\frac{2h}{W}\right)^2}\right]$$

with

$$A = 6 + (2\pi - 6)\exp\left[-\left(\frac{30.666h}{W}\right)^{0.7528}\right]$$

$$B = 0.564\left\{1+\frac{1}{49}\ln\left(\frac{(W/h)^4+(W/52h)^2}{(W/h)^4+0.432}\right) + \frac{1}{18.7}\ln\left[1+\left(\frac{W}{18.1h}\right)^3\right]\right\}\left(\frac{\varepsilon_r-0.9}{\varepsilon_r+3}\right)^{0.053}$$

and

$$\varepsilon_{\mathrm{eff}} = \frac{\varepsilon_{r+1}}{2} + \frac{\varepsilon_{r-1}}{2}\left(1+10\frac{h}{W}\right)^{-B}$$

where ε_{err} is the effective dielectric constant of the microstrip structure.

The equations show that the characteristic impedance is determined strongly by the ratio h / W of substrate height to line width.

The effective dielectric constant ε_{eff} plays some role, as well, but simulations to create the curves in chapter 3 and chapter 4 have shown that this influence can be neglected for the geometries covered in this application note. **These simulations based on a dielectric constant ε_r of 4.2**. Changing this value from 2 to 6 had no effect on the equivalent inductance.

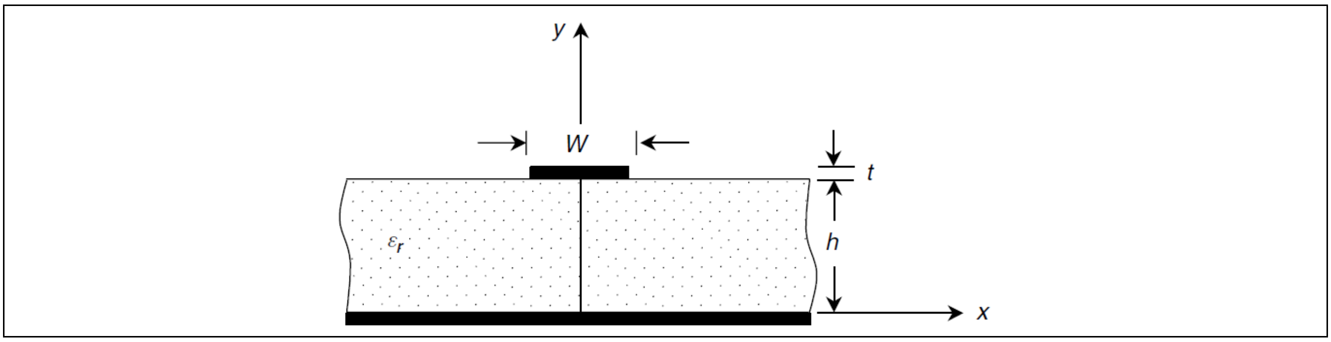

Figure 1 Cross section of a PCB

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[1] E. O. Hammerstad and O. Jensen, “Accurate Models for Microstrip Computer-Aided Design,” 1980 IEEE MTT-S Digest, pp. 407–409

3 Inductance of different line widths for fixed thickness of substrate

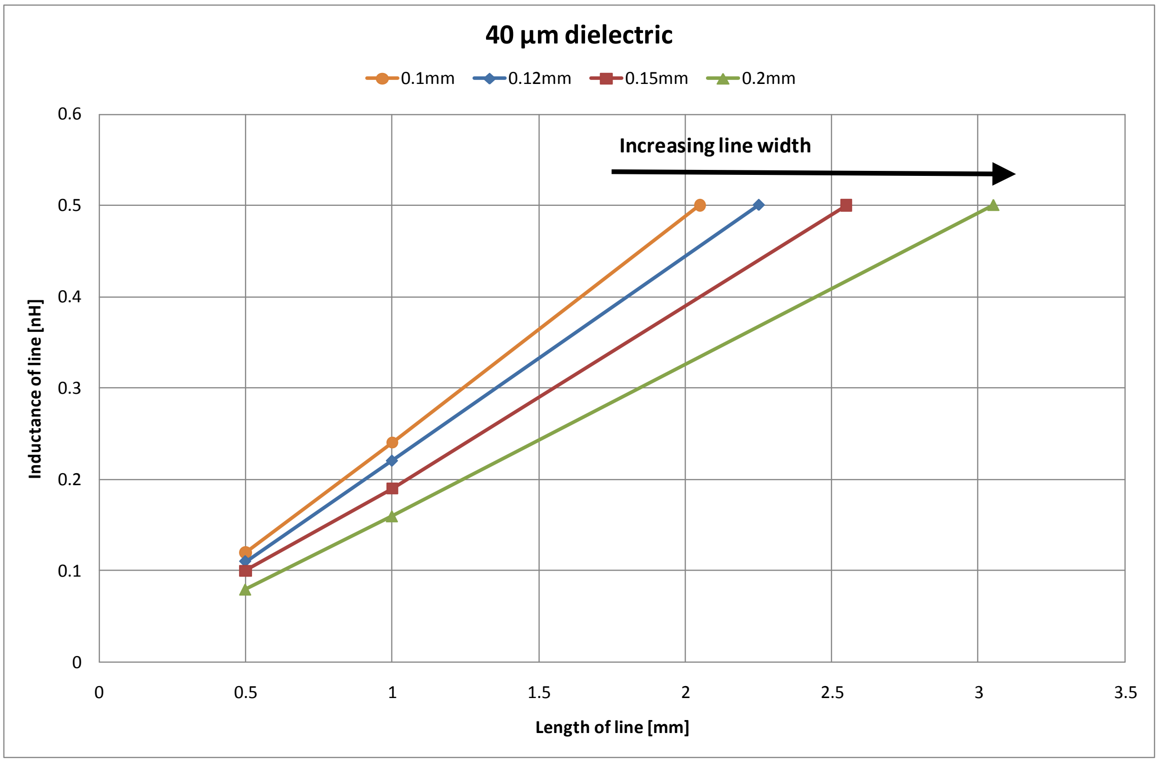

Figure 2 Inductance vs. length: Substrate thickness = 40µm

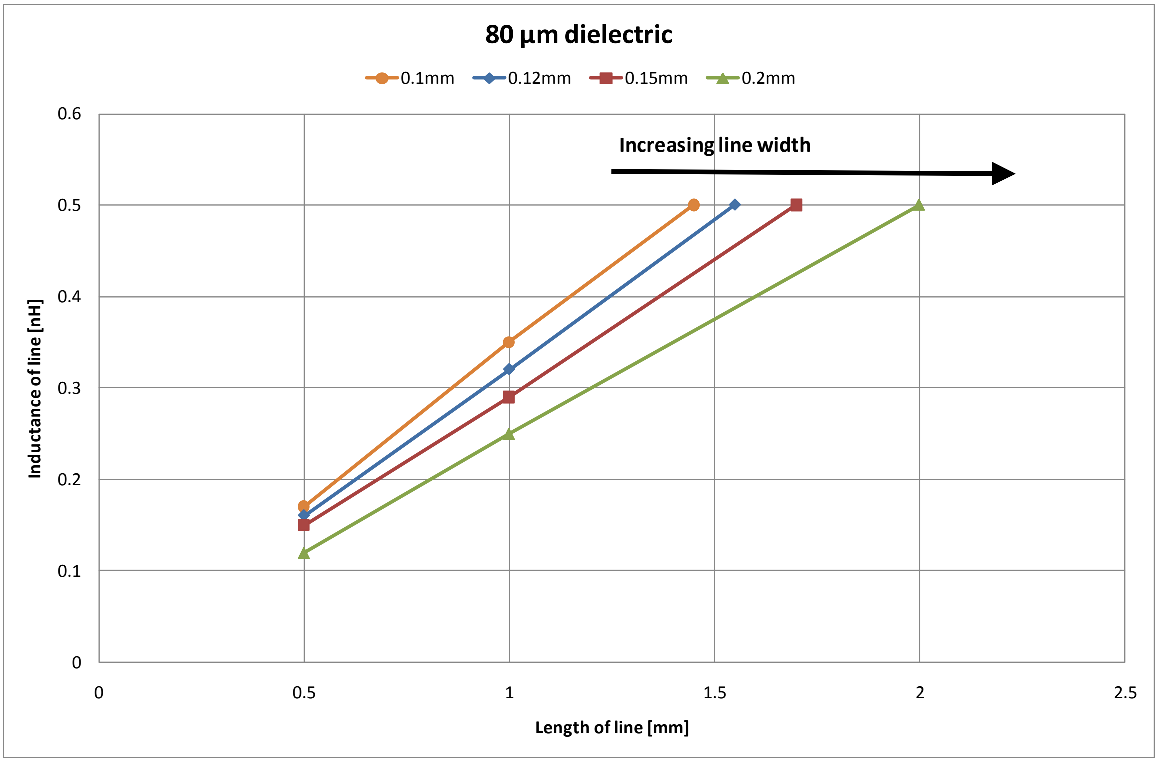

Figure 3 Inductance vs. length: Substrate thickness = 80µm

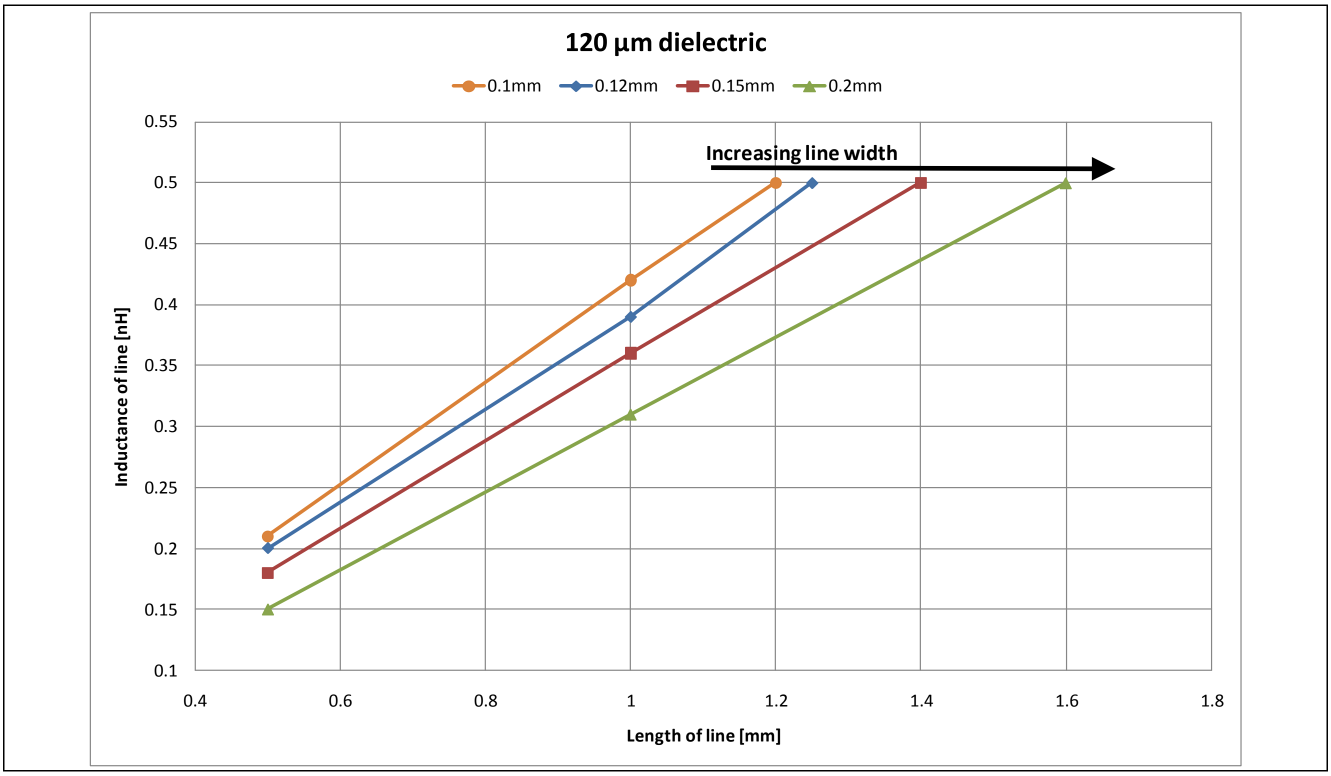

Figure 4 Inductance vs. length: Substrate thickness = 120µm

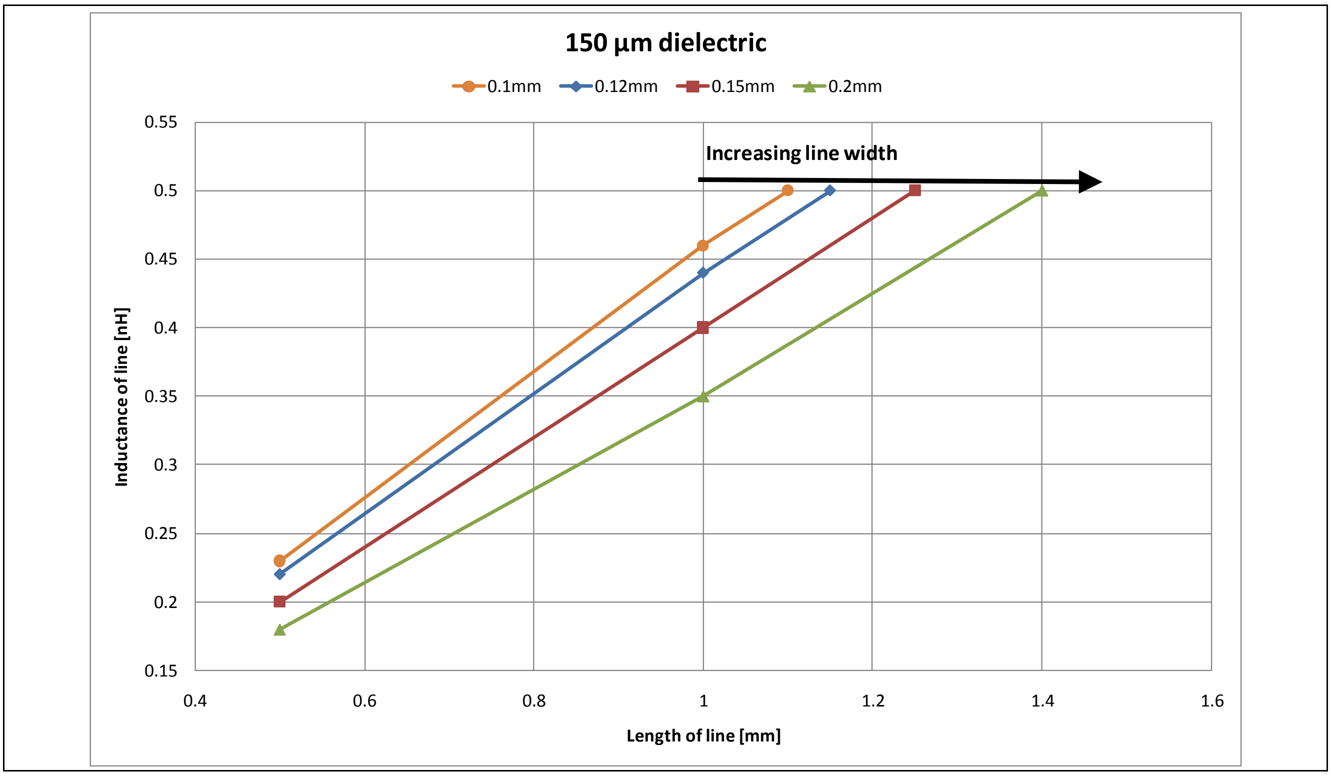

Figure 5 Inductance vs. length: Substrate thickness = 150µm

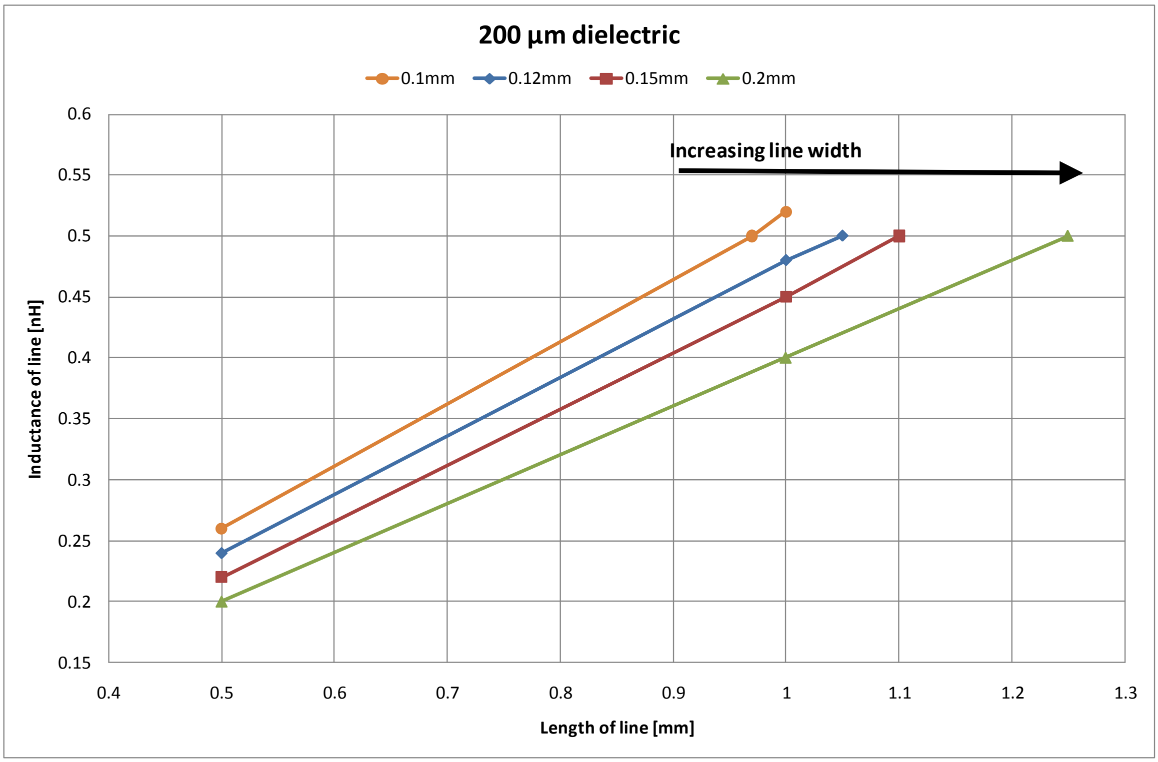

Figure 6 Inductance vs. length: Substrate thickness = 200µm

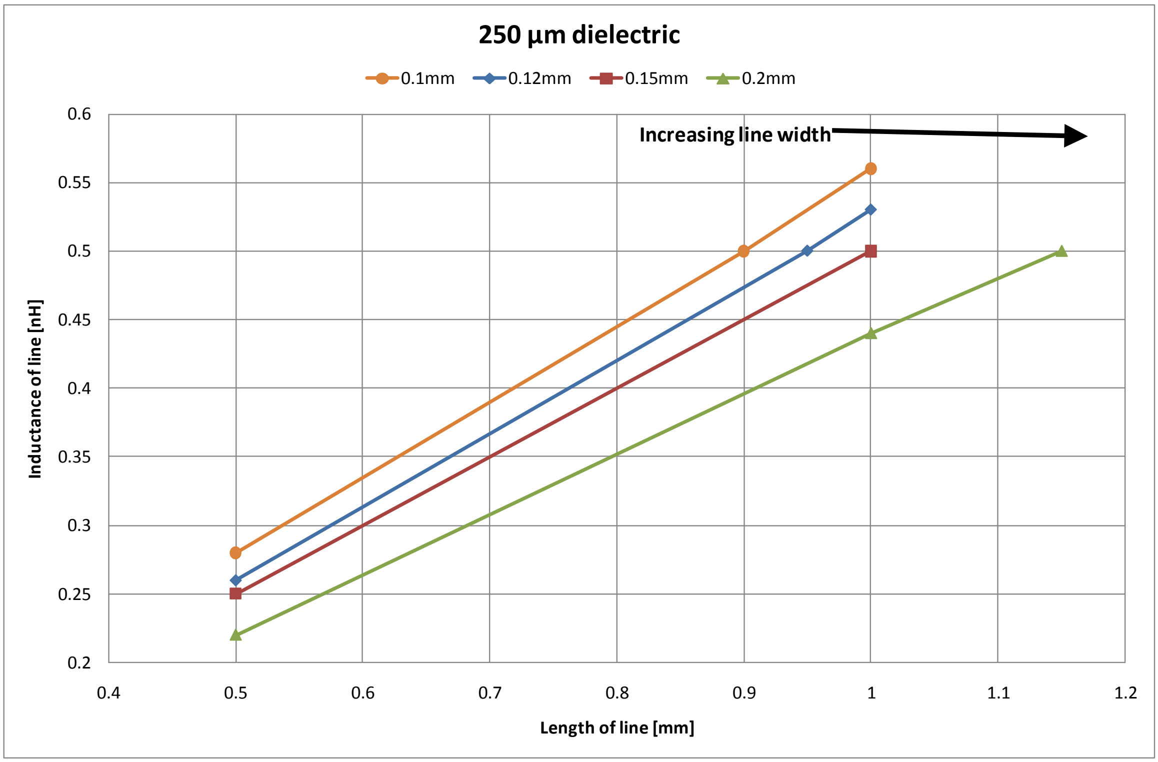

Figure 7 Inductance vs. length: Substrate thickness = 250µm

4 Inductance of lines on different substrates with fixed line widths

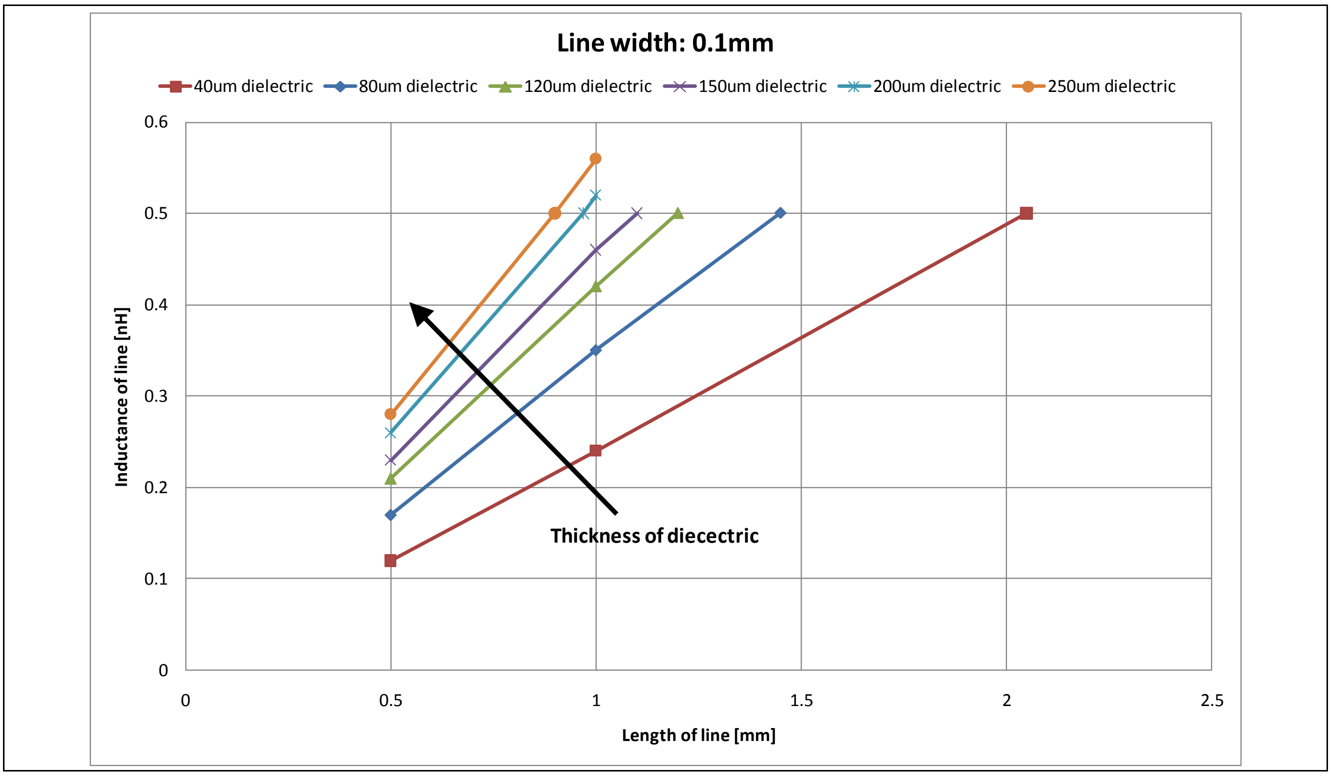

Figure 8 Inductance vs. length: Line width = 0.1mm.

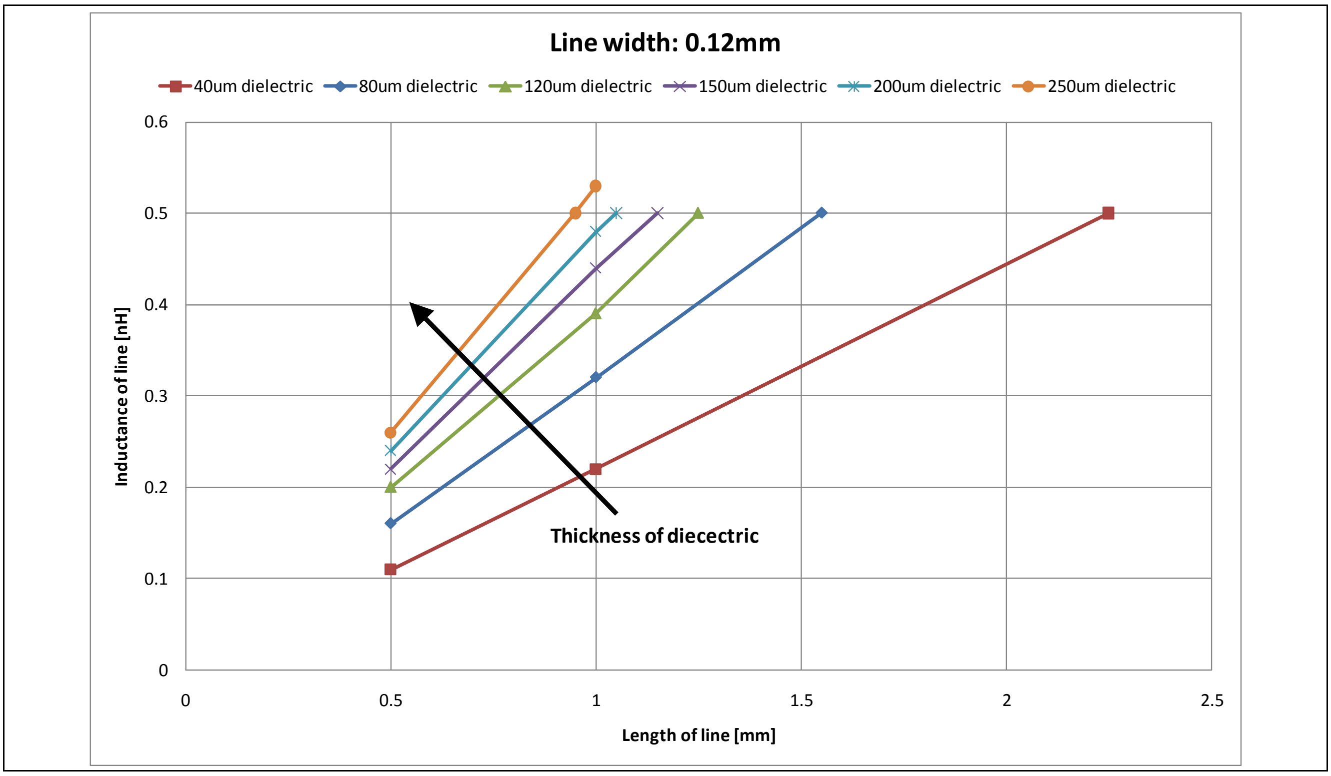

Figure 9 Inductance vs. length: Line width = 0.12mm.

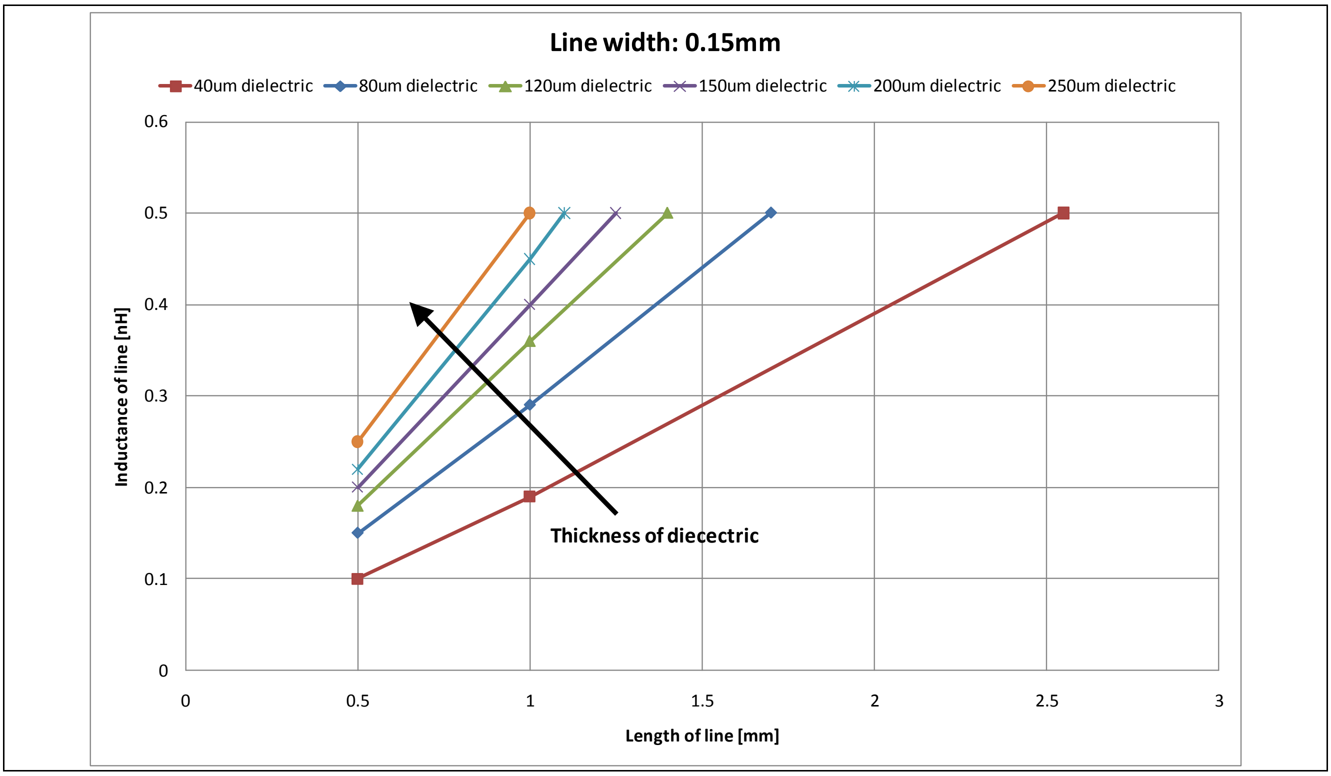

Figure 10 Inductance vs. length: Line width = 0.15mm.

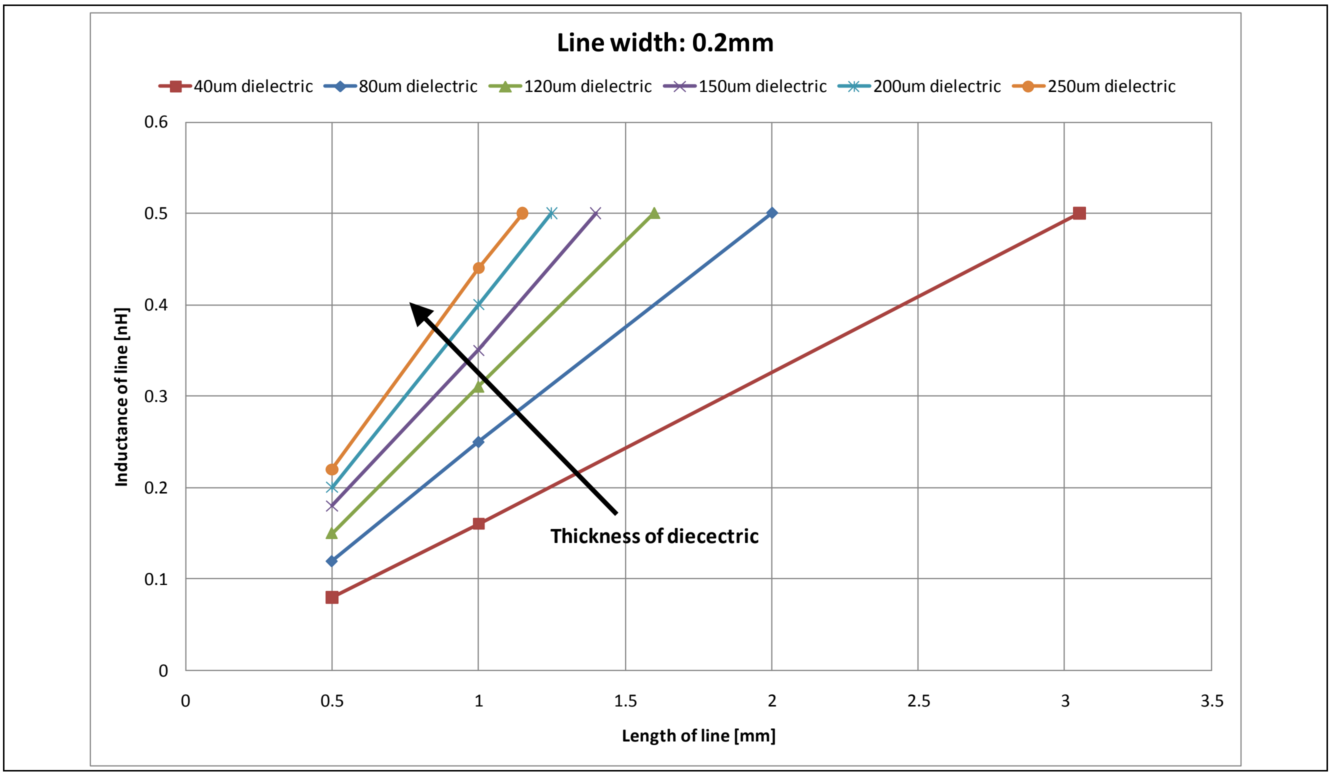

Figure 11 Inductance vs. length: Line width = 0.2mm

5 Inductance of vias

Figure 12 shows a via hole including the via pad. In this case the diameter of the via hole is 200 µm, this application note shows inductance values for via diameters of 0.1 mm, 0.15 mm and 0.2 mm. The pad of the via here is 500 µm, but many PCB manufacturers refer in their design rules rather to the rest ring width, in this example 150µm. So do we in this document, because the ring width stays constant for different hole diameters while the pad diameter would change, making the depiction of parameterized curves difficult.

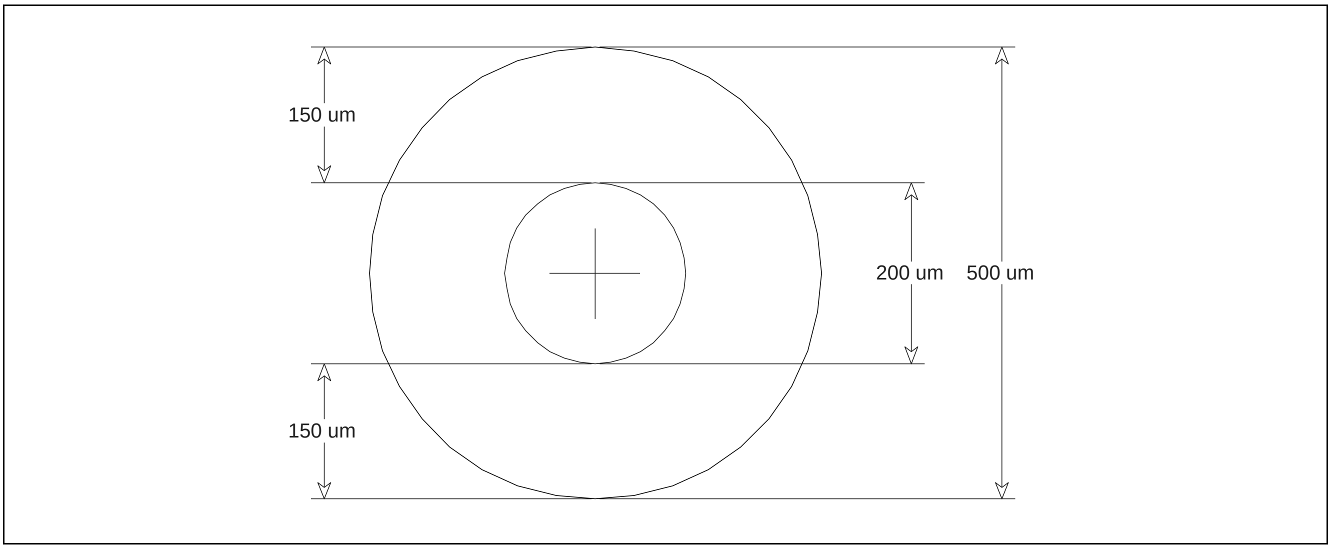

Figure 12 Example of a via hole including dimensions

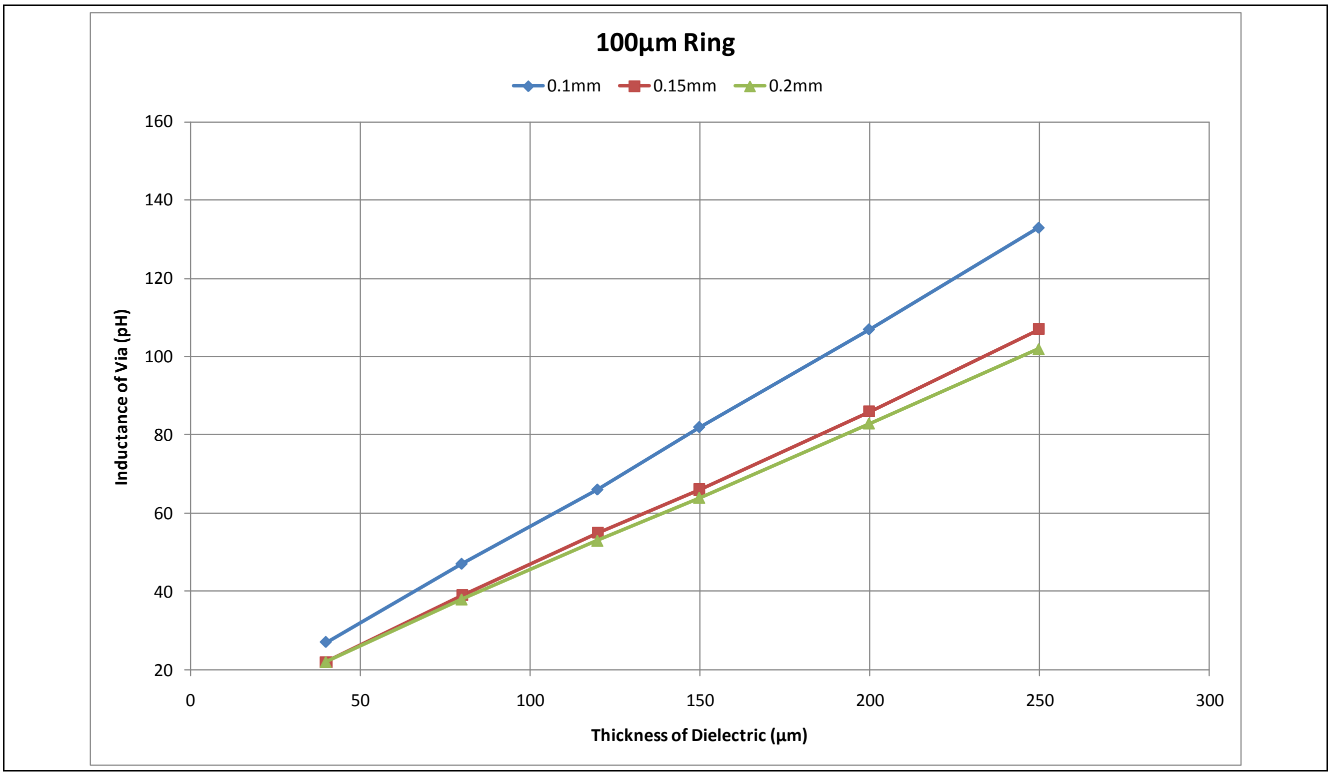

Figure 13 Via inductance vs. thickness of dielectric: 100 µm ring width

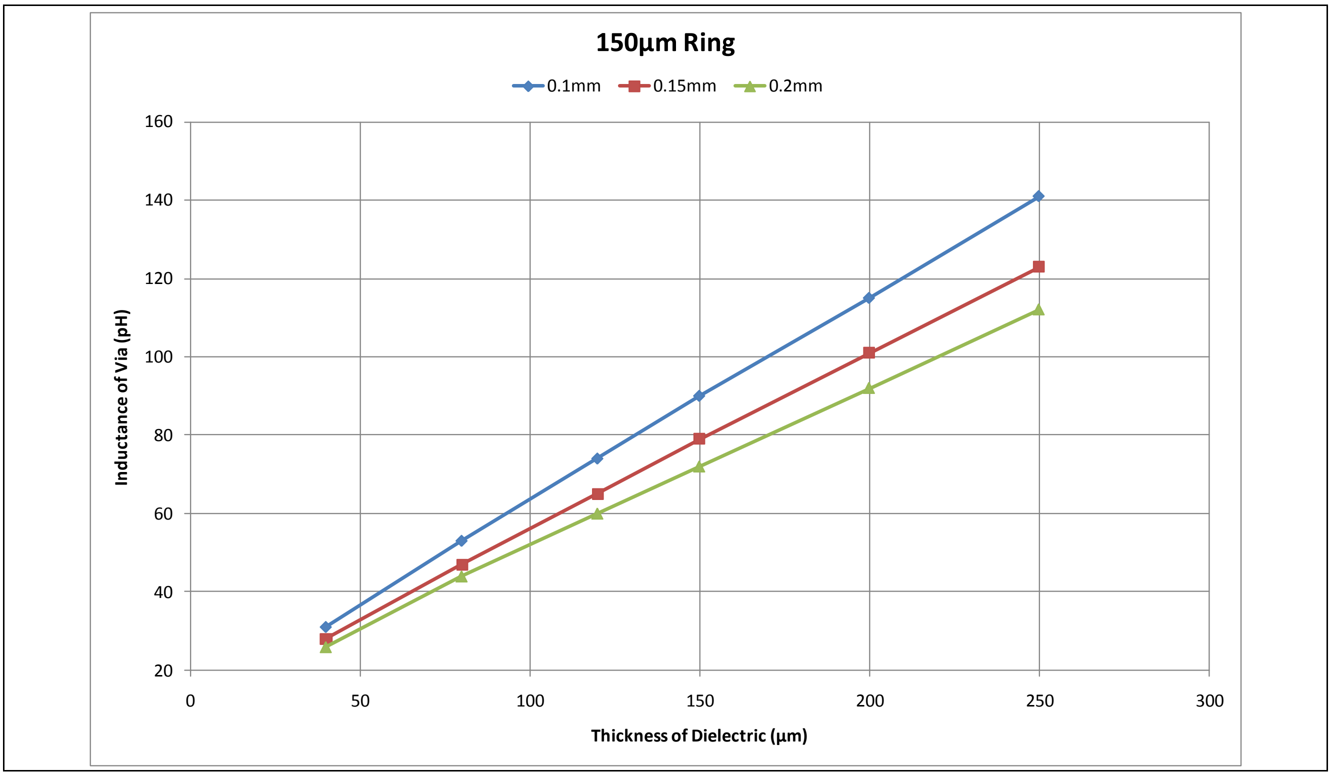

Figure 14 Via inductance vs. thickness of dielectric: 150 µm ring width

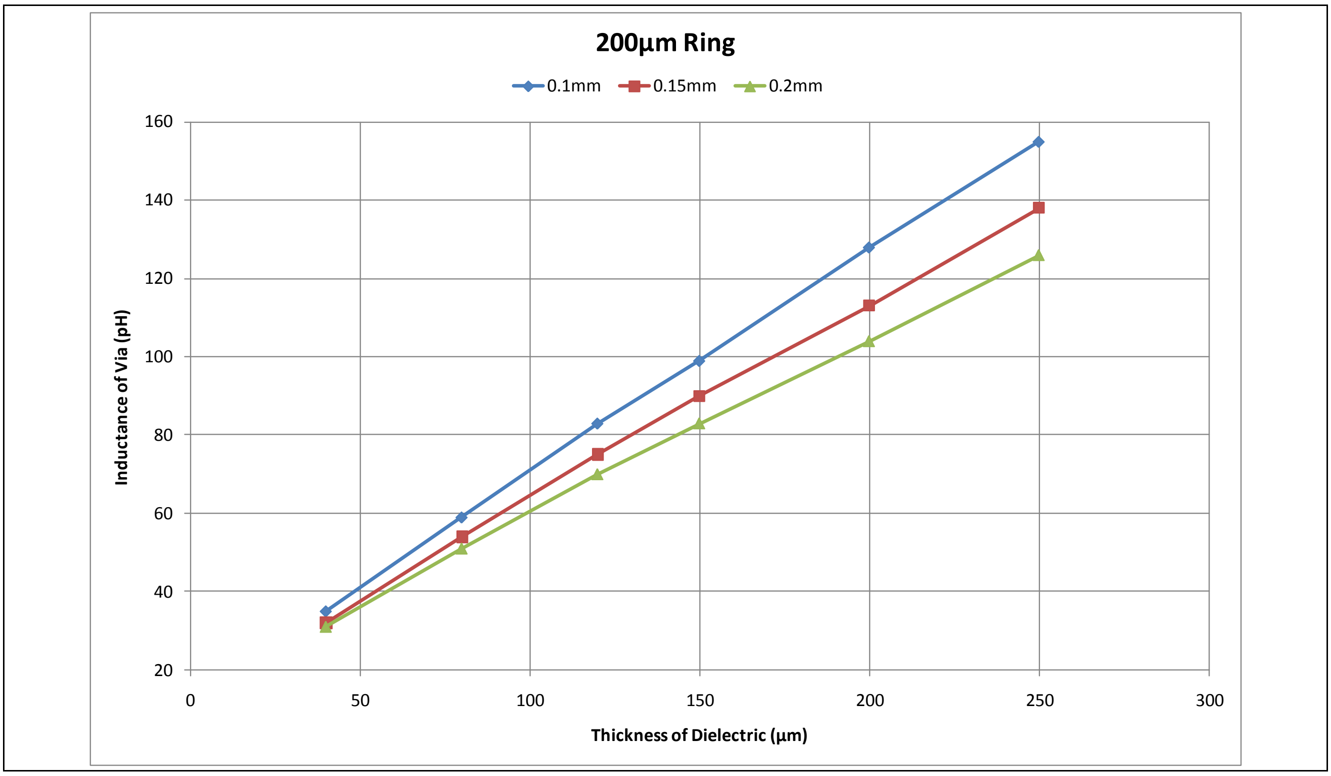

Figure 15 Via inductance vs. thickness of dielectric: 200 µm ring width

Author

Dietmar Stolz, Staff Application Engineer of Business Unit “RF and Protection Devices”

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