BGB707L7ESD

BGB707L7ESD as a Broadband Low Noise Amplifier for mobile analog TV applications

Application Note AN232
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1 Introduction

Over the last few years there has been a clear trend in television to move from the classical TV-set out to more mobile platforms like notebooks, cell phones and PDAs. Especially the introduction of digital terrestrial television in many countries and the more and more evolving hand-held television standards like DVB-H and T-DMB support this evolution.

With television going mobile the antennas are getting smaller, resulting in a loss in antenna gain. It requires an additional LNA with low noise figure to keep up a good reception of the TV signal, no matter if the TV tuner's RF frontend uses the classical three-band tuner (Figure 1) or the more space saving silicon tuner (also called double conversion tuner or up-down converter, Figure 2). Particularly the silicon tuner has the need for and external LNA as tuner ICs in general tend to have high noise figures and the silicon tuner approach doesn't implement any prestages including an RF MOSFET.

The application for BGB707L7ESD shown in this document was designed for use in mobile TV applications having electrically short (telescope) antennas. The low current consumption of the LNA makes it ideal for mobile applications while still offering a good input compression point compared to this low current. The use of short antennas relaxes the requirements for linearity anyway.

Being located directly after the antenna an LNA needs to be protected from ESD strikes. BGB707L7ESD's built-in ESD protection of 2kV HBM at all pins (3kV at the RF input pin) helps a lot in meeting this requirement.

In case of even higher protection levels being needed additional ESD protection using an Infineon TVS diode is highly recommended. For more details on ESD protection please refer to Appendix 1.

![Figure 1 Classical Three-Band Tuner](3Band.vsd)

![Figure 2 Silicon Tuner](Si_Tuner.vsd)
2 Summary of Measurement Results

All data was measured in a 50Ω system.

Table 1 Summary of Measurement Results

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
<th>Note/Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency Range</td>
<td>Freq</td>
<td>47-862</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>DC Voltage</td>
<td>Vcc</td>
<td>3.0</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>DC Current</td>
<td>Icc</td>
<td>2.9</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Gain</td>
<td>G</td>
<td>12.6 – 13.7</td>
<td>dB</td>
<td>See Figure 4</td>
</tr>
<tr>
<td>Noise Figure</td>
<td>NF</td>
<td>1.3 – 1.8</td>
<td>dB</td>
<td>See Figure 5</td>
</tr>
<tr>
<td>Input Return Loss</td>
<td>RLin</td>
<td>4</td>
<td>dB</td>
<td>See Figure 6</td>
</tr>
<tr>
<td>Output Return Loss</td>
<td>RLout</td>
<td>9</td>
<td>dB</td>
<td>See Figure 6</td>
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<tr>
<td>Reverse Isolation</td>
<td>IRev</td>
<td>24.5</td>
<td>dB</td>
<td>See Figure 8</td>
</tr>
<tr>
<td>Input 1dB compression point</td>
<td>IP1dB</td>
<td>-7.5</td>
<td>dBm</td>
<td>See Table 3</td>
</tr>
<tr>
<td>Input 3rd order intercept point</td>
<td>IIP3</td>
<td>-11</td>
<td>dBm</td>
<td>See Table 3</td>
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</table>
3 Schematic Diagram

![Schematic Diagram](schematic_diagram.vsd)

**Table 2** Bill-of-Materials

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
<th>Size</th>
<th>Manufacturer</th>
<th>Comment</th>
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</thead>
<tbody>
<tr>
<td>C1</td>
<td>330</td>
<td>pF</td>
<td>0402</td>
<td>various</td>
<td>DC blocking</td>
</tr>
<tr>
<td>C2</td>
<td>47</td>
<td>nF</td>
<td>0402</td>
<td>various</td>
<td>RF bypass</td>
</tr>
<tr>
<td>C3</td>
<td>330</td>
<td>pF</td>
<td>0402</td>
<td>various</td>
<td>DC blocking</td>
</tr>
<tr>
<td>C4</td>
<td>47</td>
<td>nF</td>
<td>0402</td>
<td>various</td>
<td>RF bypass</td>
</tr>
<tr>
<td>C5</td>
<td>330</td>
<td>pF</td>
<td>0402</td>
<td>various</td>
<td>DC blocking</td>
</tr>
<tr>
<td>L1</td>
<td>470</td>
<td>nH</td>
<td>0603</td>
<td>Tayio Yuden LK1608</td>
<td>RF choke</td>
</tr>
<tr>
<td>R1</td>
<td>12</td>
<td>kΩ</td>
<td>0402</td>
<td>various</td>
<td>Current adjustment</td>
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<tr>
<td>R2</td>
<td>1</td>
<td>kΩ</td>
<td>0402</td>
<td>various</td>
<td>Feedback, matching</td>
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<tr>
<td>R3</td>
<td>180</td>
<td>Ω</td>
<td>0402</td>
<td>various</td>
<td>Stability, output matching</td>
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<td>Q1</td>
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<td>TSLP-7-1</td>
<td>Infineon Technologies</td>
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</table>
4 Measured Graphs

All data displayed here was measured in a 50Ω system. Vcc = Vctrl = 3.0V

![Gain Graph]

**Figure 4** Gain

![Noise Figure Graph]

**Figure 5** Noise Figure
Figure 6 Matching

Figure 7 Matching – Smith Chart
Figure 8  Isolation

Table 3  1dB compression point and IP3

<table>
<thead>
<tr>
<th>Frequency / MHz</th>
<th>Input compression point(^1) / dBm</th>
<th>Input IP3 / dBm</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>-7.5</td>
<td>-11</td>
</tr>
<tr>
<td>150</td>
<td>-8</td>
<td>-11</td>
</tr>
<tr>
<td>250</td>
<td>-7.5</td>
<td>-11</td>
</tr>
<tr>
<td>450</td>
<td>-7</td>
<td>-10.5</td>
</tr>
<tr>
<td>800</td>
<td>-6.5</td>
<td>-10.5</td>
</tr>
</tbody>
</table>

\(^1\)Test condition: -35dBm / tone, \(\Delta f=1\)MHz
5 Evaluation board and layout Information

Figure 9 Picture of Evaluation Board with connector description

Note: The pin “Cadj” may be used to adjust the IC’s current quickly by connecting an external resistor decade. Prior to doing this R1 has to be removed. If the board is intended to be used as received, please leave this pin open.

Figure 10 PCB Layer Information
6 Potential Performance Enhancements

It is possible to increase gain and to reduce noise figure by increasing the current consumption of the IC.

The data displayed here was acquired using a noise figure meter. This is the reason why the gain curves are not as smooth as they would have been when using a network analyzer.

![Figure 11 Gain vs. current consumption](image1)

![Figure 12 NF vs. current consumption](image2)
Appendix 1: ESD protection circuit for system level ESD robustness

Introduction
With the advancement in miniaturization of semiconductor structures, ESD handling capability of the devices is becoming a concern. Increasing ESD handling capability of the I/O ports costs additional chip size and affects the I/O capacitance significantly. This is very important for high frequency devices, especially when high linearity is required. Therefore, tailored and cost effective ESD protection devices can be used to build up an ESD protection circuit. To handle ESD events during assembly, devices normally have on-chip ESD protection according to the device level standards e.g. “Human Body Model” JEDEC 22-A-115. To fulfill the much more stringent system level ESD requirements according to IEC61000-4-2 as shown in Figure 13, the external ESD protection circuit has to handle the majority of the ESD strike. The best external ESD protection is achieved using a TVS diode assisted by additional passive components.

Figure 13  ESD test pulse according to system level specification IEC61000-4-2 – Contact Discharge 15kV

Some examples of RF applications addressed by the Infineon ESD protection proposal are given below:
- FM Radio (76 MHz -110 MHz)
- WLAN 802.11b/g/n (2.4 GHz, Tx ~ +20 dBm)
- Bluetooth (2.4 GHz, Tx ~ +20 dBm)
- Automatic Meter Reading, AMR (900 MHz, TX ~ +20 dBm)
- Remote Keyless Entry, RKE (315 MHz - 434 MHz - 868 MHz - 915 MHz, Tx~13 dBm)
- GPS (1575 MHz, Rx only but can be affected by RF interferer)

For an ESD protection device tailored for medium power RF signals (<= +20 dBm), following requirements are essential:

1. RF requirements
   a) Bidirectional characteristic to handle DC free signals without clipping / signal distortion
   b) A highly symmetrical behavior of the ESD device for positive and negative voltage swings is mandatory to keep the power level of even Harmonics low
   c) Breakdown voltage of 5 V-10V, to avoid signal distortion at high RF voltage swing applied at the TVS diode, located close to the antenna
   d) High linearity
   e) Low leakage current and stable diode capacitance vs. RF voltage swing
   f) Ultra low diode capacitance is mandatory
2. ESD requirements
   a) Lowest dynamic resistance $R_{dyn}$ to offer best protection for the RFIC; $R_{dyn}$ is characterized by
      Transmission Line Pulse (TLP) measurement
   b) Very fast switch-on time (<1nsec) to ground the initial peak of an ESD strike according to IEC61000-4-2
   c) No performance degradation over a large number of ESD zaps (>1000)

Two-step ESD Protection approach

General structure for a 2-step ESD approach according to Figure 14 enables to split the entire ESD current
between the internal and external ESD protection device. The external device is much more robust and handles
the majority of the ESD current. To avoid any impact on the RF behavior of the system and to minimize non
linearity effects, the TVS diode should possess an ultra low device capacitance.

Therefore the bi-directional (symmetrical) Infineon TVS Diode ESD0P2RF is well suited, which provides a diode
 capacitance as low as 0.2 pF and a $R_{dyn}$ of only 1 Ohm. ESD robustness can be improved one step more by
adding a small serial resistor between the external TVS diode and the RF amplifier input. A resistor of ~2.2 Ohm
is a good compromise between additional ESD performance and insertion loss. The TVS diode ESD0P2RF in
combination with the 2.2 Ohm ESD resistor would incur less than 0.23dB insertion loss up to 3 GHz.

For further ESD improvement it is highly recommend to add a serial capacitor (C1). The capacitor cuts off most
of the high energy created by the ESD strike. For better ESD robustness, C1 should be as small as possible,
but has to match to the intended application frequency as well. For a broadband ESD protection
(80MHz…3GHz) C1 should be about 100pF…150pF. Optional matching can be implemented with a serial
inductor L1 for a dedicated frequency. In combination with L1, C1 can be reduced significantly which improves
the ESD performance.
Figure 15 Standard ESD protection topology with optional ESD resistor, blocking capacitor and a serial inductor
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