BGA728L7

Broadband Low Noise Amplifier for FM Radio Applications using BGA728L7

Including a configuration for minimum NF and one for best input matching in a 50 Ohm system
List of Figures

1 Introduction .................................................................................................................6
2 Overview ..................................................................................................................7
3 Circuit optimized for Noise Figure .............................................................................8
   3.1 Summary of Measurement Results .....................................................................8
   3.2 Schematic Diagram .........................................................................................9
   3.3 Measured Graphs ............................................................................................10
4 Circuit optimized for input matching ..........................................................................16
   4.1 Summary of Measurement Results ................................................................16
   4.2 Schematic Diagram .........................................................................................17
   4.3 Measured Graphs ............................................................................................18
5 Evaluation Board ......................................................................................................24

Appendix 1: ESD protection circuit for system level ESD robustness ................................25

Authors 27

List of Figures

Figure 1 FM Radio RF front-end block diagram ............................................................6
Figure 2 Schematic diagram for minimum NF ...............................................................9
Figure 3 Insertion power gain at minimum NF ............................................................10
Figure 4 Noise figure at minimum NF ........................................................................10
Figure 5 Out-of-band Gain at minimum NF .................................................................11
Figure 6 Input matching at minimum NF ....................................................................11
Figure 7 Output matching at minimum NF ...................................................................12
Figure 8 Reverse isolation at minimum NF .................................................................12
Figure 9 Input P1dB compression point at minimum NF .............................................13
Figure 10 Stability factor K at minimum NF ...............................................................13
Figure 11 Stability factor µ1 and µ2 at minimum NF ....................................................14
Figure 12 Output 3rd order intermodulation distortion at minimum NF .....................14
Figure 13 Input and Output impedance at minimum NF .............................................15
Figure 14 Schematic diagram for best input matching ...............................................17
Figure 15 Insertion Power Gain with best input matching .........................................18
Figure 16 Noise figure with best input matching .......................................................18
Figure 17 Out-of-Band attenuation with best input matching ....................................19
Figure 18 Input matching with best input matching ..................................................19
Figure 19 Output Matching with best input matching ...............................................20
Figure 20 Reverse Isolation with best input matching .................................................20
Figure 21 Input 1dB compression point with best input matching ............................21
Figure 22 Stability factor K with best input matching .................................................21
Figure 23 Stability factor µ1 and µ2 of with best input matching .................................22
Figure 24 Output 3rd order intermodulation distortion with best input matching .......22
Figure 25 Input and Output impedance with best input matching ............................23
Figure 26 Picture of Evaluation Board ........................................................................24
Figure 27 PCB Layer Information ...............................................................................24
Figure 28 ESD test pulse according to system level specification IEC61000-4-2 – Contact Discharge 15kV 25
Figure 29 Smart 2-step ESD protection approach based on external and internal ESD protection structure 25
Figure 30 Standard ESD protection topology with optional ESD resistor, blocking capacitor and a serial inductor 26
List of Tables

<table>
<thead>
<tr>
<th>Table</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Table 1</td>
<td>Comparison of the two circuits.</td>
<td>7</td>
</tr>
<tr>
<td>Table 2</td>
<td>Performance with min. NF at Vcc=Von=2.8 V, Vgs=0V.</td>
<td>8</td>
</tr>
<tr>
<td>Table 3</td>
<td>Bill-of-Materials for minimum NF.</td>
<td>9</td>
</tr>
<tr>
<td>Table 4</td>
<td>Performance with best input matching at Vcc=Von=2.8 V, Vgs=0V.</td>
<td>16</td>
</tr>
<tr>
<td>Table 5</td>
<td>Bill-of-Materials for best input matching</td>
<td>17</td>
</tr>
</tbody>
</table>
1 Introduction

FM Radio has a long history to its credit starting from its development in 1933. Today, FM radio is an integral part of almost all mobile phones, including the ultra low cost phones. FM Radio broadcast today is not just used to listen to songs and news, but also used for RDS (Radio Data System) to receive various services including TMC (Traffic Message Channel) which gives traffic information for navigation purposes. In addition, some handsets are being equipped with FM Radio transmission capability to send voice signals to car audio systems or Hi-Fi systems.

Therefore, FM system design in a phone is getting more and more complex. Till recently, the headset served as the antenna for FM Radio reception, wherein the antenna size is a bit relaxed and the antenna performance is satisfactory. A new trend has emerged to be able to use FM radio also without the headset, wherein the antenna embedded into the phone. But in this case, the space constraint poses a challenge on the antenna design. Shrinking the size of the antenna reduces antenna gain and bandwidth, which introduces a high loss into the system which deteriorates the receiver performance, namely the receiver sensitivity. This application note presents Infineon solution to the aforementioned challenges leading to the design of a high performance RF front end with the lowest power consumption.

A general topology for the RF front-end of FM Radio is as shown in Figure 1. Variations of the given application schematic are possible based on the complete system design and concept. These may include systems with only external headset antenna, only internal embedded antenna or both antennas co-existing. Infineon offers the complete chain of RF front-end parts between the antenna and the receiver IC for FM Radio, which include ESD protection devices, RF switches and LNAs. The focus of this application note is Low Noise Amplifier for FMR.

![Figure 1 FM Radio RF front-end block diagram](image)

An ESD protection circuit is needed at the antenna to protect the front-end system from ESD strikes, as the antenna is susceptible to ESD events. For more information please see Appendix 1.

A Single Pole Double Throw or SPDT RF switch is used to toggle between the headset and embedded antenna. The switch being in front of the LNA and in the vicinity of strong cellular signals should introduce minimal loss to the system and offer high linearity. To know more about Infineon solutions for RF Switches, please refer to application note AN175.

A Low Noise Amplifier or LNA follows the switch, which significantly reduces the noise figure of the whole receiver chain, thereby improving the receiver sensitivity. However, there are a few challenges in the design of the LNA for this purpose. Using it in a hand held device demands low current consumption and high linearity due to the coexistence of cellular bands. In a system with internal antenna, due to the very small size, the antenna impedance is very high and thus the LNA has to be matched to this high impedance and in addition offer a low noise figure.
2 Overview

This application note shows the performance of Infineon’s BGA728L7 as an LNA for FM radio.

BGA728L7 is a broadband MMIC originally targeted at mobile TV applications but may also be used for FM radio applications. It offers high integration including biasing, on/off switch and a low gain mode.

The application note is divided into two parts. The first part shows the MMIC in a configuration that is optimized for low noise figure, in the other part the LNA is optimized for a good matching to 50 Ohms.

Comparison of the two circuits. Table 1 gives a quick overview of the performance difference of the two circuits. Test conditions are the same for both configurations.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Optimized for</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Noise Figure</td>
<td>Input matching</td>
</tr>
<tr>
<td>Noise figure / dB</td>
<td>1.3</td>
<td>1.65</td>
</tr>
<tr>
<td>Gain / dB</td>
<td>14.3</td>
<td>16.4</td>
</tr>
<tr>
<td>Input return loss / dB</td>
<td>7.3</td>
<td>12.2</td>
</tr>
<tr>
<td>Output return loss / dB</td>
<td>9.7</td>
<td>9.6</td>
</tr>
<tr>
<td>Input 1dB compression point / dBm</td>
<td>-9</td>
<td>-6.5</td>
</tr>
</tbody>
</table>
3 Circuit optimized for Noise Figure

3.1 Summary of Measurement Results

Table 2 Performance with min. NF at Vcc=Von=2.8 V, Vgs=0V

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
<th>Note/Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency Range</td>
<td>Freq</td>
<td>78-108</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>DC Voltage</td>
<td>Vcc</td>
<td>2.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>DC Current</td>
<td>Icc</td>
<td>5.7</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Gain</td>
<td>G</td>
<td>14.3</td>
<td>dB</td>
<td>Pin=-30dBm</td>
</tr>
<tr>
<td>Noise Figure</td>
<td>NF</td>
<td>1.3</td>
<td>dB</td>
<td>SMA and PCB loss of 0.1 dB included</td>
</tr>
<tr>
<td>Input Return Loss</td>
<td>RLin</td>
<td>7.3</td>
<td>dB</td>
<td>Pin=-30dBm</td>
</tr>
<tr>
<td>Output Return Loss</td>
<td>RLout</td>
<td>9.7</td>
<td>dB</td>
<td>Pin=-30dBm</td>
</tr>
<tr>
<td>Reverse Isolation</td>
<td>IRev</td>
<td>28.8</td>
<td>dB</td>
<td>Pin=-30dBm</td>
</tr>
<tr>
<td>Input P1dB</td>
<td>IP1dB</td>
<td>-9.3</td>
<td>dBm</td>
<td>Measured @ 100MHz</td>
</tr>
<tr>
<td>Output P1dB</td>
<td>OP1dB</td>
<td>4</td>
<td>dBm</td>
<td></td>
</tr>
<tr>
<td>Input IP3</td>
<td>IIP3</td>
<td>-7.2</td>
<td>dBm</td>
<td>In-band, f1=100MHz, f2=101MHz, Pin=-30dBm</td>
</tr>
<tr>
<td>Output IP3</td>
<td>OIP3</td>
<td>7.1</td>
<td>dBm</td>
<td></td>
</tr>
<tr>
<td>Stability</td>
<td>k</td>
<td>&gt;1</td>
<td>--</td>
<td>Unconditionally stable from DC to 10GHz</td>
</tr>
</tbody>
</table>
3.2 Schematic Diagram

![Schematic Diagram](image)

Figure 2  Schematic diagram for minimum NF.

Table 3  Bill-of-Materials for minimum NF

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
<th>Size</th>
<th>Manufacturer</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>270</td>
<td>pF</td>
<td>0402</td>
<td>Various</td>
<td>Input matching</td>
</tr>
<tr>
<td>C4</td>
<td>1</td>
<td>µF</td>
<td>0402</td>
<td>Various</td>
<td>HF to ground</td>
</tr>
<tr>
<td>C5</td>
<td>10</td>
<td>nF</td>
<td>0402</td>
<td>Various</td>
<td>HF to ground</td>
</tr>
<tr>
<td>C6</td>
<td>9</td>
<td>pF</td>
<td>0402</td>
<td>Various</td>
<td>Output matching</td>
</tr>
<tr>
<td>L1</td>
<td>470</td>
<td>nH</td>
<td>0603</td>
<td>Tayio Yuden LK</td>
<td>DC Feed/ Input matching</td>
</tr>
<tr>
<td>L2</td>
<td>150</td>
<td>nH</td>
<td>0402</td>
<td>Murata LQG15A</td>
<td>Output matching</td>
</tr>
<tr>
<td>N1</td>
<td>BGA728L7</td>
<td></td>
<td></td>
<td>Infineon Technologies</td>
<td>SiGe:C LNA MMIC</td>
</tr>
</tbody>
</table>
3.3 Measured Graphs

![Insertion Power Gain InBand](image)

**Figure 3** Insertion power gain at minimum NF.

![Noise figure](image)

**Figure 4** Noise figure at minimum NF.
Out of band attenuation

Figure 5 Out-of-band Gain at minimum NF

Input Matching

Figure 6 Input matching at minimum NF.
Figure 7  Output matching of at minimum NF.

Figure 8  Reverse isolation at minimum NF.
Figure 9  Input P1dB compression point at minimum NF.

Figure 10  Stability factor K at minimum NF.
Figure 11  Stability factor $\mu_1$ and $\mu_2$ at minimum NF.

Figure 12  Output 3rd order intermodulation distortion at minimum NF.
Figure 13  Input and Output impedance at minimum NF.
4 Circuit optimized for input matching

4.1 Summary of Measurement Results

Table 4 Performance with best input matching at Vcc=Von=2.8 V, Vgs=0V

<table>
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<th>Note/Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
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<td></td>
</tr>
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<td>Vcc</td>
<td>2.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>DC Current</td>
<td>Icc</td>
<td>5.8</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Gain</td>
<td>G</td>
<td>14.6</td>
<td>dB</td>
<td>Pin=-30dBm</td>
</tr>
<tr>
<td>Noise Figure</td>
<td>NF</td>
<td>1.65</td>
<td>dB</td>
<td>SMA and PCB loss of 0.10 dB included</td>
</tr>
<tr>
<td>Input Return Loss</td>
<td>RLin</td>
<td>12.2</td>
<td>dB</td>
<td>Pin=-30dBm</td>
</tr>
<tr>
<td>Output Return Loss</td>
<td>RLout</td>
<td>9.6</td>
<td>dB</td>
<td>Pin=-30dBm</td>
</tr>
<tr>
<td>Reverse Isolation</td>
<td>IRev</td>
<td>28.8</td>
<td>dB</td>
<td>Pin=-30dBm</td>
</tr>
<tr>
<td>Input P1dB</td>
<td>IP1dB</td>
<td>-10.4</td>
<td>dBm</td>
<td>Measured @ 100MHz</td>
</tr>
<tr>
<td>Output P1dB</td>
<td>OP1dB</td>
<td>3.7</td>
<td>dBm</td>
<td></td>
</tr>
<tr>
<td>Input IP3</td>
<td>IIP3</td>
<td>-6.4</td>
<td>dBm</td>
<td>In-band, f1=100MHz, f2=101MHz, Pin=-30dBm</td>
</tr>
<tr>
<td>Output IP3</td>
<td>OIP3</td>
<td>8.2</td>
<td>dBm</td>
<td></td>
</tr>
<tr>
<td>Stability</td>
<td>k</td>
<td>&gt;1</td>
<td></td>
<td>Unconditionally stable from DC to 10GHz</td>
</tr>
</tbody>
</table>
4.2 Schematic Diagram

![Schematic Diagram]

Figure 14 Schematic diagram for best input matching.

Table 5 Bill-of-Materials for best input matching

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
<th>Unit Size</th>
<th>Manufacturer</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>39</td>
<td>pF</td>
<td>0402</td>
<td>Various</td>
<td>Input matching/DC block</td>
</tr>
<tr>
<td>C4</td>
<td>1</td>
<td>uF</td>
<td>0402</td>
<td>Various</td>
<td>HF to ground</td>
</tr>
<tr>
<td>C5</td>
<td>10</td>
<td>nF</td>
<td>0402</td>
<td>Various</td>
<td>HF to ground</td>
</tr>
<tr>
<td>C6</td>
<td>9</td>
<td>pF</td>
<td>0402</td>
<td>Various</td>
<td>Output matching</td>
</tr>
<tr>
<td>L1</td>
<td>180</td>
<td>nH</td>
<td>0402</td>
<td>Murata LQG15A</td>
<td>DC Feed/ Input matching</td>
</tr>
<tr>
<td>L2</td>
<td>150</td>
<td>nH</td>
<td>0402</td>
<td>Murata LQG15A</td>
<td>Output matching</td>
</tr>
<tr>
<td>N1</td>
<td>BGA728L7</td>
<td>TSLP-7-6</td>
<td>Infineon Technologies</td>
<td>SiGe:C MMIC LNA</td>
<td></td>
</tr>
</tbody>
</table>
4.3 Measured Graphs

Figure 15  Insertion Power Gain with best input matching

Figure 16  Noise figure with best input matching
BGA728L7 as a LNA for FM Radio

Circuit optimized for input matching

**Figure 17** Out-of-Band attenuation with best input matching

**Figure 18** Input matching with best input matching
**Figure 19** Output Matching with best input matching

**Figure 20** Reverse Isolation with best input matching
BGA728L7 as a LNA for FM Radio
Circuit optimized for input matching

Figure 21  Input 1dB compression point with best input matching

Figure 22  Stability factor K with best input matching.
Figure 23  Stability factor $\mu_1$ and $\mu_2$ with best input matching

Figure 24  Output 3rd order intermodulation distortion with best input matching
Z Parameters Input output matching

Swp Max
110MHz

110 MHz
r 1.77503
x 0.523561

78 MHz
r 0.941334
x -0.010687

110 MHz
r 1.64196
x 0.088891

78 MHz
r 0.924681
x -0.320277

Swp Min
78MHz

Figure 25  Input and Output impedance with best input matching.
5 Evaluation Board

Figure 26 Picture of Evaluation Board

Figure 27 PCB Layer Information
Appendix 1: ESD protection circuit for system level ESD robustness

Introduction

With the advancement in miniaturization of semiconductor structures, ESD handling capability of the devices is becoming a concern. Increasing ESD handling capability of the I/O ports costs additional chip size and affects the I/O capacitance significantly. This is very important for high frequency devices, especially when high linearity is required. Therefore, tailored and cost effective ESD protection devices can be used to build up an ESD protection circuit. To handle ESD events during assembly, devices normally have on-chip ESD protection according to the device level standards e.g. “Human Body Model” JEDEC 22-A-115. To fulfill the much more stringent system level ESD requirements according to IEC61000-4-2 as shown in Figure 28, the external ESD protection circuit has to handle the majority of the ESD strike. The best external ESD protection is achieved using a TVS diode assisted by additional passive components.

![Reference Pulse 15kV contact discharge according IEC61000-4-2](image)

The reference pulse used for ESD testing according to IEC61000-4-2. The pulse is a 1.5kV contact discharge with a peak current of 57.68A and a duration of 1.507 nanoseconds.

Figure 28 ESD test pulse according to system level specification IEC61000-4-2 – Contact Discharge 15kV

Some examples of RF applications addressed by the Infineon ESD protection proposal are given below:

- FM Radio (76 MHz -110 MHz)
- WLAN 802.11b/g/n (2.4 GHz, Tx ~ +20 dBm)
- Bluetooth (2.4 GHz, Tx ~ +20 dBm)
- Automatic Meter Reading, AMR (900 MHz, TX ~ +20 dBm)
- Remote Keyless Entry, RKE (315 MHz - 434 MHz - 868 MHz - 915 MHz, Tx~13 dBm)
- GPS (1575 MHz, Rx only but can be affected by RF interferer)

For an ESD protection device tailored for medium power RF signals (<= +20 dBm), following requirements are essential:

1. RF requirements
   a) Bidirectional characteristic to handle DC free signals without clipping / signal distortion
   b) A highly symmetrical behavior of the ESD device for positive and negative voltage swings is mandatory to keep the power level of even Harmonics low
   c) Breakdown voltage of 5 V-10V, to avoid signal distortion at high RF voltage swing applied at the TVS diode, located close to the antenna
   d) High linearity
   e) Low leakage current and stable diode capacitance vs. RF voltage swing
   f) Ultra low diode capacitance is mandatory
2. ESD requirements
   a) Lowest dynamic resistance \( R_{\text{dyn}} \) to offer best protection for the RFIC; \( R_{\text{dyn}} \) is characterized by Transmission Line Pulse (TLP) measurement
   b) Very fast switch-on time (\(<1\text{ns})\) to ground the initial peak of an ESD strike according to IEC61000-4-2
   c) No performance degradation over a large number of ESD zaps (\(>1000\))

Two-step ESD Protection approach

General structure for a 2-step ESD approach according to Figure 29 enables to split the entire ESD current between the internal and external ESD protection device. The external device is much more robust and handles the majority of the ESD current. To avoid any impact on the RF behavior of the system and to minimize non linearity effects, the TVS diode should possess an ultra low device capacitance.

Therefore the bi-directional (symmetrical) Infineon TVS Diode ESD0P2RF is well suited, which provides a diode capacitance as low as 0.2 pF and a \( R_{\text{dyn}} \) of only 1 Ohm. ESD robustness can be improved one step more by adding a small serial resistor between the external TVS diode and the RF amplifier input. A resistor of \(~2.2\) Ohm is a good compromise between additional ESD performance and insertion loss. The TVS diode ESD0P2RF in combination with the 2.2 Ohm ESD resistor would incur less than 0.23dB insertion loss up to 3 GHz.

![Figure 29 Smart 2-step ESD protection approach based on external and internal ESD protection structure](image)

For further ESD improvement it is highly recommend to add a serial capacitor (C1). The capacitor cuts off most of the high energy created by the ESD strike. For better ESD robustness, C1 should be as small as possible, but has to match to the intended application frequency as well. For a broadband ESD protection (80MHz...3GHz) C1 should be about 100pF...150pF. Optional matching can be implemented with a serial inductor L1 for a dedicated frequency. In combination with L1, C1 can be reduced significantly which improves the ESD performance.

![Figure 30 Standard ESD protection topology with optional ESD resistor, blocking capacitor and a serial inductor](image)
Authors

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Dr. Lin Chih-I, Senior Staff Engineer of “RF and Protection Devices”
Dietmar Stolz, Staff Engineer of Business Unit “RF and Protection Devices”