Application Note No. 145

Low Cost, 3 V, 2.33 GHz Class A SDARS Active Antenna Amplifier Output Stage using the Infineon BFP450 Transistor

RF & Protection Devices

Never stop thinking

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Revision History: 2008-02-21, Rev. 1.2

Previous Version: 2005-03-01, Rev. 1.1

Page	Subjects (major changes since last revision)
All	Small changes in figure descriptions

1 Low Cost, 3 V, 2.33 GHz Class A SDARS Active Antenna Amplifier Output Stage using the Infineon BFP450 Transistor

Overview

BFP450 SIEGET transistor is investigated as an alternative to the BFP650 SiGe Low Noise Transistor for the output stage of an SDARS active antenna LNA. A key parameter is +20 dBm P_{1dB} capability in the output stage. The PCB used is standard FR4 material & "0402" case sizes components are used. A total of approximately 50 mm² of PCB area is required, the total component count, including the BFP450 and all passives, is 13. Net result is: BFP450 provides slightly more available output power than BFP650 at comparable DC operating points; however, BFP450 has less gain and higher noise figure. See table below. Both devices are in SOT343 package with identical pin-outs. Note output power is "voltage limited" = e.g. if bias resistors were changed after power supply voltage was increased, one should be able to hit +20 dBm OP_{1dB} with less than 100 mA current.

Table 1 Comparison of BFP650 and BFP450 as SDARS active antenna output stage at 2.33 GHz

Device	DC Operating Point	Small Signal Gain, dB	Output P_{1dB}, dBm	Noise Figure, dB
BFP450	3 V, 76 mA, V_{CE} = 2.7 V	9.8	+18.7	2.7
BFP450	3.7 V, 100 mA, V_{CE} = 3.2 V	10.0	+20.5	Not tested
BFP650	3.0 V, 53 mA	14.1	≈ +18.0	1.3

Summary

- Achieved 9.8 dB gain, 2.7 dB Noise Figure over the 2320 - 2345 MHz band, drawing 76 mA @ 3.0 V, or 100 mA @ 3.7 V. Amplifier is unconditionally stable from 5 MHz to 8 GHz. Output P_{1dB} = +18.7 dBm @ 3 V, 76 mA or +20.5 dBm @ 3.7 V, 100 mA.
- BFP450 seems to show a slight advantage in Output P_{1dB} as compared to the BFP650. However, gain of BFP450 in same PC board is approx. 4 dB lower, and noise figure of BFP450 is 1.4 dB higher.

Block Diagram of Application

Typical SDARS Active Antenna LNA
2320 - 2332.5 MHz (SIRIUS, 3 Stages)
2332.5 - 2345 MHz (XM Radio, 2 Stages)

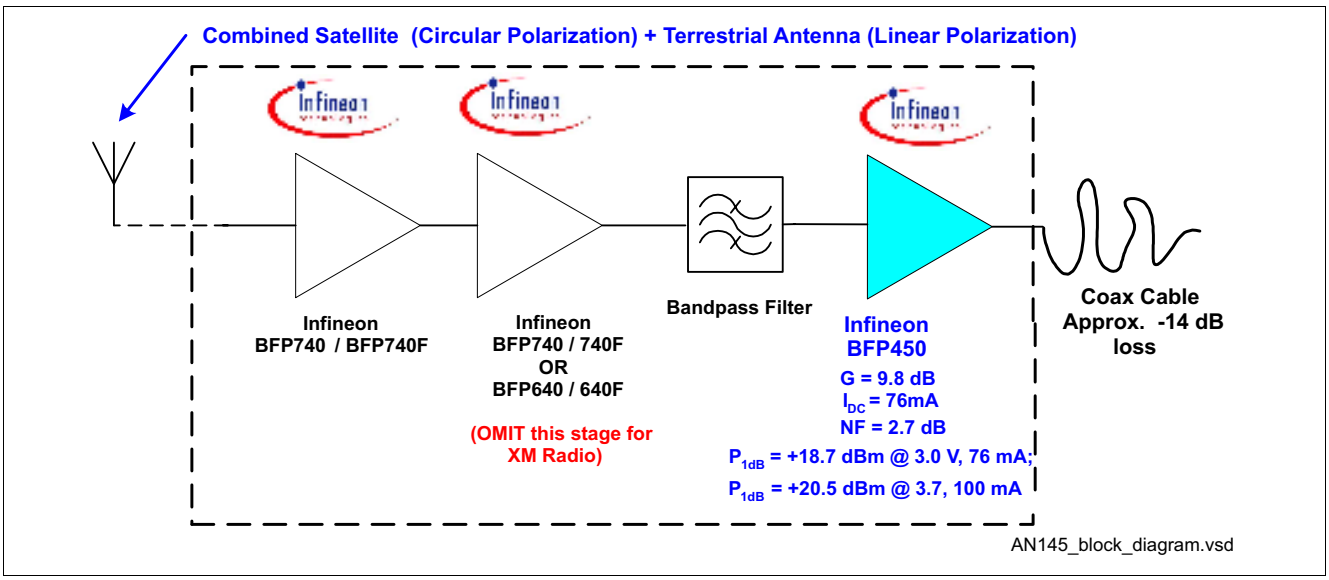


Figure 1 Block Diagram of Application

PC Board Cross Sectional Diagram

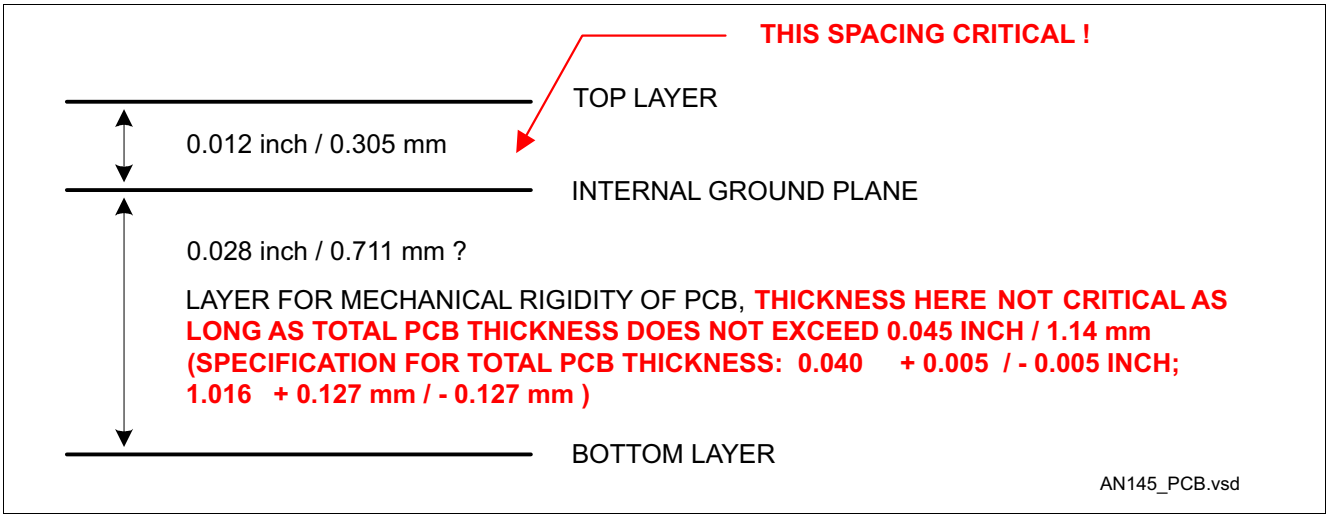


Figure 2 PCB - Cross Sectional Diagram

Schematic Diagram

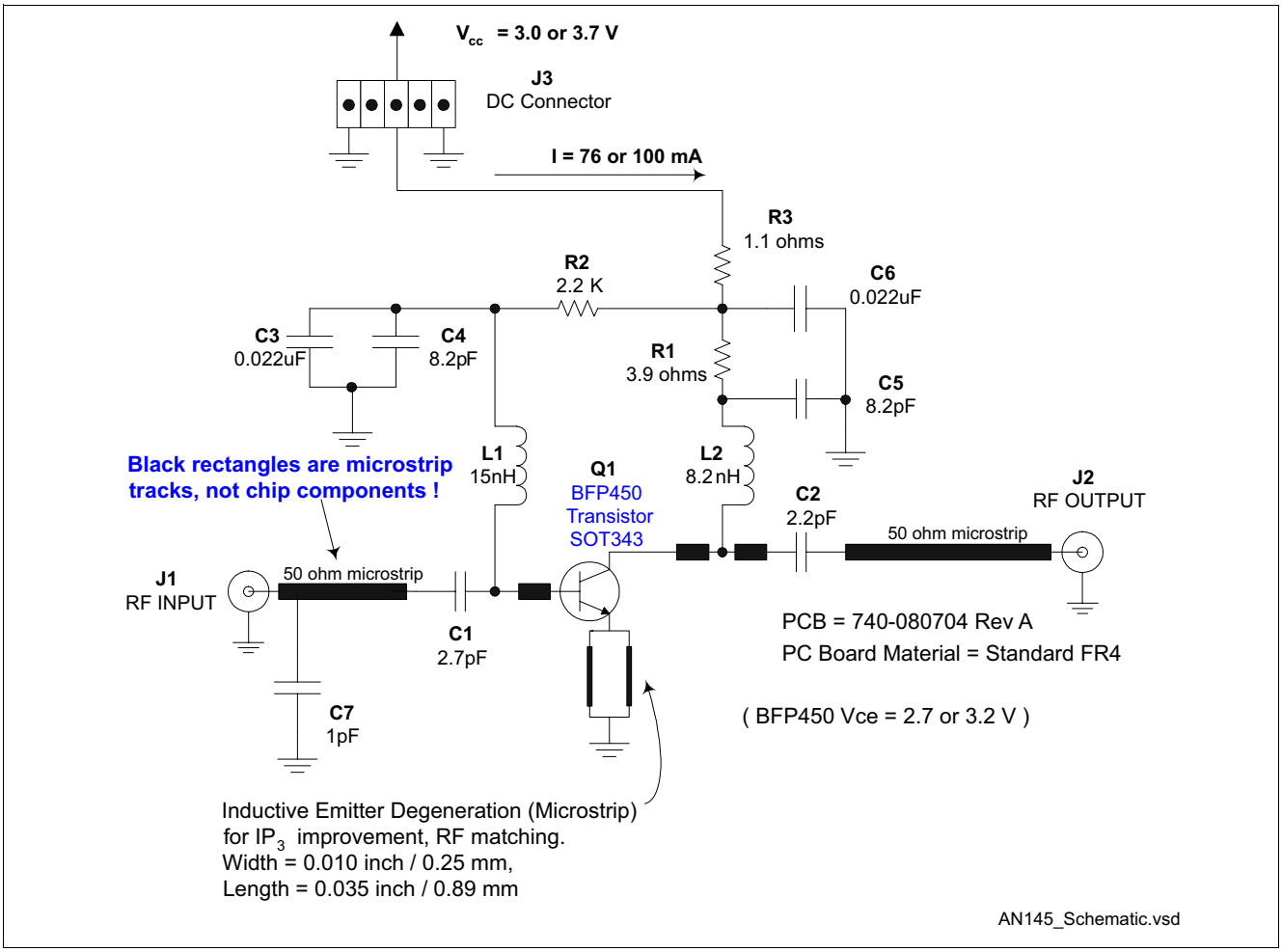


Figure 3 Schematic Diagram

Summary of Data

T = 25 °C, Network analyzer source power ≈ -30 dBm

Table 2 Summary of Results

Parameter	Result	Comments
Frequency Range	Under 2320 to 2345 MHz	Covers both XM Radio and SIRIUS frequency bands.
DC Current	100 mA @ 3.7 V 76 mA @ 3.0 V	Note power supply voltage is measured directly across PCB supply line and ground, to eliminate voltage drop across wire harness.
Gain	9.8 dB @ 2332.5 MHz	
Noise Figure	2.7 dB @ 2332.5 MHz	These values do not extract PCB losses, etc. resulting from FR4 board an passives used on PCB - these results are at input SMA connector.
Input P_{1dB}	+11.7 dBm @ 3.7 V +9.9 dBm @ 3.0 V	Measured @ 2332.5 MHz. See **Table 4** and **Table 5**.
Output P_{1dB}	+20.5 dBm @ 3.7 V +18.7 dBm @ 3.0 V	See **Table 4** and **Table 5**.
Collector Efficiency at 1 dB Compression Point	30.3 % @ 3.7 V 32.5 % @ 3.0 V	Decent results for a Class A amplifier
Input 3rd Order Intercept	+22.9 dBm @ 2332 MHz	**Figure 14** and **Figure 15**. Measured at 3.0 V.
Output 3rd Order Intercept	+32.6 dBm @ 2332 MHz	**Figure 14** and **Figure 15**. Measured at 3.0 V.
Input Return Loss	9.0 dB @ 2332.5 MHz	
Output Return Loss	9.8 dB @ 2332.5 MHz	
Reverse Isolation	14.6 dB @ 2332.5 MHz	

Noise Figure, Plot, 2232.5 MHz to 2432.5 MHz, Center of Plot (x-axis) is 2332.5 MHz.

Rohde & Schwarz FSEK3

01 Mar 2005

Noise Figure

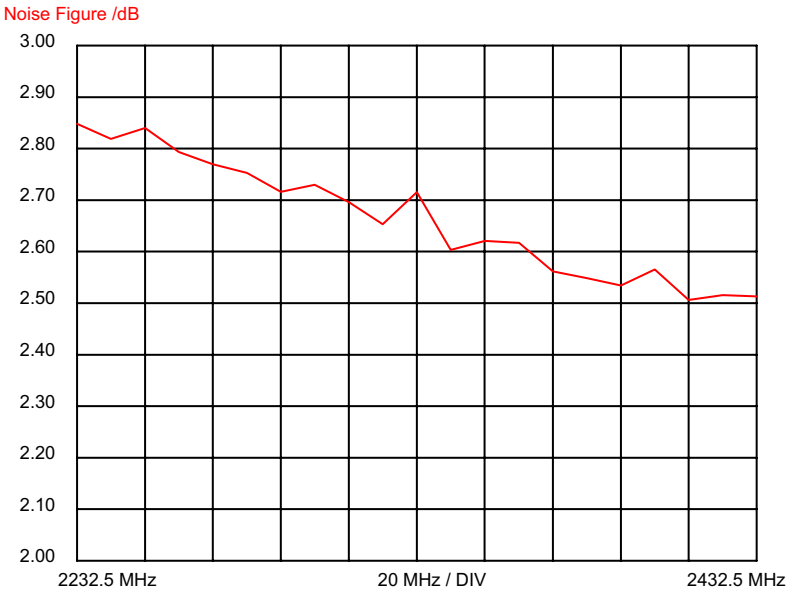
EUT Name:	BFP450 SDARS Output Stage
Manufacturer:	Infineon Technologies
Operating Conditions:	V = 3.0 V, I =76 mA, T = 25 C
Operator Name:	Gerard Wevers
Test Specification:	2.33 GHz SDARS band
Comment:	On BFP740 PCB 740-080704 RevA 1 March 2005

Analyzer

RF Att:	0.00 dB	RBW :	1 MHz	Range:	40.00 dB
Ref Lvl:	-41.00 dBm	VBW :	100 Hz	Ref Lvl auto:	ON

Measurement

2nd stage corr: ON	Mode: Direct	ENR: HP346A.ENR



AN145_plot_nf.vsd

Figure 4 Noise Figure

Noise Figure, Tabular Data

From Rohde & Schwarz FSEK3 + FSEM30
System Preamplifier = MITEQ SMC-02

Table 3 Noise Figure

Frequency	Noise Figure
2232.5 MHz	2.85 dB
2242.5 MHz	2.82 dB
2252.5 MHz	2.84 dB
2262.5 MHz	2.79 dB
2272.5 MHz	2.77 dB
2282.5 MHz	2.75 dB
2292.5 MHz	2.72 dB
2302.5 MHz	2.73 dB
2312.5 MHz	2.70 dB
2322.5 MHz	2.65 dB
2332.5 MHz	2.72 dB
2342.5 MHz	2.60 dB
2352.5 MHz	2.62 dB
2362.5 MHz	2.62 dB
2372.5 MHz	2.56 dB
2382.5 MHz	2.55 dB
2392.5 MHz	2.53 dB
2402.5 MHz	2.57 dB
2412.5 MHz	2.51 dB
2422.5 MHz	2.52 dB
2432.5 MHz	2.51 dB

Scanned Image of PC Board

Figure 5 Image of PC Board

Scanned Image of PC Board, Close-In Shot.

Total PCB area used ≅ 50 mm².

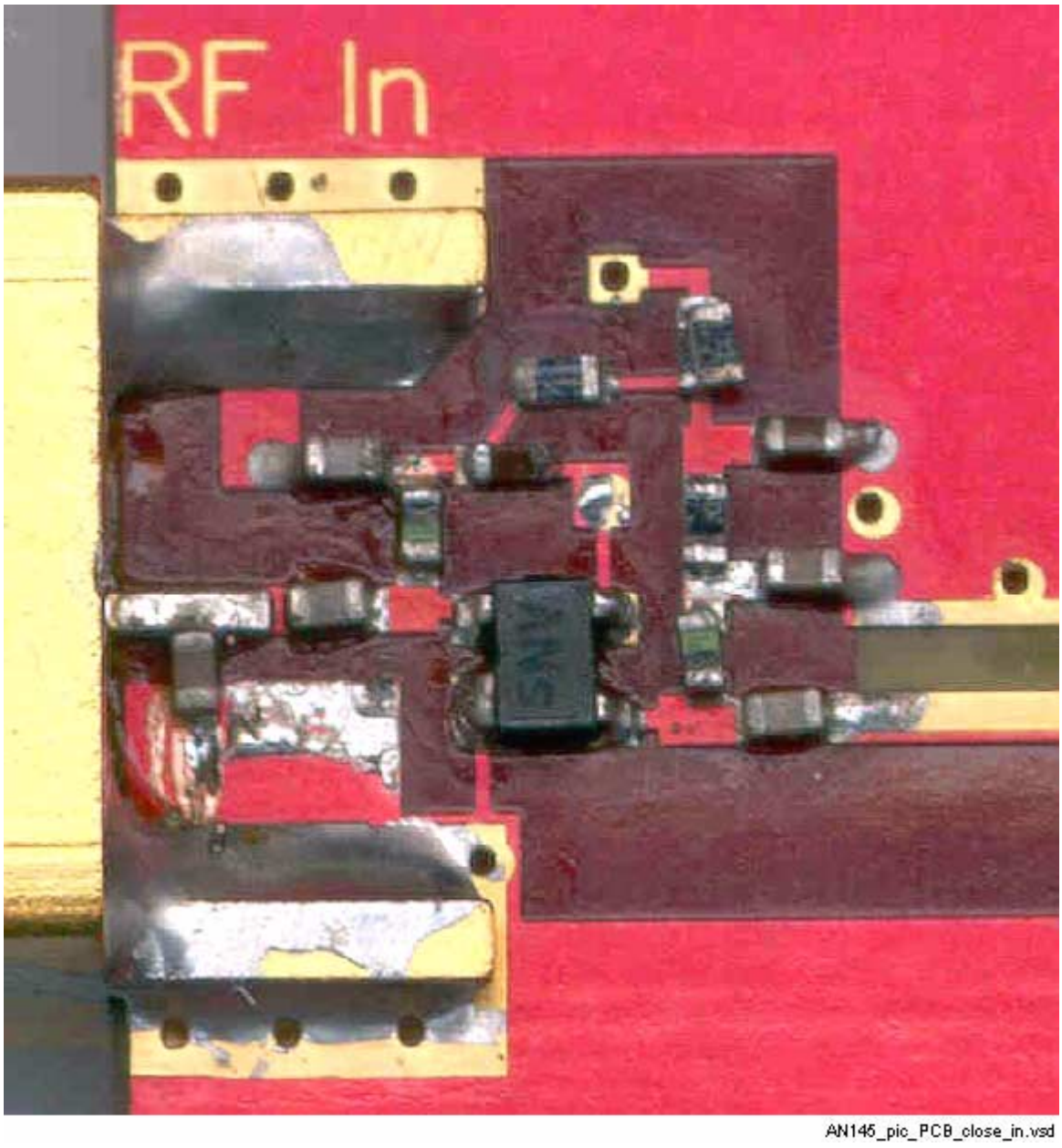


Figure 6 Image of PC Board, Close-In Shot

Stability

Rohde and Schwarz ZVC Network Analyzer calculates and plots Stabilty Factor "K" in real time. Note minimum K value is approximately 1.04 over the 5 MHz to 8 GHz range. Since inductive emitter degeneration is used, S parameters should be measured up to at least 15 GHz to verify K > 1, B_1 > 0 up to 15 GHz.

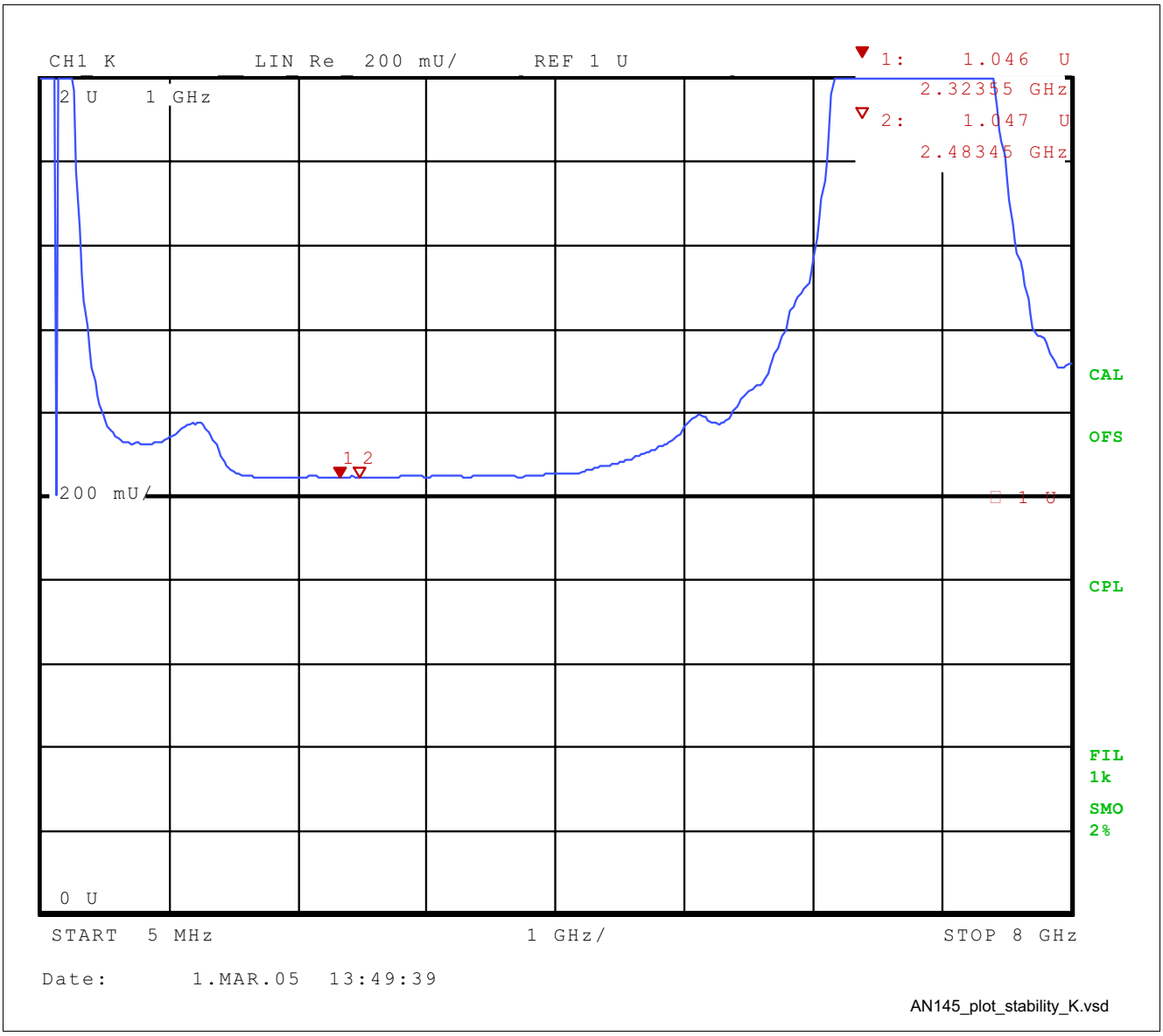


Figure 7 Plot of K(f)

Gain Compression

Amplifier is checked for 1 dB compression point at V_{CC} = 3.0 V, I = 76 mA (with V_{CE} = 2.7 V), and at V_{CC} = 3.7 V, I = 100 mA (with V_{CE} = 3.2 V). An Agilent power meter was used to ensure accurate power levels are measured (as opposed to using Vector Network Analyzer in "Power Sweep" mode).

For 3.0 V power supply voltage $\Rightarrow O_{P1dB} \cong$ +18.7 dBm, or 74.1 mW
Collector efficiency at this point is 74.1 mW / (3 V x 76 mA) = 32.5 %

For 3.7 V power supply voltage $\Rightarrow O_{P1dB} \cong$ +20.5 dBm, or 112.2 mW
Collector efficiency at this point is 112.2 mW / (3.7 V x 100 mA) = 30.3 %

Table 4 3.0 V, 76 mA

P_{IN}, dBm	P_{OUT}, dBm	Gain
0	+9.9	9.9
+5.0	+14.8	9.8
+6.0	+15.8	9.8
+7.0	+16.6	9.6
+8.0	+17.5	9.5
+9.0	+18.2	9.2
+10.0	+18.8	8.8
+11.0	+19.2	8.2

Table 5 3.7 V, 100 mA

P_{IN}, dBm	P_{OUT}, dBm	Gain
0	+10.1	10.1
+5.0	+15.0	10.0
+6.0	+16.0	10.0
+7.0	+16.9	9.9
+8.0	+17.8	9.8
+9.0	+18.7	9.7
+10.0	+19.5	9.5
+11.0	+20.3	9.3
+12.0	+20.9	8.9

Please Note - all plots are taken from ZVC Network Analyzer with amplifier DC bias set to 3.0 V, 76 mA.

Input Return Loss, Log Mag

5 MHz - 8 GHz

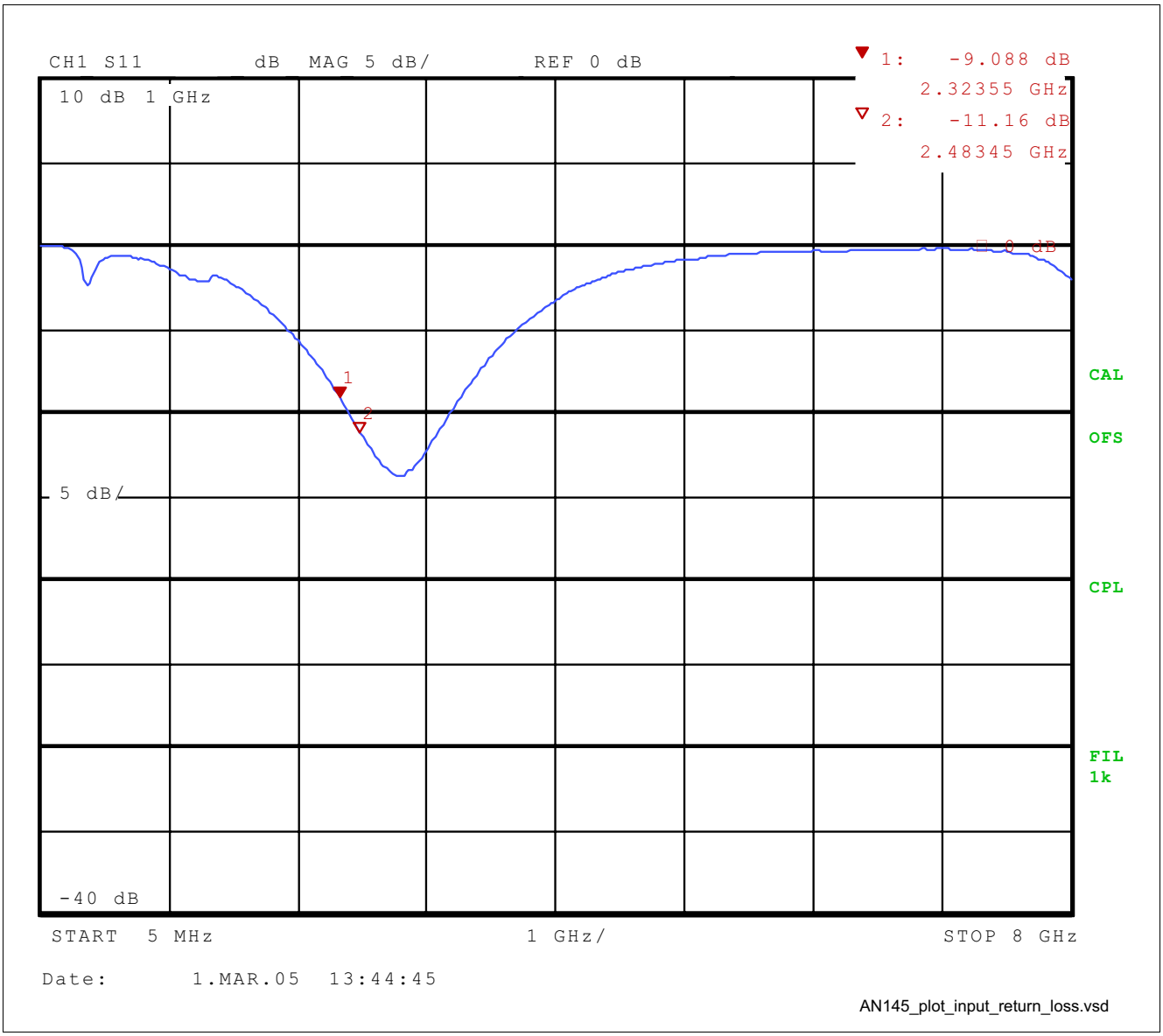


Figure 8 Plot of Input Return Loss

Input Return Loss, Smith Chart

Reference Plane = Input SMA Connector on PC Board
5 MHz - 8 GHz

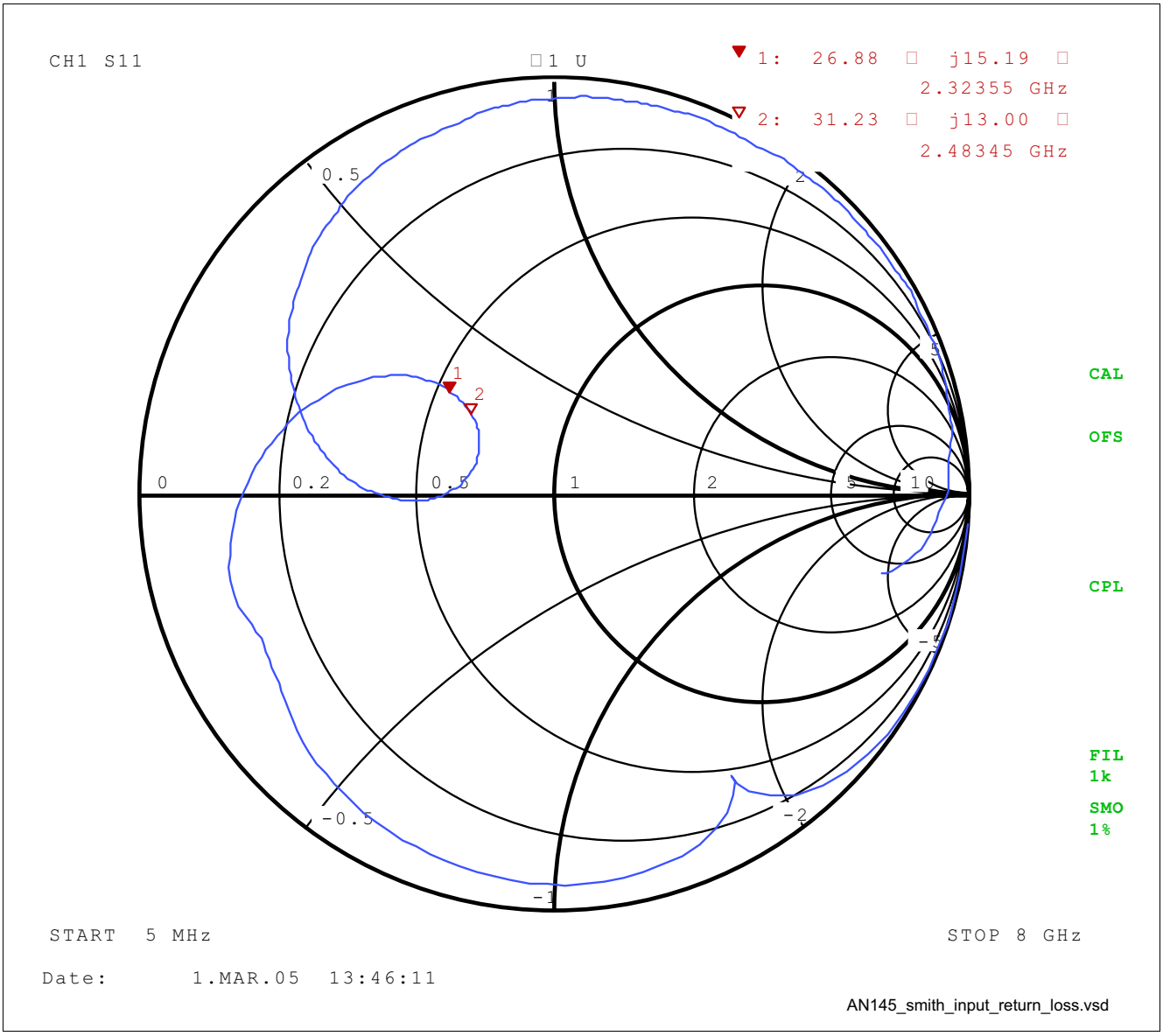


Figure 9 Smith Chart of Input Return Loss

Forward Gain, Wide Sweep

5 MHz - 8 GHz

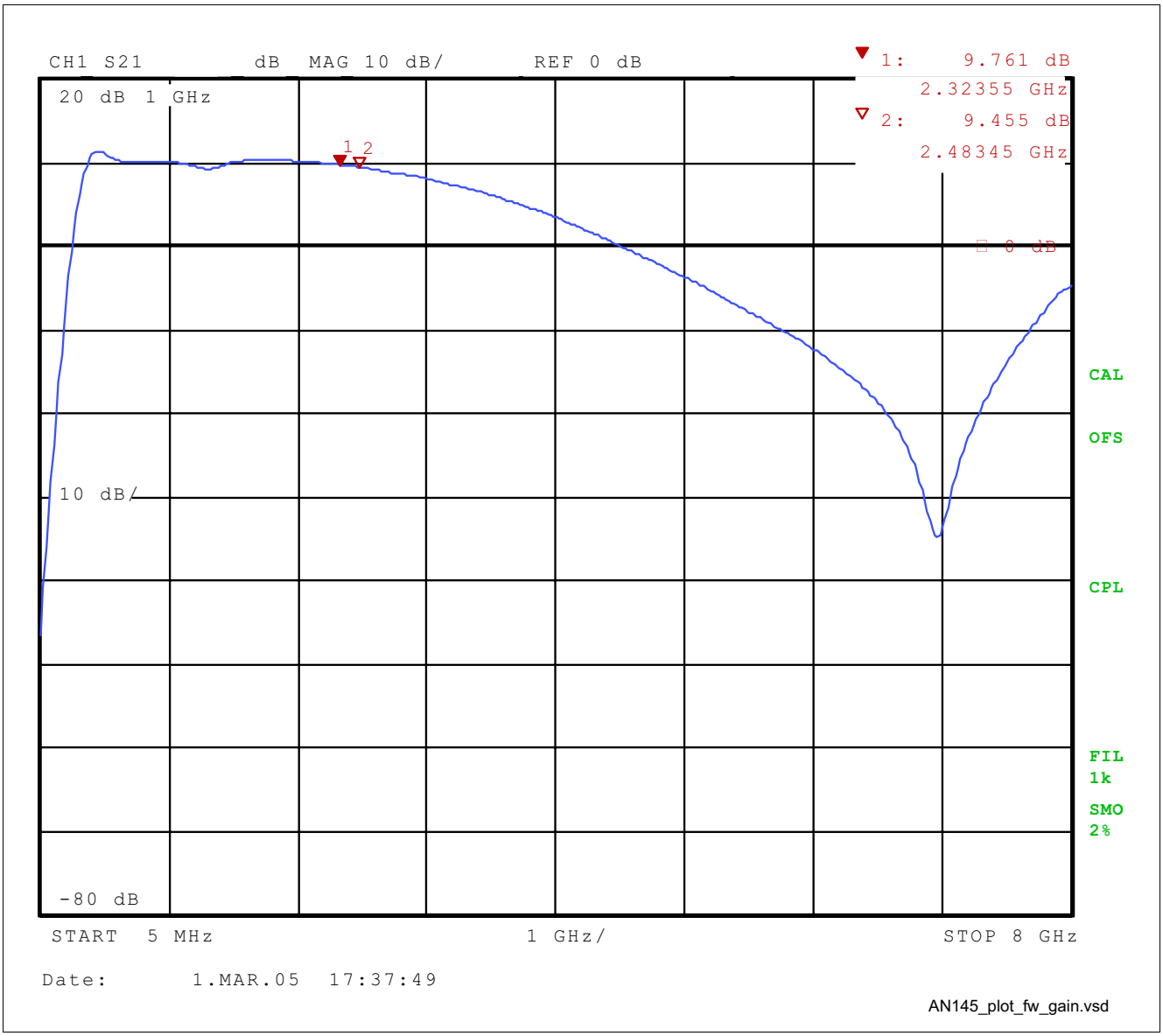


Figure 10 Plot of Forward Gain

Reverse Isolation

5 MHz - 8 GHz

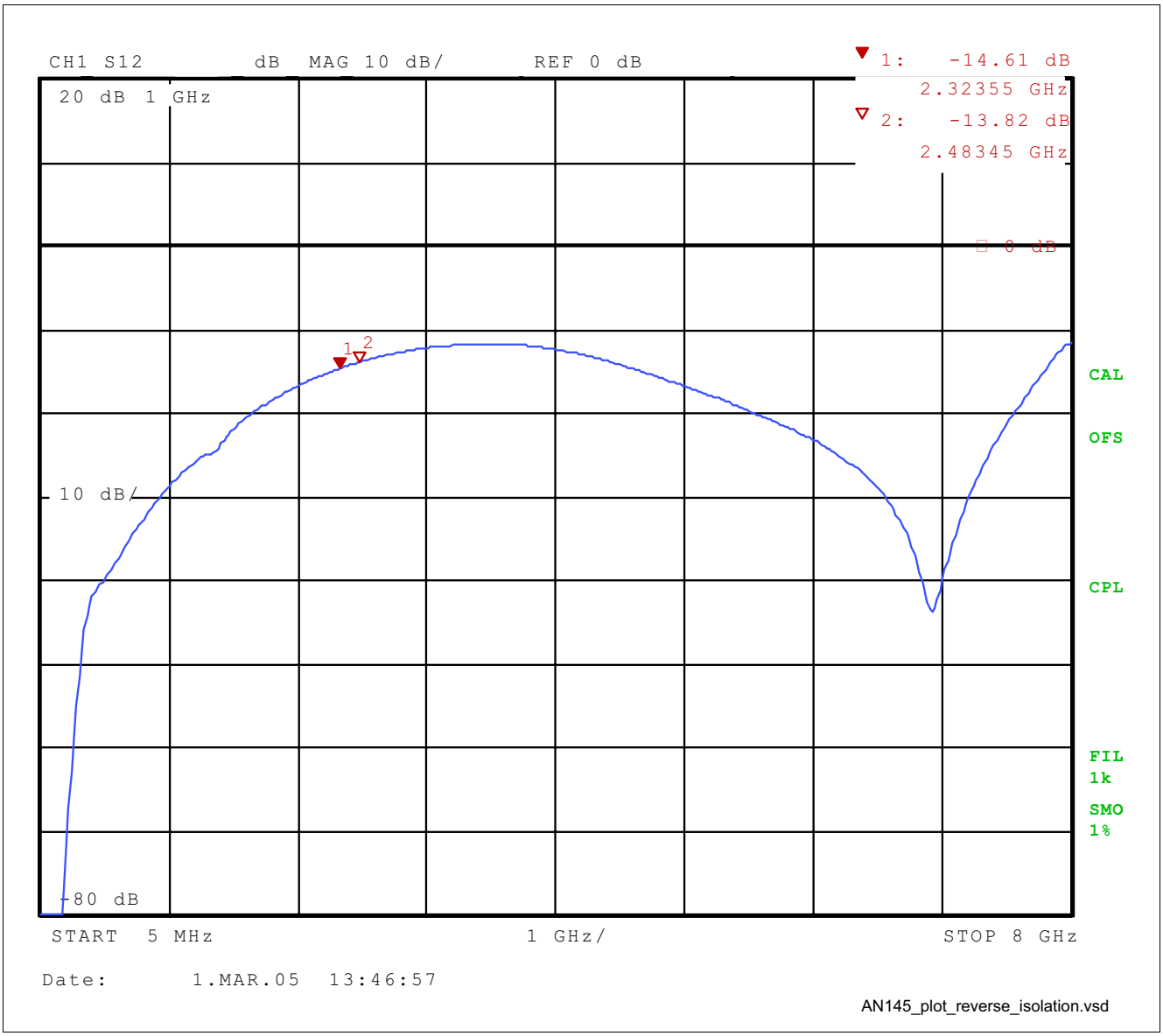


Figure 11 Plot of Reverse Isolation

Output Return Loss, Log Mag

5 MHz - 8 GHz

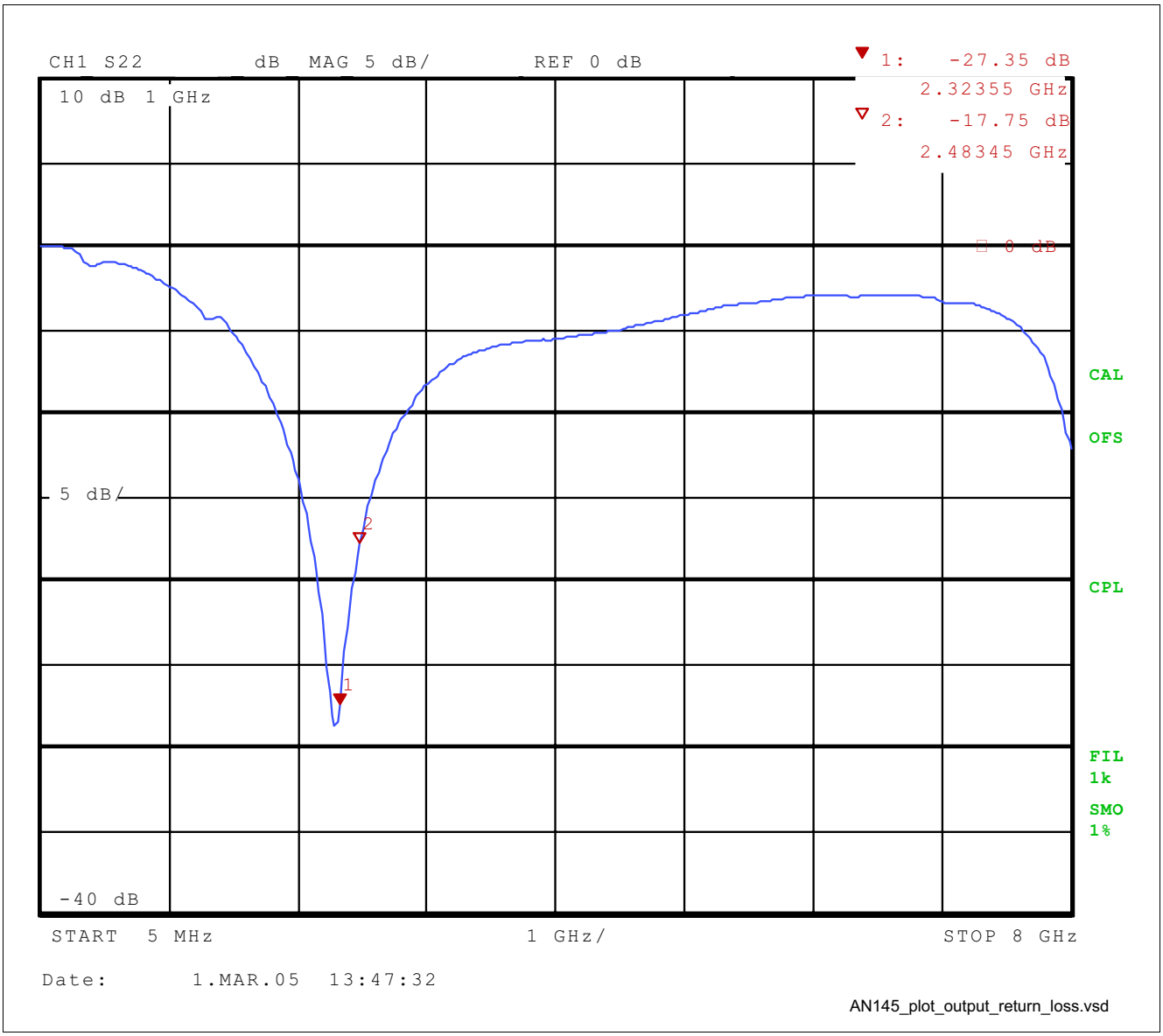


Figure 12 Plot of Output Return Loss

Output Return Loss, Smith Chart

Reference Plane = Output SMA Connector on PC Board
5 MHz - 8 GHz

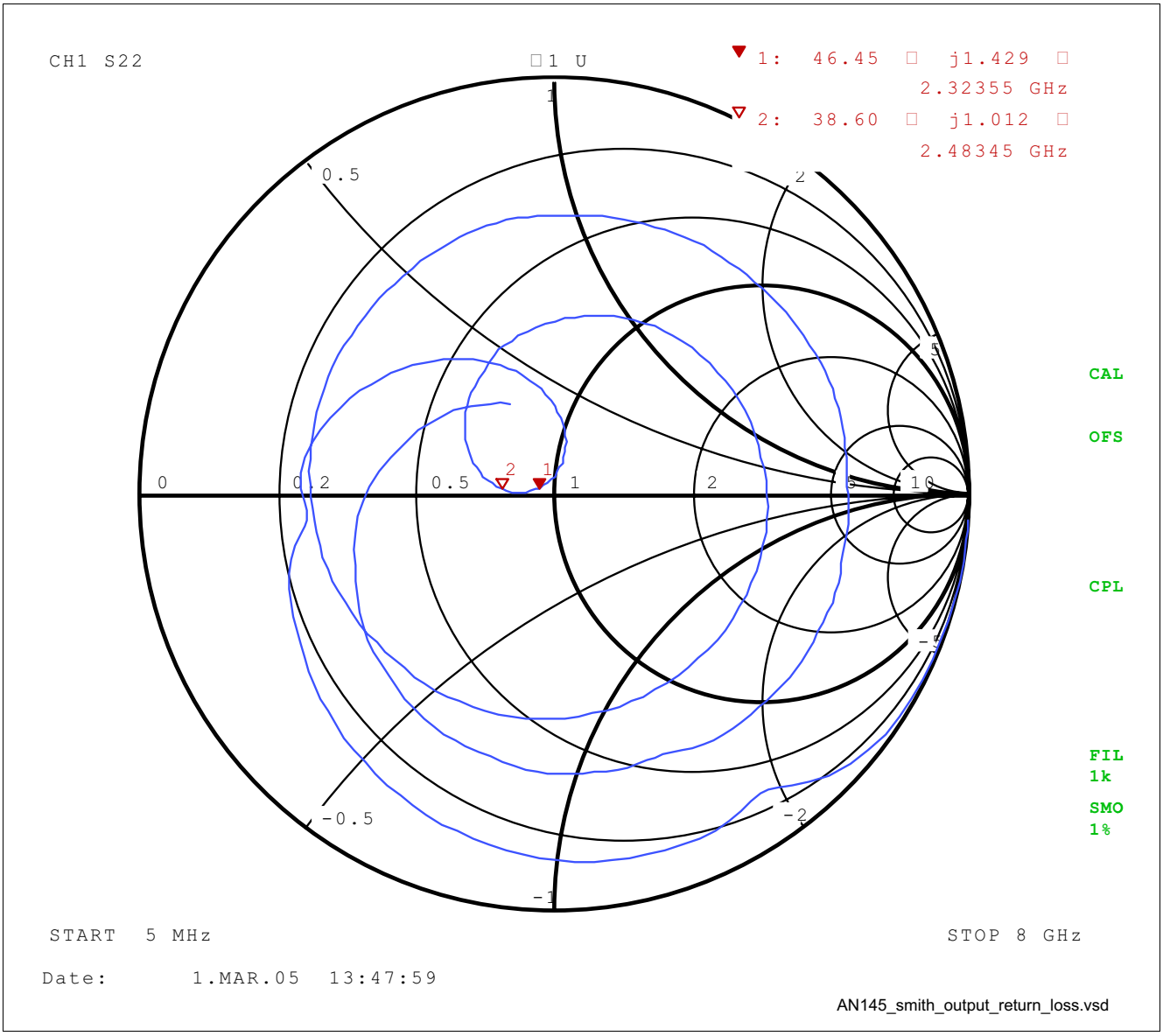


Figure 13 Smith Chart of Output Return Loss

Two Tone Test

Input Stimulus for Amplifier Two-Tone Test:
f_1 = 2332 MHz, f_2 = 2333 MHz, -10 dBm each tone.

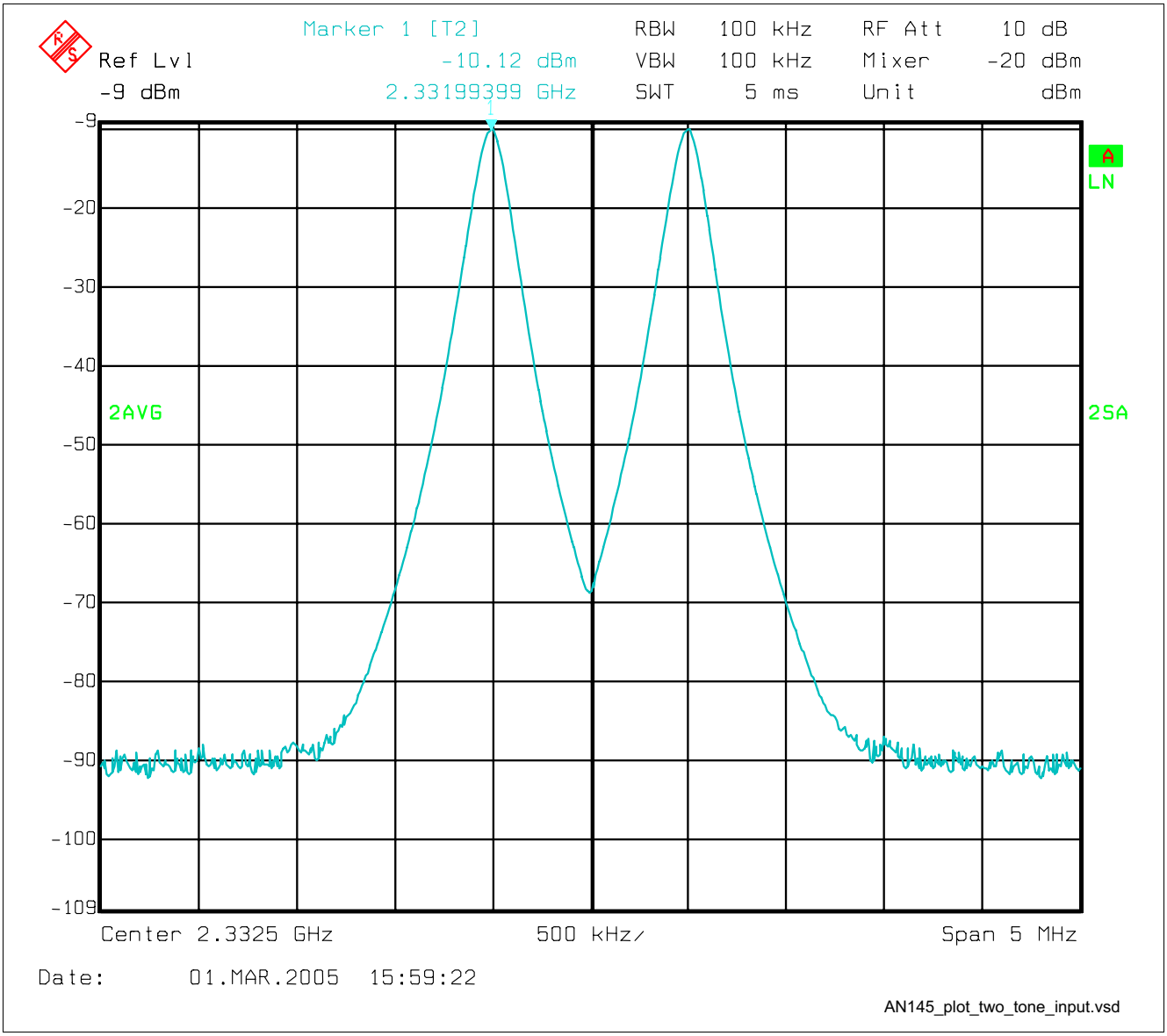


Figure 14 Tow-Tone Test, Input Stimulus

LNA Response to Two Tone Test

3.0 V, 76 mA for LNA.

Input IP_3 = -10 + (65.5 / 2) = +22.8 dBm
Output IP_3 = +22.8 dBm + 9.8 dB gain = +32.6 dBm

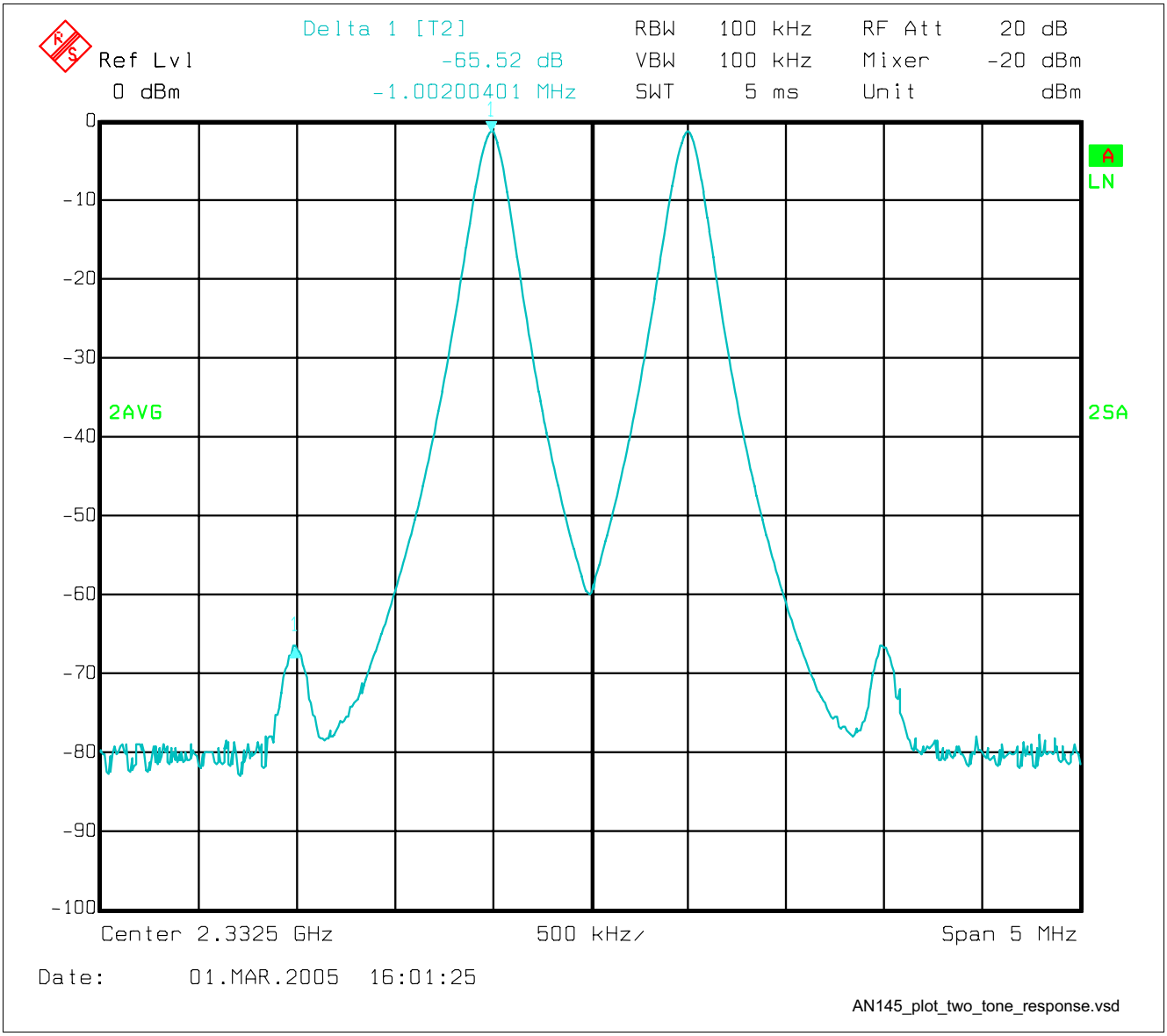


Figure 15 Tow-Tone Test, LNA Response