Application Note No. 140

ESD Protection for Digital High-Speed Interfaces (HDMI, FireWire, ...) using ESD5V3U1U

RF & Protection Devices

Never stop thinking

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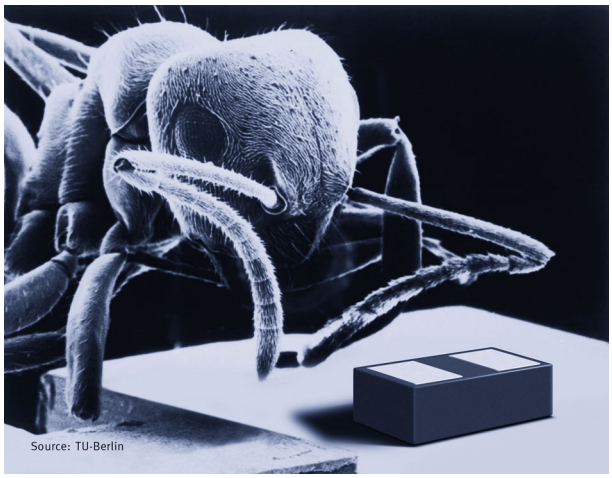
1 Introduction

As feature sizes continue to shrink and the trend toward higher data rates progresses, highly integrated chips are becoming increasingly sensitive, placing tougher demands on ESD components. The only way to ensure stable operation and maximum reliability in today's communications electronics is to ensure equipment is properly protected against electrostatic discharge and transients. This means TVS diodes are a key quality feature. Infineon seizes the opportunity to meet the challenge of the market and offers the world's first TVS diodes in the EIA case size 0201 (0.62 mm x 0.32 mm x 0.31 mm) and a capacitance of only 0.45 pF. The low capacitance of the diode together with the low parasitic inductance of the thin super small leadless package (TSSLP-2-1) features a 3 dB bandwidth of 11 GHz in a 50 W system, adequate for digital high-speed interfaces with baud rates as high as 4 GBd without any need to compensate for the diode's capacitance.



Infineon's Thin Super Small Leadless Package TSSLP-2-1

This greatly simplifies layout and design for today's digital high-speed interfaces like FireWire S1600β, DisplayPort, SATA II and HDMI 1.3a with baud rates of 1.966 GBd, 2.7 GBd, 3 GBd and 3.4 GBd respectively (a HDMI TMDS link makes uses of 3 channels, one for each color, providing a total data signaling rate of 10.2 Gbit/s). The low capacitance can be compensated by just a trace as short as 2 mm for baud rates of more than 6 GBd. Despite the low capacitance the diode can discharge ESD events of at least ±20 kV as per IEC 61000-4-2 specification during either air or contact discharge and is therefore qualified for all applications requiring compliance with level 4 of IEC 61000-4-2.

Although the 0201 package size is already standardized for years, market demand for such small packages is only slightly growing. Thus, Infineon's TVS diodes are also available in the bigger TSLP-2-7 (1.0 mm x 0.6 mm x 0.39 mm). Because of the higher parasitic inductance of the bigger package, the TVS diode in the EIA case size 0402 has a slightly lower bandwidth of 9.3 GHz, which is still adequate for all today's digital high-speed interfaces including HDMI 1.3a. The package size is coded in the suffix of the part number, for example, ESD5V3U1U-02LS identifies the 0201 package size (TSSLP-2-1) while ESD5V3U1U-02LRH identifies the 0402 package size (TSLP-2-7).

ESD5V3U1U-02LS / -02LRH

The unidirectional TVS diode ESD5V3U1U, featuring a typical capacitance of 0.45 pF and a typical breakdown voltage of 8.3 V, was designed for digital high-speed applications operating at voltages of up to 5.3 V at leakage currents of less than 10 nA.

ESD3V3U1U-02LS / -02LRH

The unidirectional TVS diode ESD3V3U1U was especially designed for mobile phone applications with a maximum operating voltage of 3.3 V only. In order to ensure long battery life, leakage current is further reduced to less than 1 nA.

ESD8V0R1B-02LS / -02LRH

The bidirectional TVS diode ESD8V0R1B is designed for use in a wide voltage range from -8 V to +14 V. With a typical capacitance of 4 pF, it ensures signal integrity on digital high-speed interfaces with baud rates of up to approximately 500 MBd. The key feature of this TVS diode is its low leakage current of less than 1 nA, an important factor in battery-powered devices.

2 Overview

The focus in this application note is on Infineon's new TVS diode ESD5V3U1U for digital high-speed interfaces at baud rates of more than 6 GBd. All measurements presented herein are based on S-parameter measurements from 10 MHz to 20 GHz using wafer probes in order to measure directly on the package level without the need of de-embedding S-parameters from measurements on a printed circuit board. First of all, **Chapter 3** gives a brief overview on different ESD protection concepts for digital interfaces. Since in common speech the term "bit rate" often leads to confusion, **Chapter 4** will clarify the difference between bit rate, data signaling rate and baud rate. In order to avoid any misinterpretation, the term "bit rate" is avoided and only baud rate is used within this application note. In **Chapter 5** we will discuss the capacitance vs. frequency and DC voltage as well as the parallel resistance. In digital high-speed interfaces with baud rates above 100 MBd the capacitance results in reflections, leading to signal distortions. Thus, in **Chapter 6** the peak reflected signal magnitude vs. rise time is discussed, while **Chapter 7** briefly discusses the influence on the rise time. Next, **Chapter 8** presents example layouts as well as design rules on how the capacitance can be compensated. **Chapter 9** finally compares Infineon's TVS diode ESD5V3U1U with other technologies like polymer-based suppressor and multilayer varistor. A simple example shows the importance of a low differential series resistance and low breakdown voltage for the transient voltage suppressor. For the mathematical enthusiast, **"Appendix" on Page 19** gives the derivation of the equations used to calculate the peak reflected signal magnitude.

Figure 1 shows the characteristic curve of an unidirectional diode and gives a definition of terms and symbols related to diodes. **Table 1** lists electrical characteristics that are especially useful for the digital engineer of digital high-speed interfaces.

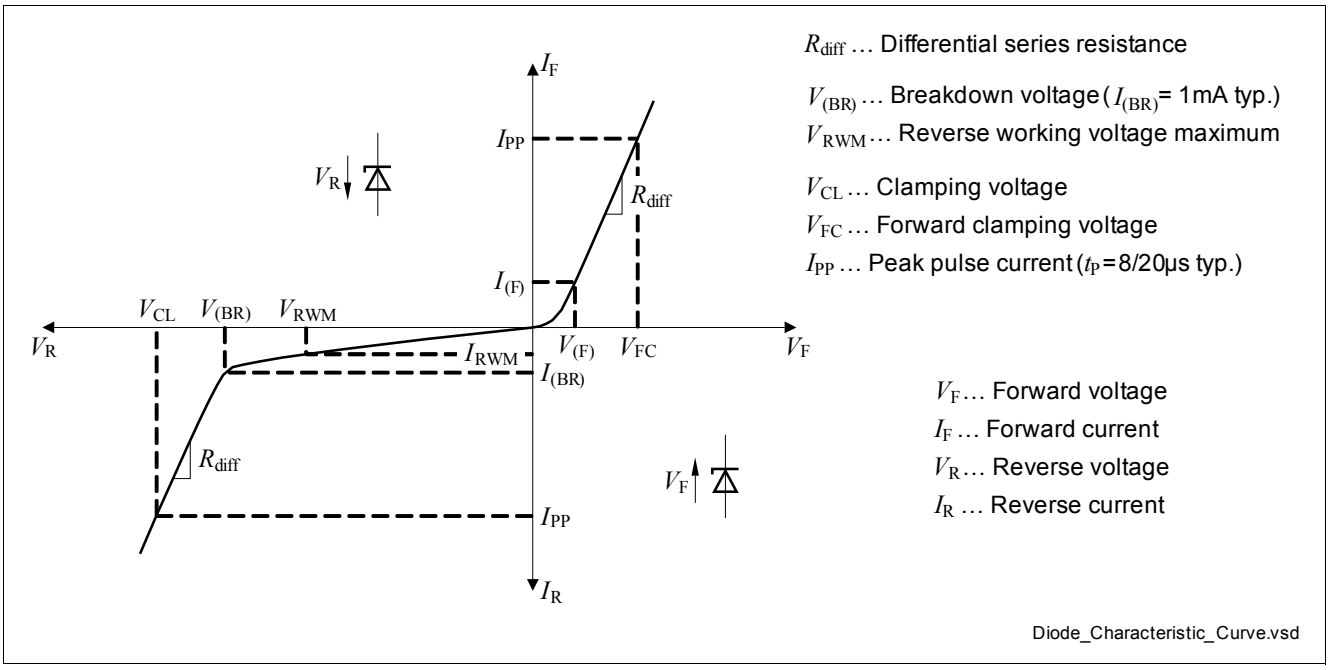


Figure 1 Characteristic curve of unidirectional diode

Table 1 Electrical characteristics of ESD5V3U1U-02LS

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse voltage	V_R	-0.3		5.3	V	
Capacitance	C		0.36		pF	V_R = 3 V, f = 2 GHz
Parallel resistance	R_p		1400		Ω	V_R = 3 V, f = 2 GHz
3dB bandwidth	f_{3dB}		11		GHz	Z_S = Z_L = 50 Ω, TSSLP-2-1
Time constant	τ		9		ps	V_R = 3 V, f = 2 GHz, Z_S = Z_L = 50 Ω
ESD test voltage	V_{ESD}	20			kV	as per IEC 61000-4-2
Series inductance	L		0.2		nH	TSSLP-2-1
Breakdown voltage	$V_{(BR)}$		8.3		V	
Differential series resistance	R_{diff}		1		Ω	t_p = 8/20 µs as per IEC61000-4-5
ESD rise time	$t_{r,esd}$		0.2		ns	10% to 90% rise time in response to an 15kV ESD event as per IEC61000-4-2 contact discharge

3 TVS Diode Concepts

For ESD protection of digital interfaces there are, in general, three different configurations possible, as shown in **Figure 2**. The simplest one is a single TVS Zener diode, which operates during normal mode in reverse biased condition. Thus, it can handle only voltages between -0.3 V and the reverse working voltage maximum V_{RWM}, also referred to as stand-off voltage. Since ESD events with positive polarity are discharged by the TVS Zener diode in reverse biased condition, the active area of the diode must be sufficiently large to not be destroyed by the ESD event. On the other hand, the bigger the active area of the diode the higher the capacitance will be. Hence, there is a lower limit with respect to capacitance for single TVS Zener diodes, typically around 10pF.

In order to further decrease the capacitance, a combination of two fast switching PIN diodes and one single TVS Zener diode is commonly used. Since the capacitance of the PIN diodes is much lower than the capacitance of the TVS Zener diode, the total capacitance is mainly determined by the PIN diodes. Unlike TVS Zener diodes, PIN diodes can not absorb ESD events in reverse biased condition and are therefore always arranged in an anti-parallel configuration. This makes sure that neither PIN diode absorbs ESD events in reverse biased condition. With such a configuration, capacitances of less than 1pF can be realized. With the TVS diode ESD5V3U1U Infineon carries this technique to new extremes now.

The bidirectional configuration, where two TVS Zener diodes are arranged in series but reverse order, has the advantage that it can handle voltages between $-V_{RWM}$ and $+V_{RWM}$, which may not be necessarily symmetrically. Since both diodes are connected in series, the total capacitance compared to a single diode is lowered too, but it is limited to only half the capacitance of one diode in the case of two symmetrical diodes. So, the lower limit for the capacitance of this configuration is around 5 pF. Infineon's bidirectional TVS diode ESD8V0R1B with a capacitance of 4 pF is an example.

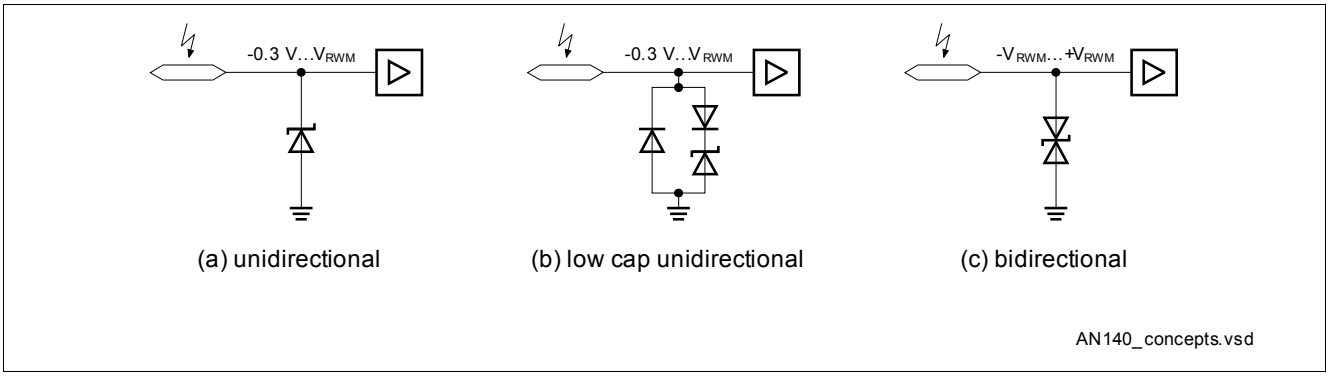


Figure 2 Three different concepts for TVS diodes: (a) single TVS Zener diode, (b) combination of two fast switching PIN diodes and one TVS Zener diode to reduce the capacitance and (c) two back-to-back TVS Zener diodes make a bidirectional TVS diode

4 Baud Rate, Bit Rate and Nyquist Frequency

Baud (unit symbol Bd) is the unit of modulation rate (also known as symbol rate), that is the number of data signaling events (symbols) per second in a digitally modulated signal. Bit rate (unit symbol bit/s) is different from the modulation rate, because one symbol may carry more than one bit of information. For example, in wireless networks, where spectral efficiency is important, it is common to carry two or more bits per symbol to achieve higher data transfer rates. However, in wired short-range digital communication systems it is common to carry only one bit per symbol, that is only binary digits. Only in the case of binary digits baud rate is a synonym for bit rate or more precisely binary digit rate **[4]**. In common speech bit rate is frequently confused with data signaling rate, which is the total number of physically transferred bits per second over a communication link. If a communication link is made up of two or more parallel channels, then the bit rate on one single channel is the data signaling rate divided by the number of channels, provided the bits per symbol is the same on all channels. For example, HDMI with a data signaling rate of 10.2 Gbit/s makes use of 3 parallel channels, one each for the colors red, blue and green. Hence, the bit rate on each channel is 3.4 Gbit/s and since HDMI carries only binary digits (one bit per symbol), the baud rate is thus 3.4 GBd. In order to avoid any confusion between bit rate and data signaling rate, only the term “baud rate” (expressed in Bd) is used within this application note.

Binary digits that are coded using the non-return-to-zero (NRZ) line code require a channel with a bandwidth of at least half the binary digit rate. This fundamental rule was first published 1928 by Harry Nyquist in the paper “Certain topics in Telegraph Transmission Theory”. A HDMI channel, for instance, should have a bandwidth of at least 1.7 GHz in order to make binary digit rates of 3.4 Gbit/s possible.

5 Capacitance and Resistance

The capacitance of a TVS diode is generally voltage- and frequency-dependent. In order to facilitate comparisons, it is common practice to state the capacitance of diodes at a reverse working voltage V_R = 0 V and a frequency f = 1 MHz. However, for digital high-speed interfaces like HDMI with baud rates of several GBd, the capacitance in the high-frequency range is of more interest than the capacitance at 1 MHz. Furthermore, HDMI is a DC coupled digital interface and the single-ended voltage level of the digital data signal has to lie between 2.6 V and 3.3 V. Consequently, the HDMI data signal can be seen as a bipolar, DC free, digital data signal with a voltage swing of approximately 0.5 V and a superimposed DC voltage of approximately 3 V. Typically, the capacitance reduces with frequency and reverse voltage. **Figure 3** and **Figure 4** show the apparent capacitance and resistance of the TVS diode ESD5V3U1U-02LS vs. frequency and different reverse voltages when the diode is seen as simple parallel RC circuit. The higher the frequency, the more weight the inductance of the bond wire (approximately 0.2 nH) carries, and so the apparent capacitance increases at frequencies above 6 GHz. As one can see in

Figure 3, the capacitance at 1.7 GHz and V_R = 3 V is just 0.36 pF, 20% lower than at 1 MHz and V_R = 0 V, and reaches its minimum of 0.34 pF around 5 GHz. The parallel resistance of the TVS diode is much higher than the capacitive reactance, so that the parallel resistance can be neglected for simple calculations.

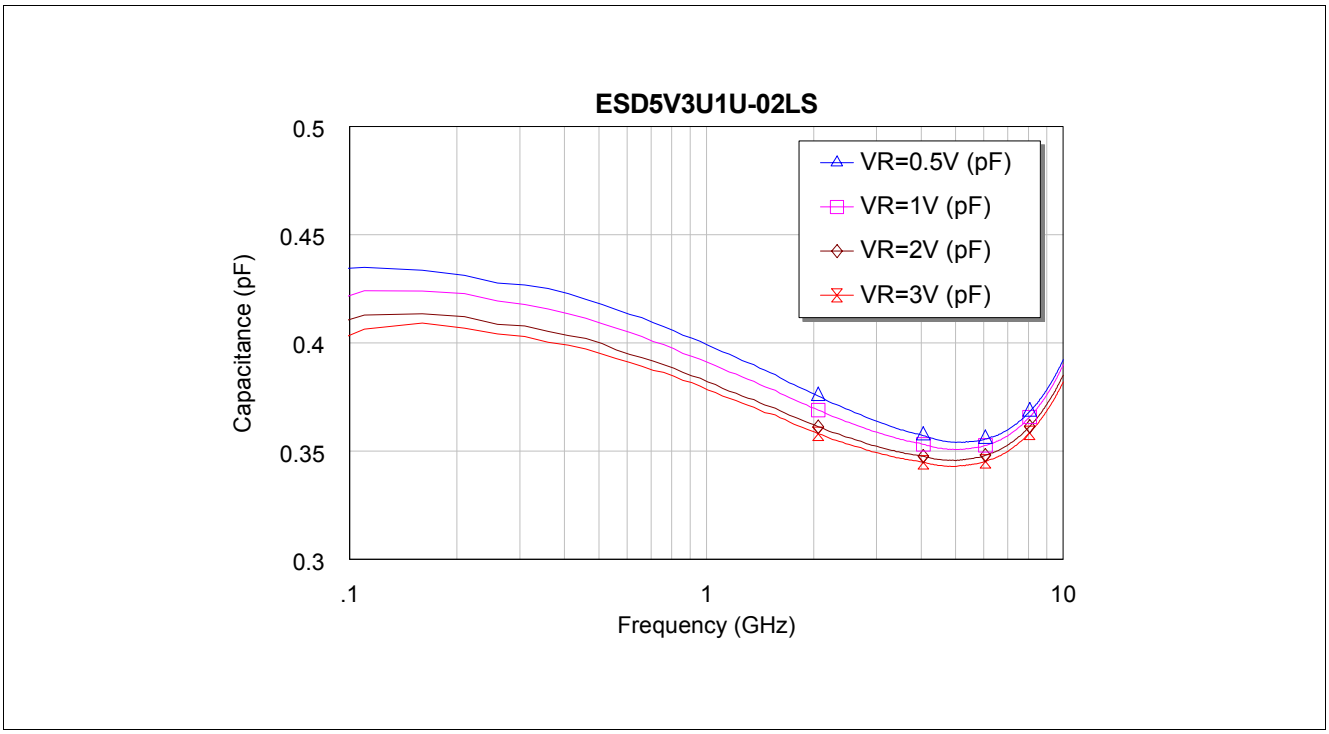


Figure 3 Apparent parallel capacitance of ESD5V3U1U-02LS (TSSLP-2-1 package)

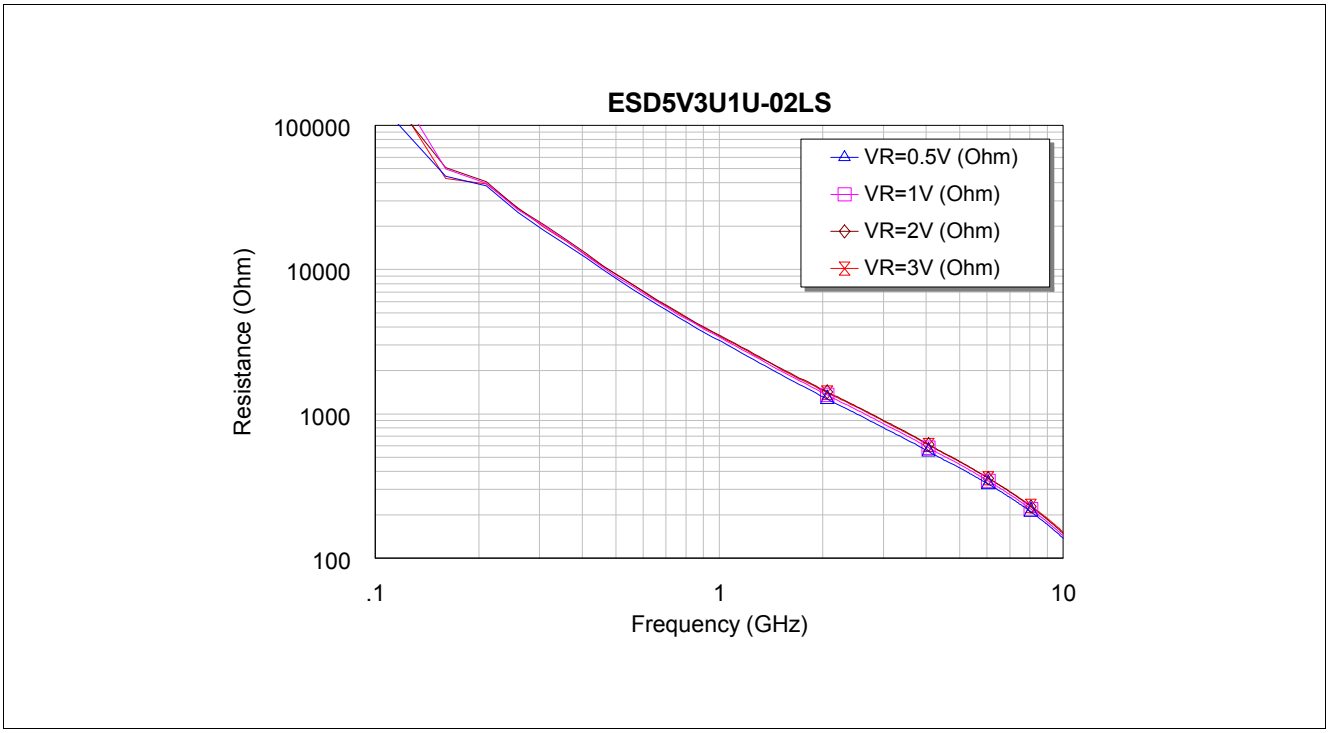


Figure 4 Apparent parallel resistance of ESD5V3U1U-02LS (TSSLP-2-1 package)

6 Reflections

When the bit time of the digital system is in the same order as the transit time of the signal from the transmitter to the receiver, the signal must be seen as composition of forward and backward traveling voltage waves according to the rules of RF engineering. Backward traveling waves lead to signal distortions and hence must be avoided. Traveling waves are reflected at impedances discontinuities and the magnitude ratio of the backward traveling wave V^- to the incoming forward traveling wave V^+ is given by the reflection coefficient Γ as follows:

$$\Gamma = \frac{V^-}{V^+} = \frac{Z_X - Z_0}{Z_X + Z_0}, \tag{1}$$

where Z_X is the impedance at a specific location x on the transmission line and Z_0 is the characteristic impedance of the transmission line the wave is traveling on. For this reason the capacitance of TVS diodes at baud rates of more than 1 GBd must be less than 1 pF in order to keep reflections low. The lower the capacitance, the less the traveling wave will be bothered by the TVS diode.

In digital engineering it is common to measure and specify the impedance Z_X on the transmission line by using time-domain reflectometry (TDR) rather than in the frequency domain by using network analysis. Since the reflection coefficient is frequency dependent, the impedance measured by TDR is a function of the rise time of the step edge that is used for the measurement. Thus, many standards for digital systems specify the rise time that has to be used for the TDR measurement. Now, in the case of a capacitive TVS diode with the time constant τ and a given 10% to 90% rise time t_r of the step edge, the peak reflected signal magnitude Γ_{pk} is approximately as follows:

$$\Gamma_{pk} \approx \frac{\tau}{t_r}\bigg|_{t_r > 8\tau}. \tag{2}$$

Figure 5 shows the peak reflected signal magnitude vs. rise time of Infineon's TVS diode ESD5V3U1U in both packages. The influence on the peak reflected signal magnitude of the slightly higher inductance of the 0402 case size TSLP-2-7 compared to the 0201 case size TSSLP-2-1 is negligible.

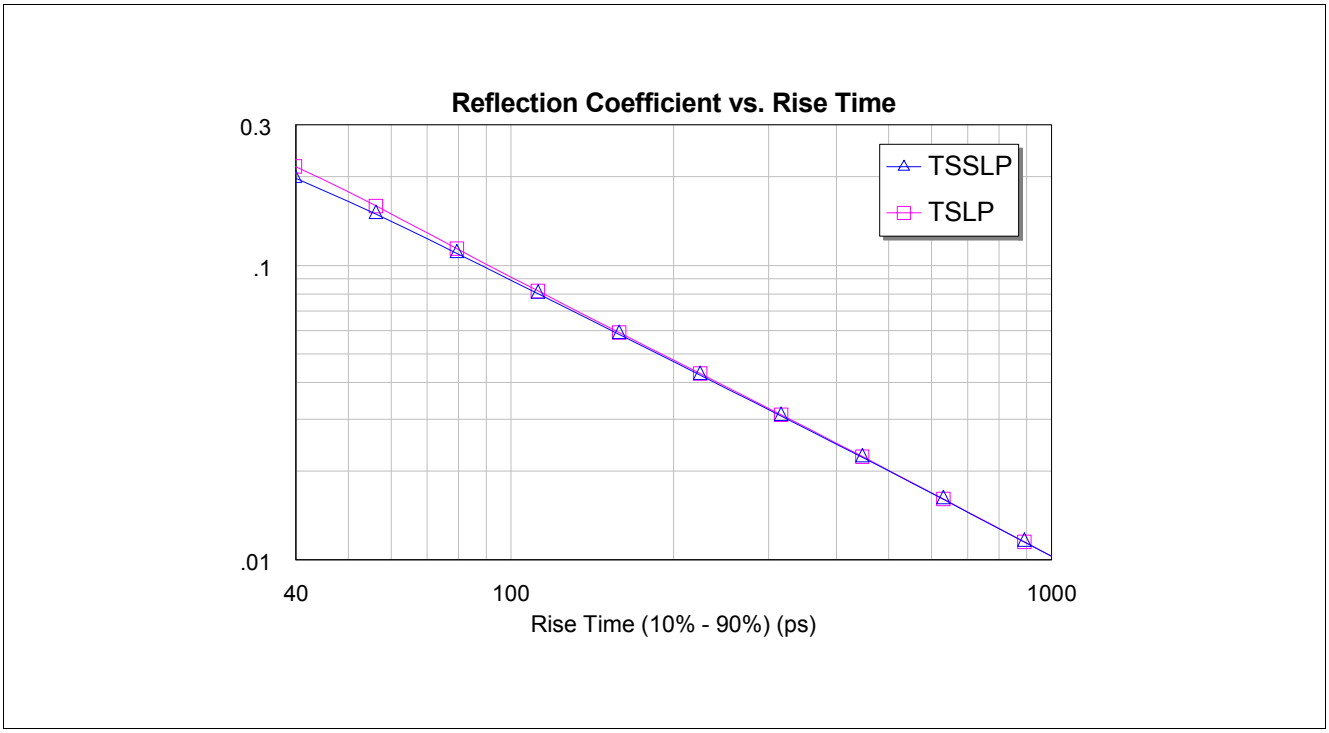


Figure 5 Peak reflected signal magnitude as a fraction of incoming step size vs. 10% – 90% rise time of incoming gaussian pulse (Z_0 = 50 Ohm, Z_{diff} = 100 Ohm)

Example

If a 100 Ω differential transmission line pair is protected by two TVS diodes ESD5V3U1U, what change in impedance can be expected for a step edge with a 20% to 80% rise time of 100 ps?

First of all, the 20% to 80% rise time has to be converted to a 10% to 90% rise time. For a step with a gaussian edge, following relation can be used to convert between both:

$$t_r = 1.52 \cdot t_{r,\,20\%-80\%}. \tag{3}$$

Thus, we obtain a 10% to 90% rise time of 152 ps. The time constant τ for ESD5V3U1U is given by following equation (see also **Figure 6**):

$$\tau = \frac{Z_0}{2} C. \tag{4}$$

With $Z_0 = Z_{diff}/2 = 50\ \Omega$ and $C = 0.36$ pF we obtain a time constant $\tau = 9$ ps (the time constant is the same for a 50 Ω transmission line and a 100 Ω differential transmission line pair, because the resistance doubles and the capacitance halves). Now, from **Figure 5** (or by applying **Equation (2)**), a peak reflected signal magnitude of 0.06 is obtained. By rewriting **Equation (1)** and keeping in mind that capacitance results in negative reflection coefficient and thus reduced impedance, we can calculate the impedance at the TVS diode as follows:

$$Z_{tvs} = Z_0 \frac{1 - |\Gamma_{pk}|}{1 + |\Gamma_{pk}|}. \tag{5}$$

Thus, we obtain a differential impedance of 89 Ω, which is 11% less the nominal impedance of 100 Ω. For example, the HDMI 1.3a standard permits through connection impedance variations of ±15% for a 10% to 90% rise time of 200 ps. Hence, there is no need for compensation of the capacitance of the TVS diode.

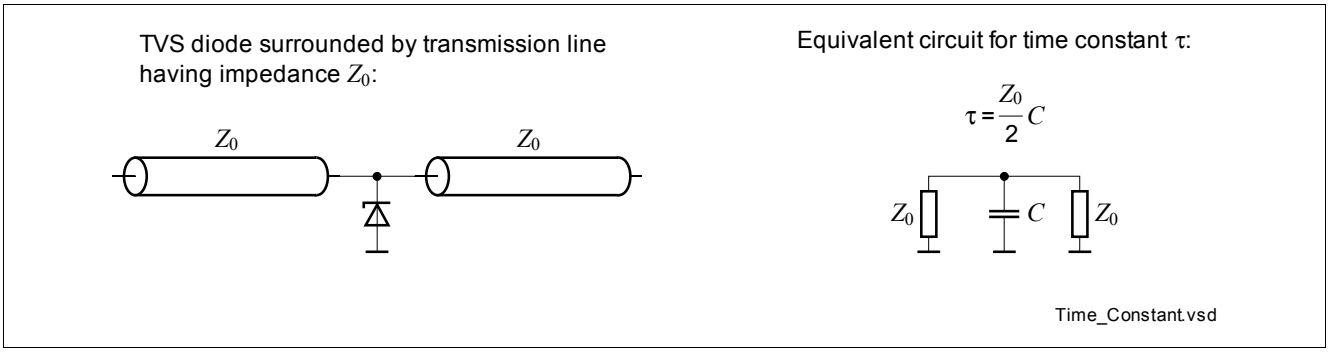


Figure 6 Time constant of TVS diode having capacitance C, surrounded by transmission line

Note: Please note that the time constant of the diode is the same for both single-ended 50 Ω transmission lines and differential 100 Ω transmission lines, because two diodes are needed for the differential transmission line.

7 Rise Time and Bandwidth

If the incoming step has the 10% to 90% rise time t_r, then the rise time of the forward-propagating signal t_{fwd} is estimated as

$$t_{fwd} \approx \sqrt{t_r^2 + (2.2\tau)^2}\,. \tag{6}$$

From **Equation (2)** one can see that the peak reflected signal magnitude is inversely proportional to the rise time of the incoming step: The faster the rise time the higher the peak reflected signal magnitude. This is because faster rise times are composed of higher frequency components and the 3 dB bandwidth of the gaussian step is given as

$$f_{3dB} = \frac{0.34}{t_r}\,, \tag{7}$$

where t_r is the 10% to 90% rise time.

Since rise times much shorter than the bit time T_b of the digital system just show you more fine-structure detail by increasing the resolution, but are not going to matter in the system, many standards specify a lower limit for the rise time, for example the HDMI 1.3a standard specifies a lower limit of 75ps for the 20% to 80% rise time, which is equivalent to a 10% to 90% rise time of 114ps by applying **Equation (3)**. On the other hand, there exists an upper limit for the rise time and for NRZ signaling with the binary digit rate $r_b = 1/T_b$, the bandwidth must be greater than the Nyquist frequency:

$$f_n = \frac{r_b}{2} = \frac{1}{2T_b} < f_{3dB}\,. \tag{8}$$

Dependent on the maximum length and thus the maximum transmission losses of the interconnection, different standards have different requirements on the transceivers, so that there does not exist an absolute upper limit for the baud rate a TVS diode with a given capacitance can be used for.

Example

If a 100Ω differential transmitter, for example a HDMI compliant source, has a 20% to 80% rise time of 75ps (this is the minimum rise time for HDMI compliant sources **[5]**), what is the 20% to 80% rise time of the forward propagating wave after the wave has passed the TVS diode ESD5V3U1U?

First, the 20% to 80% rise time has to be converted into the 10% to 90% rise time according to **Equation (3)**, which gives 114 ps. On 100 Ω differential transmission line pairs, the TVS diode ESD5V3U1U has a time constant τ = 9 ps. Then, from **Equation (6)** the 10% to 90% rise time of the forward propagating wave gives t_{fwd} = 116 ps, and converted back to the 20% to 80% rise time gives 76ps. Hence, the rise time is only an insignificant 1ps increased by the TVS diode.

8 PCB Design

For TVS diodes a low-ohmic and low-inductive path to chassis earth is absolutely mandatory in order to achieve good ESD protection. Novices in the area of ESD protection should take following suggestions to heart:

- Do not use stubs, but place the cathode of the TVS diode directly on the signal trace.
- Do not make false economies and save copper for the ground connection.
- Place via holes to ground as close as possible to the anode of the TVS diode.
- Use as many via holes as possible for the ground connection.
- Keep the length of via holes in mind! The longer the more inductance they will have.

Decoupling between TVS diode and ESD sensitive transceiver greatly enhances ESD robustness. Of course there are limits, because the transmission of digital high-speed signals should not be affected by this. **Figure 7** shows an equivalent circuit including parasitic elements as seen by an ESD event. If the transmission line is terminated with its characteristic impedance Z_0, then there will be no reflection at the end and thus only the forward propagating wave is traveling on the transmission line. Hence, during normal operation the transmission line behaves like a resistance of value Z_0 (for high-speed digital interfaces the single-ended impedance Z_0 is usually 50 Ω). But as soon as the on-chip ESD protection structure triggers during an ESD event, the transmission line is no longer terminated with its characteristic impedance, but with a low-ohmic resistance. Thus, it no longer behaves like a resistance of value Z_0, but as an inductance of value L_{TL}, approximately given by

$$L_{TL} \approx \frac{l}{v} Z_0 = \frac{l}{c_0} \sqrt{\varepsilon_r} Z_0 \Big|_{l < \lambda/10}, \quad (9)$$

where l is the length of the transmission line, v is the trace velocity, c_0 = 300 mm/ns is the speed of light, ε_r is the effective dielectric constant and Z_0 is the characteristic impedance of the transmission line. **Equation (9)** is only valid for wave lengths λ greater than ten times the length of the transmission line. Nevertheless, this should be sufficient to estimate the inductance for the high energy part of the ESD event, which is located in the frequency range below 200 MHz. One important observation can be made from **Equation (9)**: The inductance is directly proportional to the length of the transmission line. Thus, keep the transmission line as long as practical, place the TVS diode as close as possible to the connector and keep the ESD sensitive transceiver away from the connector.

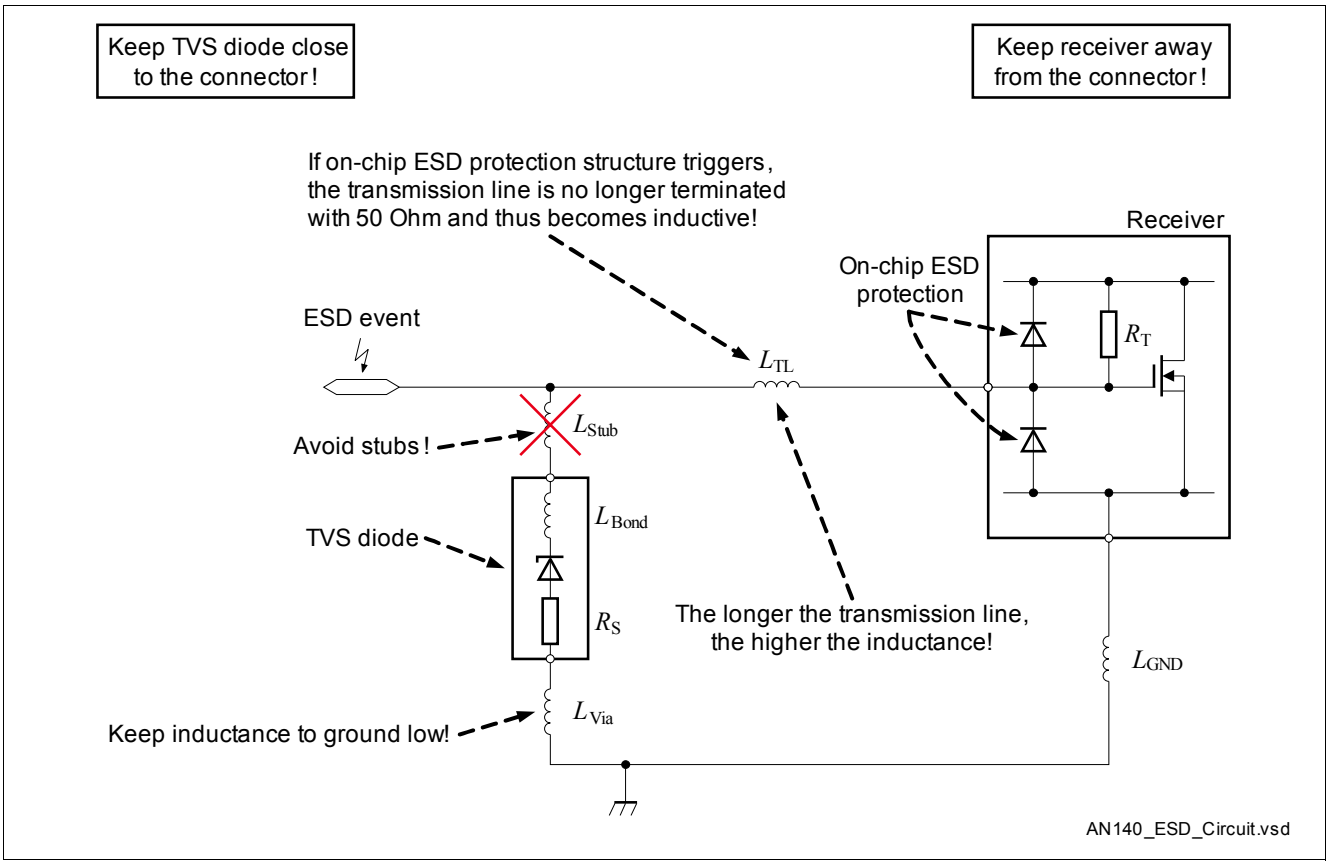


Figure 7 Equivalent circuit including parasitic elements as seen by an ESD event

8.1 Simple Layout

While the termination impedance must be closely matched to the characteristic impedance of the transmission line in order to avoid reflections and to absorb all the backward travelling waves, the specification for the through connection impedance is more relaxed. Typically, a variation of ±10% is allowed for the termination impedance and for the through connection impedance often excursions from the specified values are permitted as long as the duration is less than a specific time, typically twice the rise time, but at least less than the bit time. The excursions are needed for the imperfections of connectors, and so it is good practice to apply the specification for the termination impedance to the TVS diode as well.

By applying **Equation (1)**, a variation in the impedance of 10% results in a reflection coefficient Γ = -0.053 (take into account that a capacitance reduces the impedance). With a time constant of 9ps and applying **Equation (2)**, a rise time of 170 ps is obtained, which we consider to be the maximum rise time of the system. Then, from **Equation (7)** a minimum 3 dB bandwidth of 2 GHz is obtained for the system and according to Nyquist the system can therefore transmit data with a baud rate of 4 GBd.

Example

HDMI 1.3a specifies a maximum rise time of 200 ps for TDR measurements, so that it is not necessary to compensate the capacitance of the TVS diode by layout techniques. **Figure 8** shows an example layout for one single HDMI TMDS channel, where the 100 Ω differential transmission line impedance has not been changed for the TVS diode. Since the trace separation s of the differential transmission line pair is greater than 4 times the trace height h (substrate thickness), the differential transmission line is only loosely-coupled (s = 0.76 mm > $4h$ = 0.6 mm) and thus the ground extension from the connector to the TVS diodes is not going to change the differential impedance much. The simulation result for a gaussian edge with 10% to 90% rise time t_r = 180 ps < 200 ps is shown in **Figure 9**. As expected, the impedance remains within ±10% of the nominal impedance of 100 Ω. Please note that the port numbers of the S-parameters refer to the reference planes shown in **Figure 8**. Since the HDMI specification allows variations in the impedance measured by TDR of up to 15% and 25% for a duration of less than 250 ps, HDMI 1.3a compliance is met **[5]**.

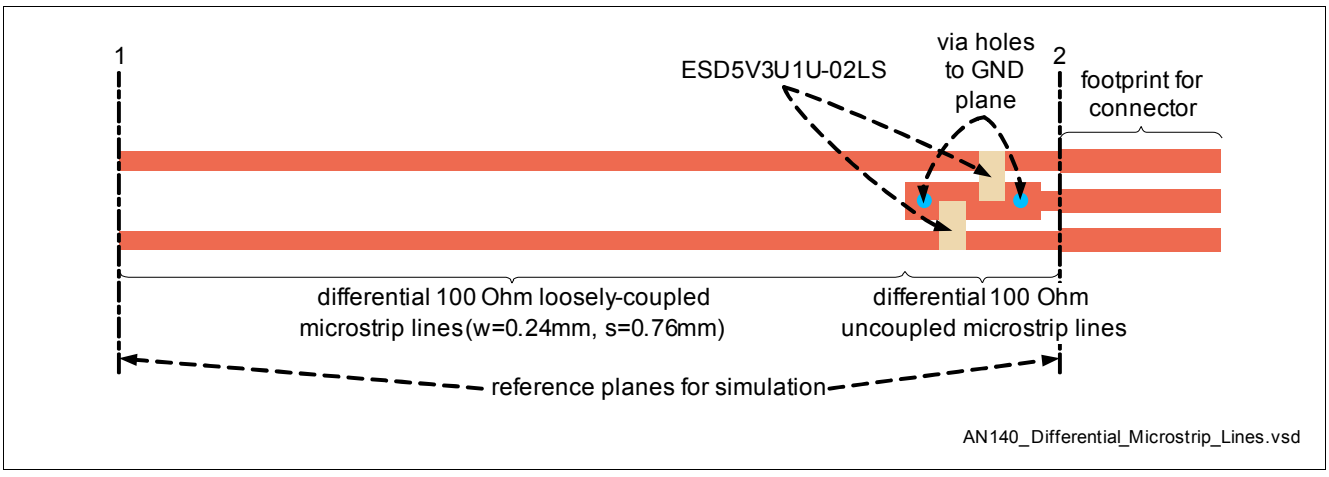


Figure 8 Example layout for a differential pair of loosely-coupled microstrip lines for a single HDMI TMDS channel (pitch of connector pins is 0.5 mm, substrate thickness h = 0.15 mm (6mil))

Attention: For good ESD protection, keep the parasitic inductance of traces and via holes in mind!

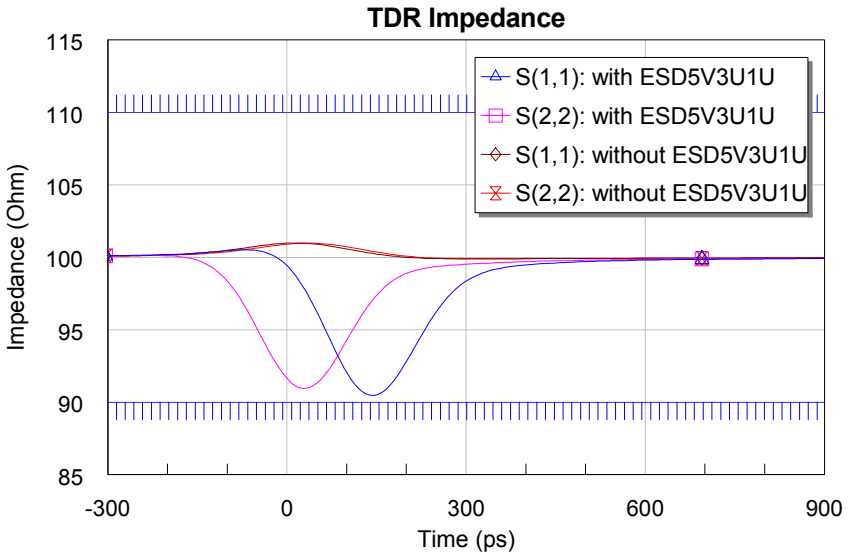


Figure 9 Time domain reflectometry (TDR) impedance with and without ESD5V3U1U as response to an incoming gaussian pulse with a rise time of 180 ps (10% – 90%)

8.2 Advanced Layout

When tighter tolerances must be met, the capacitance of the diode has to be compensated. Compensation is achieved by the skinny-trace compensation technique for example **[1]**. What makes this technique adequate is that the higher the frequency and the lower the capacitance of the TVS diode, the smaller distributed structures (traces) will be, so that only a short trace of 2 to 3 millimeters is needed.

The skinny trace without TVS diode has a higher impedance than the adjacent transmission line, which results in a higher inductance and thus effectively compensates the capacitance of the TVS diode (see **Figure 10**). The length l for the skinny trace is calculated such that the effective impedance of trace plus TVS diode is again Z_0:

$$l = vZ_0C_\mathrm{d}\frac{k}{k^2-1}, \tag{10}$$

where $k = Z_1/Z_0$ defines the characteristic impedance of the skinny transmission line, Z_0 is the characteristic impedance of the adjacent transmission line, C_d is the capacitance of the TVS diode and v is the trace velocity. From this equation one may notice that the skinnier the trace (the higher the impedance Z_1), the shorter the necessary length l will be. Of course, this technique does not work for arbitrary fast edges, there is a lower limit determined by the time delay t_L of the skinny trace plus TVS diode,

$$t_\mathrm{L} = Z_0C_\mathrm{d}\frac{k^2}{k^2-1}, \tag{11}$$

which must be at least 2 to 3 times lower than the 10% to 90% rise time of the edge:

$$t_\mathrm{r} > 2\ldots3t_\mathrm{L}. \tag{12}$$

Otherwise the step will not see the skinny trace plus TVS diode as one single structure, but as individual structures only and thus there will be no effect of compensation anymore.

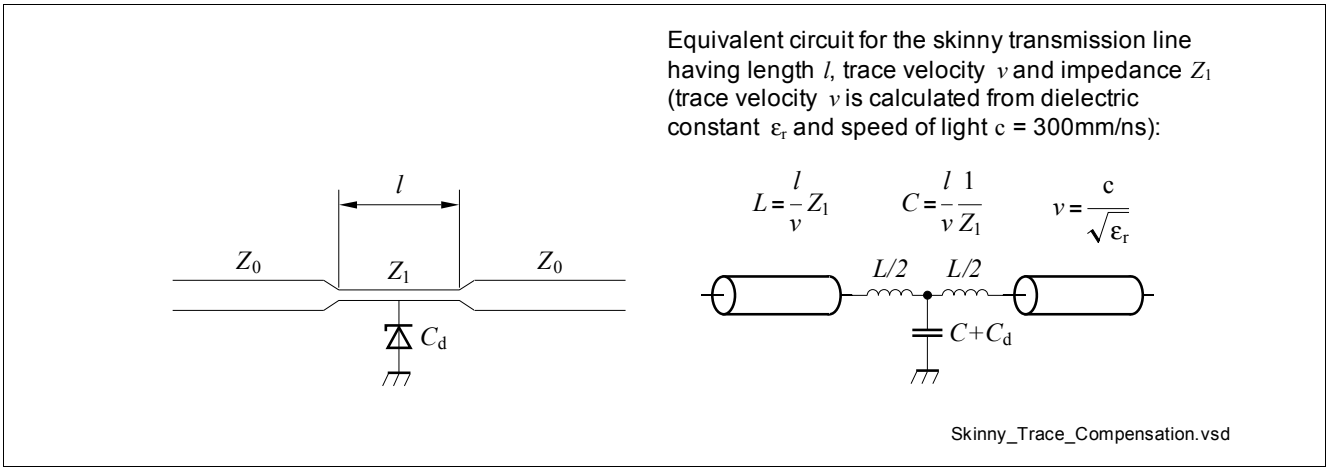


Figure 10 Compensate of the capacitance of the TVS diode

Example

Figure 11 shows an example layout where the capacitance of the TVS diode is compensated by a skinny-trace. For the skinny trace an impedance of 160 Ω was chosen (and thus k = 1.6), which results here in a trace width of w = 0.12 mm at a trace height h = 0.2 mm (substrate thickness), still wide enough for practical reasons. With $Z_0 C_d$ = 18 ps and an effective dielectric constant $\varepsilon_{r,eff}$ = 2.8 (and thus a trace velocity $v \approx$ 179 mm/ns), **Equation (10)** gives an estimation for the length of $l \approx$ 3.3 mm. For the example layout a length of l = 3.2 mm was chosen, but the difference is only marginal and irrelevant for any practical purpose. **Equation (12)** gives a lower limit of approximately 60…90 ps for the 10% to 90% rise time of the edge, and for the simulation a rise time of 90 ps was chosen. The TDR impedance shown in **Figure 12** has only a variation of ±5%. Hence, HDMI 1.3a compliance is easily met **[5]**. There is also the impedance without the TVS diodes in place shown and one can clearly see the highly inductive peaks caused by the skinny trace.

For a rise time of 60 ps (approximately twice the time delay t_L), the impedance variation is already about 10%, but still acceptable. Hence, this example layout is adequate for edges with rise times above 60 ps and it works reliably at baud rates of 5.6 GBd (assuming a maximum rise time of 120 ps, which is twice the minimum rise time). At a ratio of k = 2 this compensation technique can be used to protect digital interfaces at baud rates as high as 6.8 GBd from ESD events by using ESD5V3U1U (assuming a minimum rise time of 50 ps and a maximum rise time of 100 ps).

The FireWire S1600β (IEEE 1394b-2002) standard **[6]** allows variations in the impedance measured by TDR with rise times of 50 ps of ±18% and permits an excursion from this for a duration of less than 100 ps within a 700 ps exception window. Hence, FireWire S1600β compliance is met by compensating the capacitance of the TVS diode with just a 2 mm long skinny trace (k = 2).

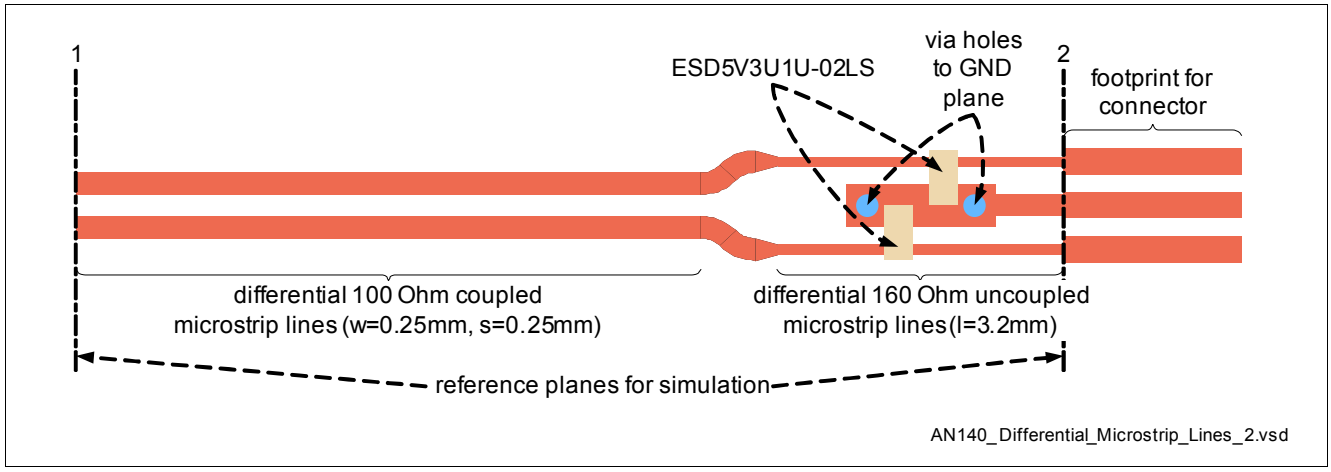


Figure 11 Example layout for a differential pair of coupled microstrip lines for a single HDMI TMDS channel (pitch of connector pins is 0.5 mm, substrate thickness h = 0.2 mm (8 mil))

Attention: For good ESD protection, keep the parasitic inductance of traces and via holes in mind!

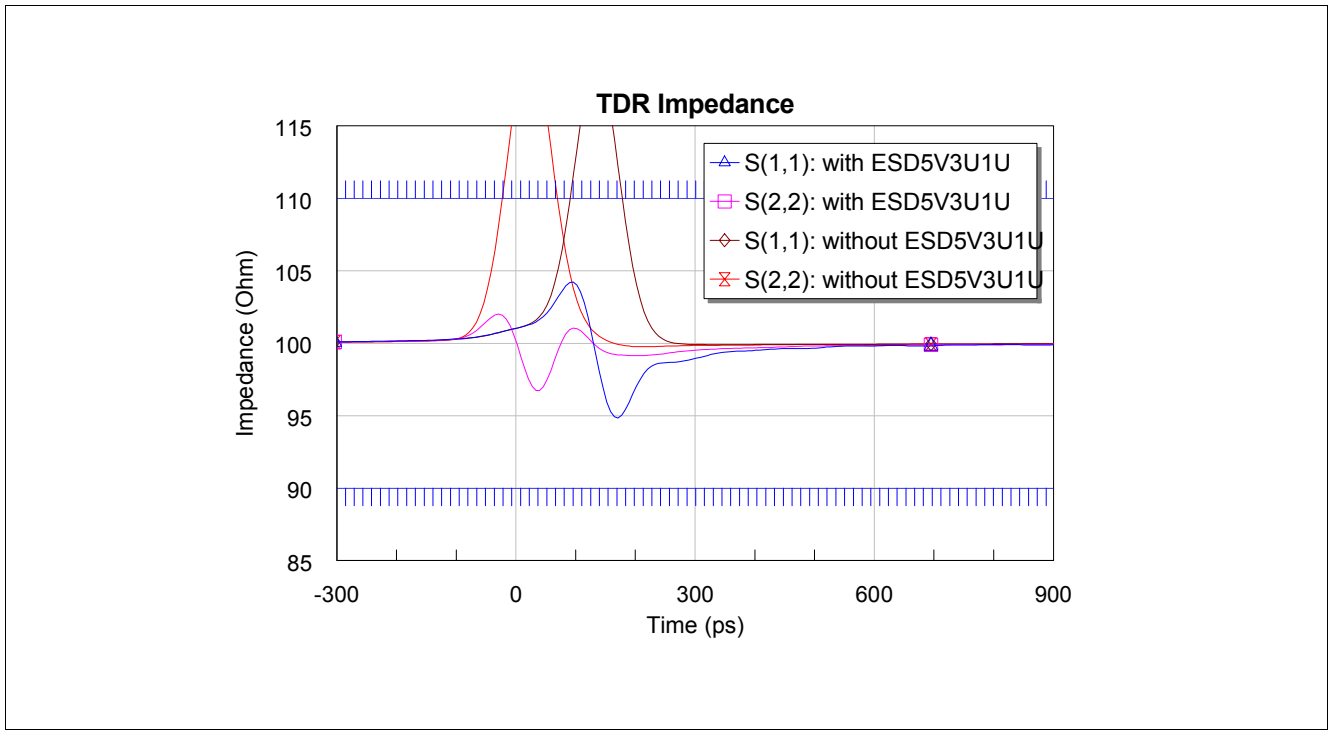


Figure 12 Time domain reflectometry (TDR) impedance with and without ESD5V3U1U as response to an incoming gaussian pulse with a rise time of 90 ps (10% – 90%)

9 Polymer-based Suppressor and Varistor

Even though ESD robustness is specified by stating voltage levels, for example 2 kV as per HBM (Human Body Model [2]), an ESD source is a current source rather than a voltage source, because of its high internal resistance, for instance 1500 Ω for HBM and 330 Ω as per IEC 61000-4-2 [3]. The ESD test voltage level is the voltage the ESD source (human being or capacitor in the case of an ESD tester) is charged to. Thus, during ESD the stressed device does not see the charging voltage, but approximately the discharge current through a short circuit. For the HBM device level test the peak current through a shorting wire is around 0.67 A per kilovolt charging voltage and for the system level test as per IEC 61000-4-2 the peak current is around 3.75 A per kilovolt charging voltage. Therefore, both standards lead to quite different results and it is important not to confuse the device level with the system level test. Typically, ESD robustness measured as defined by the HBM is approximately twice as high as per IEC 61000-4-2. On the basis of an example we will briefly discuss the applicability of TVS diodes, polymer-based suppressors and multilayer varistors for ESD protection of high-speed transceivers. A more detailed comparison between them can be found in [7].

9.1 Example

Transceivers for digital high-speed interfaces should be able to withstand ESD events of at least 2 kV as per HBM. Since it is difficult to achieve higher ESD ratings by utilizing on-chip ESD protection structures, many transceivers can not withstand more than 3 kV as per HBM, which is equivalent to a peak current of at most 3 x 0.67 A ≈ 2 A.

Now, we estimate the peak voltage during an ESD event as per the system level test IEC 61000-4-2. The time delay for a 40 mm transmission line is less than one third of the rise time of the ESD pulse, that is l/v = 0.24 ns < $t_r/3$ ≈ 0.29 ns, thus we can approximate the transmission line by an inductance and use **Equation (9)** to obtain the value L_{TL} for that inductance:

$$L_{TL} \approx \frac{l}{v} Z_0 = \frac{40\text{mm}}{170\text{mm/ns}} 50\Omega \approx 12\text{nH}\,. \tag{13}$$

For the on-chip ESD protection structure, for example a grounded gate NMOS (ggNMOS), we assume a high-current on resistance R_{on} = 3 Ω and a offset voltage V_{Hold} = 5 V, so that we can calculate the voltage at the connector in the case of an 2 kV ESD event directly discharged at the connector (see also **Figure 7**):

$$V_{pk} \approx L_{TL} \left.\frac{dI}{dt}\right|_{max} + R_{on} I_{pk} + V_{Hold}$$

$$V_{pk} \approx (12\text{nH} \cdot 4.3\text{A/(kV ns)} + 3\Omega \cdot 3.75\text{A/kV}) \cdot 2\text{kV} + 5\text{V} = 131\text{V}\,, \tag{14}$$

where the IEC 61000-4-2 specification [3] defines

$$I_{pk} = 3.75\text{A/kV} \quad \text{and} \quad \left.\frac{dI}{dt}\right|_{max} = 4.3\text{A/(kV ns)}\,. \tag{15}$$

The simulated peak voltage by using a 50 Ω microstrip line and the mathematical model of the discharge waveform as given in the IEC 61000-4-2 specification is 141 V. With an estimated peak voltage of 131 V, this simple calculation gives acceptable accuracy for transmission lines with time delays of up to one-third of the rise time of the ESD pulse.

9.2 TVS Diode ESD5V3U1U

With its low breakdown voltage of 8V, a differential series resistance of approximately 1Ω, low series inductance of 0.2nH (0.4nH for the bigger TSLP package) and fast response time—the 10% to 90% rise time in response to an ESD event is only 0.2ns—Infineon's TVS diode ESD5V3U1U clamps ESD events from less than 1kV up to 20kV and is therefore qualified for ESD protection of sensitive high-speed transceivers. For above example, approximately eight-ninth of the peak current of 7.5A is absorbed by the TVS diode, and thus only one-ninth or 0.8A are flowing into the transceiver.

9.3 Polymer-based Suppressor

Despite the very low capacitance of typically less than 0.2 pF, a polymer-based suppressor is inadequate to protect digital high-speed interfaces because of its very high trigger voltage of more than 150 V, often 300 V typical. This means, as long as the voltage at the connector stays below the trigger voltage, the polymer-based suppressor does not clamp at all. For above example, all the peak current of 7.5 A is flowing into the transceiver, which is too much for high-speed transceivers. Due to its relatively high resistance of several ohms after triggering, also the current absorbed by the polymer-based suppressor is much lower than for a TVS diode, which has a differential series resistance around 1 Ω.

9.4 Multilayer Varistor

Although multilayer varistors (MLVs) with capacitance values of less than 1 pF are possible, they suffer from high clamping voltages of several hundreds of volts. This is due to their inherent structural characteristics, which makes it impossible to reach low capacitance values and simultaneously maintain low clamping voltages. Typical varistor voltage—the voltage at a current of 1 mA—of MLVs with capacitances of less than 1 pF is between 80 V and 150 V and together with a differential series resistance of several tens of ohms, MLVs are even worse than polymer-based suppressors and therefore inadequate to protect sensitive high-speed transceivers from ESD events. For above example this means that almost all of the current flows into the transceiver and only a small part through the MLV. In fact, the high differential series resistance of the MLV, which is several times higher than that of the transceiver, means that the transceiver acts as ESD protection device rather than the MLV. The transceiver protects the MLV from being destroyed!

10 Conclusion

It has been shown that the capacitance of the diode does not influence either rise time or bandwidth of today's digital high-speed systems and for many digital interfaces there is no need to compensate the capacitance of Infineon's TVS diode ESD5V3U1U. However, compensation of the capacitance is achieved by skinny traces with a length of just 2 to 3 mm, if tighter tolerances for the impedance are required, for example for FireWire S1600β compliance. Furthermore, it was shown by a simple example, that neither polymer-based suppressors nor multilayer varistors are adequate for ESD protection of digital high-speed interfaces, because they are not capable to absorb currents from 2 kV ESD events as per IEC 61000-4-2, which is already enough to permanently damage ESD sensitive high-speed transceivers. Hence, Infineon's ESD5V3U1U is a first-class ESD protection device capable to protected ESD sensitive digital high-speed transceivers from ESD events as low as 200 V up to ESD events as high as 20 kV.

Appendix

Anyone who is interested in more detailed mathematics, the derivation of all the equations needed within this application note are provided as reference information on following pages.

The parallel resistance (see **Figure 4**) of TVS diodes at RF frequencies is still much higher than the impedance of the parasitic capacitance given by $1/(2\pi f C)$. Thus, the capacitance is the predominant factor contributing to impedance mismatch and reflections. In order to calculate rise time and reflection in response to an incoming step with the rise time t_r, one important parameter that characterizes the TVS diode is the time constant τ, given as follows:

$$\tau = (R \parallel Z_0 \parallel Z_0)C = \left(R \parallel \frac{Z_0}{2}\right)C = \frac{Z_0 R}{Z_0 + 2R}C \approx \frac{Z_0}{2}C, \tag{16}$$

where Z_0 is the characteristic impedance of the transmission line, for example 50 Ω, R is the parallel resistance and C is the parallel capacitance of the TVS diode. At a frequency of 2 GHz the parallel resistance R is less than 2% of half the characteristic impedance of 25 Ω and can therefore be neglected. Please note that when you use two TVS diodes per differential signal pair, one for each transmission line, and both anodes are directly connected on the PCB through a low ohmic path, the time constant does not change, because then all resistances are doubled and the capacitance is halved. Hence, it does not matter if you use one TVS diode for a 50 Ω single ended transmission line or two TVS diodes for a 100 Ω differential transmission line pair, the time constant remains always the same. Now then, the 10% to 90% step rise time t_d calculates as follows:

$$t_d = \tau(\ln 0.9 - \ln 0.1) \approx 2.2\tau. \tag{17}$$

If the incoming step has the 10% to 90% rise time t_r, then the rise time of the forward-propagating signal t_{fwd} is estimated as

$$t_{fwd} \approx \sqrt{t_r^2 + t_d^2} \approx \sqrt{t_r^2 + (2.2\tau)^2}. \tag{18}$$

The diode placed on a transmission line with characteristic impedance Z_0 presents impedance Z_d to an incoming harmonic wave with angular frequency ω:

$$Z_d = Z_0 \parallel R \parallel \frac{1}{j\omega C} = \frac{Z_0}{1 + Z_0/R + j\omega Z_0 C} \approx \frac{Z_0}{1 + j2\omega\tau}, \tag{19}$$

whereas the approximation assumes $R >> Z_0$. Setting $Z_x = Z_d$ and applying **Equation (1)**, the reflection coefficient Γ in the frequency domain calculates to

$$\Gamma(j\omega) = -\frac{Z_0/R + j\omega Z_0 C}{2 + Z_0/R + j\omega Z_0 C} \approx -\frac{j\omega\tau}{1 + j\omega\tau}. \tag{20}$$

For $\omega\tau < 1/2$ the denominator is approximately 1 and **Equation (20)** simplifies to

$$\Gamma(j\omega) \approx -j\omega\tau|_{\omega\tau < 1/2}. \tag{21}$$

The advantage of the gaussian edge over others, especially the linear-ramp edge, is its limited bandwidth and therefore effectively eliminates the need for windowing, provided the 3dB bandwidth of the gaussian edge is 3 times smaller than the maximum simulation frequency. It also comes closer to the shape of real world digital differential wave forms. The step with gaussian edge and normalized magnitude 1 has the time-domain representation

$$g(t) = \int_{-\infty}^{t} \frac{1}{\sqrt{4\pi a}} e^{-\frac{\upsilon^2}{4a}} d\upsilon \tag{22}$$

and, by applying the fourier transformation, following frequency-domain representation

$$G(\mathrm{j}\omega) = \frac{\mathrm{e}^{-a\omega^2}}{\mathrm{j}\omega}, \tag{23}$$

where $a = (0.275 t_r)^2$ and t_r is the 10% to 90% rise time of the step. Then, the reflected pulse $H(\mathrm{j}\omega)$ in response to an incoming gaussian step calculates to

$$H(\mathrm{j}\omega) = \Gamma(\mathrm{j}\omega) G(\mathrm{j}\omega) \tag{24}$$

and with the approximation of **Equation (21)** the reflected pulse can be approximated by

$$H(\mathrm{j}\omega) \approx -\tau \mathrm{e}^{-a\omega^2}. \tag{25}$$

Applying the inverse fourier transformation to **Equation (25)** gives the reflected pulse $h(t)$ in the time domain:

$$h(t) \approx -\frac{\tau}{\sqrt{4\pi a}} \mathrm{e}^{-\frac{t^2}{4a}}. \tag{26}$$

In general only the peak reflected signal magnitude Γ_{pk} is of interest. The peak of the reflected pulse is delayed approximately by the time constant τ of the diode, thus

$$\Gamma_{pk} = \left| \frac{\max(h(t))}{\max(g(t))} \right| \approx |h(\tau)| \approx \left. \frac{\tau}{t_r} \right|_{t_r > 8\tau}, \tag{27}$$

where t_r is the 10% to 90% rise time of the incoming step. **Equation (27)** is a good approximation for rise times as low as 8 times the time constant of the diode. For faster rise times, **Equation (27)** overestimates the peak reflected signal magnitude.

The peak reflected signal magnitude shown in **Figure 5** was calculated in the frequency domain by using the measured S-parameters ($\Gamma(\mathrm{j}\omega) = S_{11}$) to evaluate **Equation (24)**. Bearing in mind that the time domain signal must be real, following relation is given by the inverse fourier transformation:

$$h(\tau) = \frac{1}{2\pi} \int_{-\infty}^{\infty} H(\mathrm{j}\omega) \mathrm{e}^{\mathrm{j}\omega\tau} \mathrm{d}\omega = \frac{1}{\pi} \int_{0}^{\infty} \mathrm{Re}(H(\mathrm{j}\omega) \mathrm{e}^{\mathrm{j}\omega\tau}) \mathrm{d}\omega. \tag{28}$$

Once the peak reflected signal magnitude is given, the characteristic impedance simple calculates by rewriting **Equation (1)**:

$$Z_x = Z_0 \frac{1+\Gamma}{1-\Gamma}. \tag{29}$$

For small reflections of less than 0.1, the relative variation in impedance $\Delta Z / Z_0$ from the characteristic impedance Z_0 is approximately two times the reflection:

$$\frac{\Delta Z}{Z_0} = \frac{Z_x - Z_0}{Z_0} = \frac{2\Gamma}{1-\Gamma} \approx 2\Gamma|_{\Gamma < 0.1}. \tag{30}$$

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[2] JESD22-A114D, “Electrostatic Discharge (ESD) sensitivity testing Human Body Model (HBM),” JEDEC Solid State Technology Association, March 2006.

[3] IEC 61000-4-2, Electromagnetic Compatibility (EMC) Part 4: Testing and measurement techniques – Section 2: “Electrostatic discharge immunity test,” International Electrotechnical Commission, 1995.

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[5] High-Definition Multimedia Interface, Specification Version 1.3a, 10 November 2006.

[6] IEEE Std 1394b™-2002, IEEE Standard for a High-Performance Serial Bus—Amendment 2, IEEE Computer Society, 14 December 2002.

[7] Infineon Technologies: “Application Note No. 103: ESD and Antenna Protection using Infineon ESD0P8RFL”