# Application Note No. 136

## Low Cost, 3 Volt, +14 dBm 2.33 GHz SDARS Active Antenna 2nd Stage Low Noise Amplifier using the Infineon BFP640 SiGe Transistor

RF & Protection Devices

Never stop thinking

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**Application Note No. 136**

**Revision History: 2008-01-07, Rev. 1.2**

| **Previous Version: 2004-11-12, Rev. 1.1** | |
|---|---|
| **Page** | **Subjects (major changes since last revision)** |
| All | Small changes in figure descriptions |
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# 1 Low Cost, 3 Volt, +14 dBm 2.33 GHz SDARS Active Antenna 2nd Stage Low Noise Amplifier using the Infineon BFP640 SiGe Transistor

### Overview

The Silicon-Germanium BFP640 SiGe Low Noise Transistor is shown in an SDARS active antenna LNA application. The BFP640 is targeted for the 2nd stage in a 3 stage SIRIUS LNA chain. The demo board is standard FR4 material and "0402" case sizes components are used throughout. A total of approximately 41 mm² of PCB area is required, and the total component count, including the BFP640 and all passives, is 12.

### SDARS Active Antenna LNA

2320 - 2332.5 MHz (SIRIUS, 3 Stages)

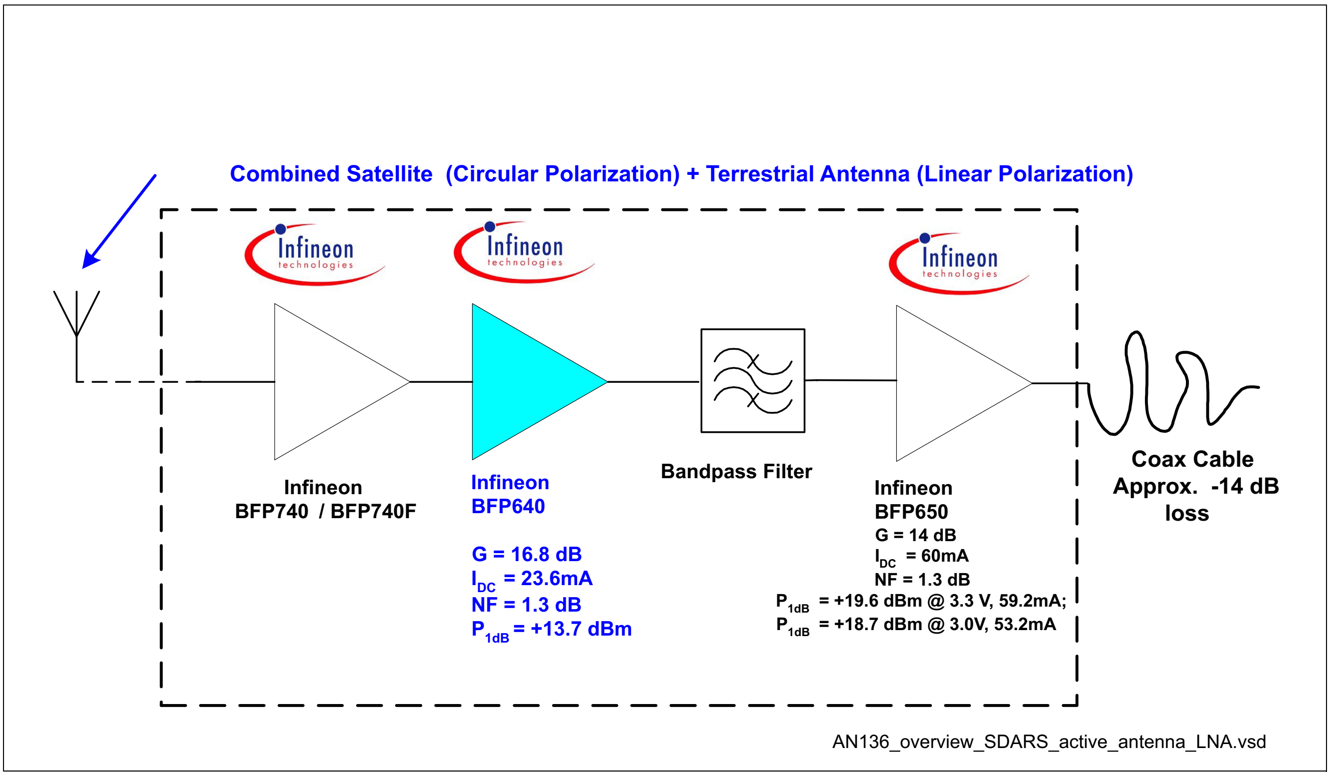



**Figure 1 Overview of SDARS Active Antenna LNA**

### Summary

Achieved 16.8 dB gain, 1.3 dB Noise Figure over the 2320 - 2345 MHz band, drawing 23.6 mA @ 3.0 V. Noise figure result does NOT "back out" FR4 PCB losses - if PCB loss at LNA input were extracted, Noise Figure result would be approximately 0.1 - 0.2 dB lower. Amplifier is unconditionally stable from 5 MHz to 6 GHz.
Output $P_{1dB}$ = +13.7 dBm @ 3 V. Input 3rd Order Intercept = +13.01 dBm @ 2332 MHz, Output $IP_3$ = +29.8 dBm.

**PCB Cross - Section Diagram**

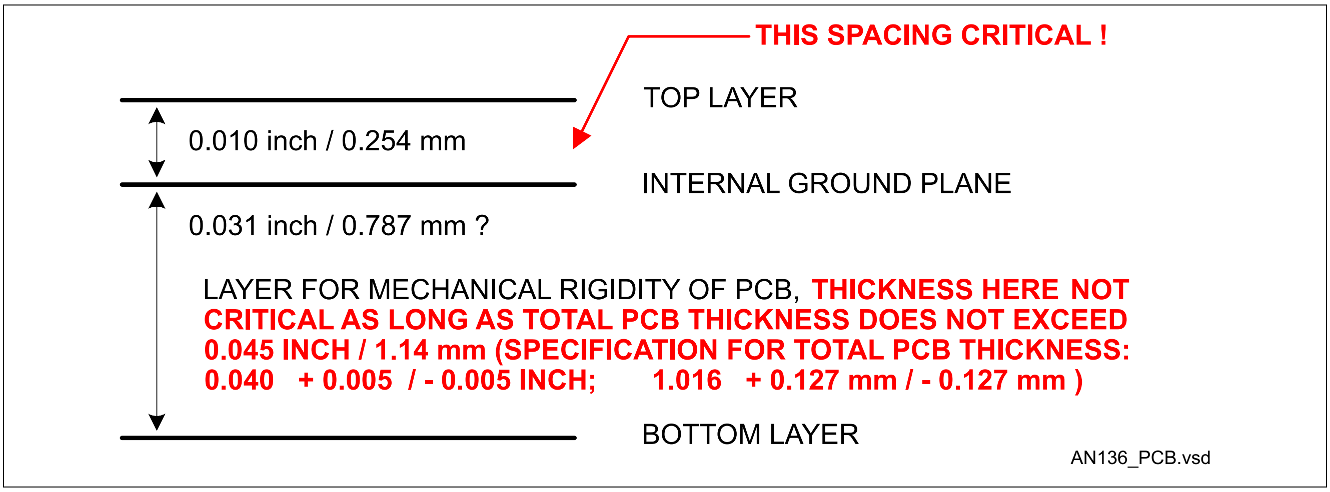



**Figure 2 PCB - Cross Sectional Diagram**

**Schematic Diagram**

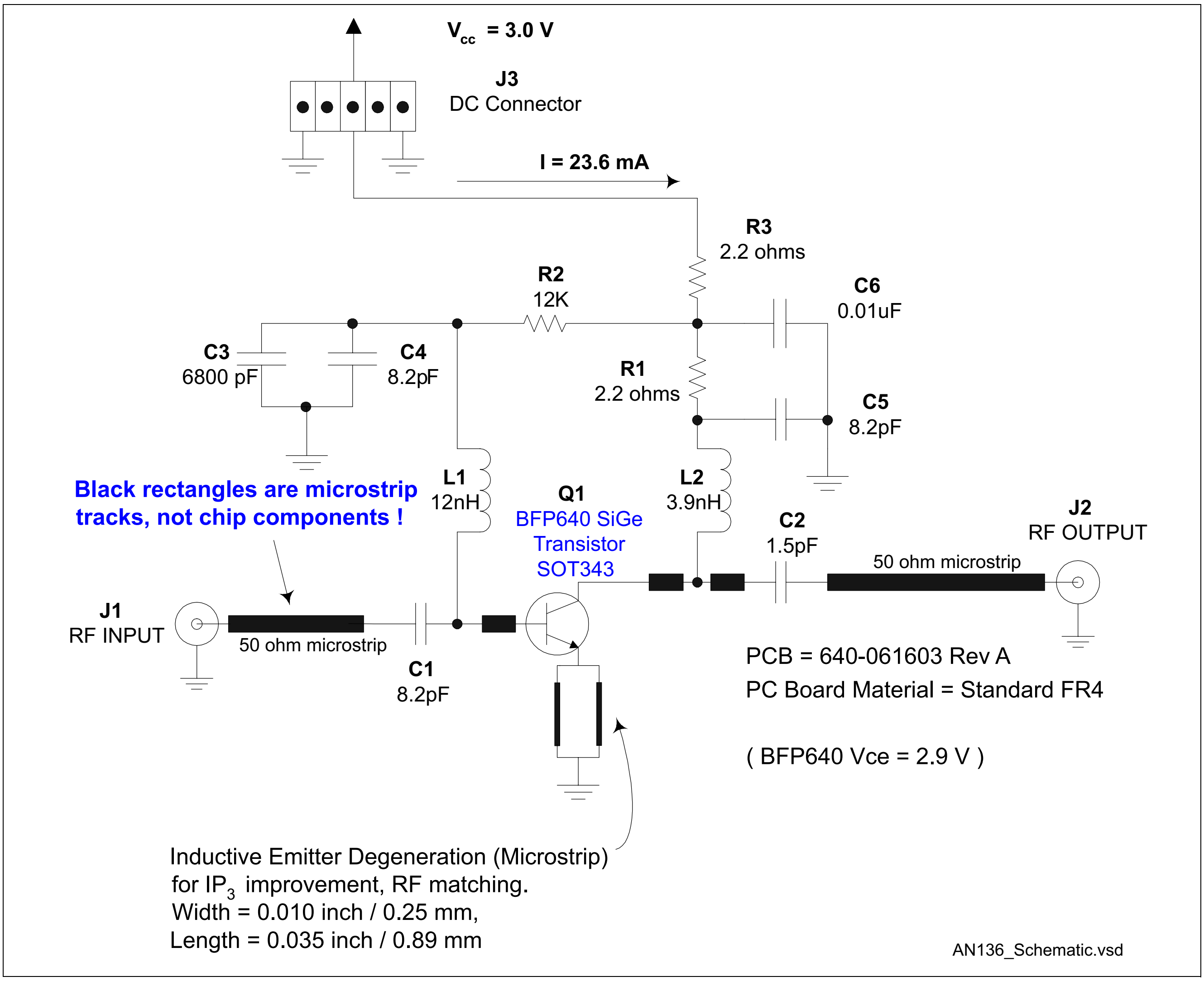



**Figure 3 Schematic Diagram**

**Summary of Data**

$T$ = 25 °C, Network analyzer source power = -25 dBm

**Table 1 Summary of Data**

| Parameter | Result | Comments |
|---|---|---|
| Frequency Range | Under 2320 - over 2345 MHz | Covers both XM Radio and SIRIUS frequency bands. |
| DC Current | 23.6 mA @ 3.0 V | Note power supply voltage is measured directly across PCB supply line and ground, to eliminate voltage drop across wire harness. |
| Gain | 16.9 dB @ 2320 MHz<br>16.8 dB @ 2332.5 MHz<br>16.8 dB @ 2345 MHz | Negligible change in gain or matching at 3.3 or 3.0 volts. |
| Noise Figure | 1.3 dB @ 2320 MHz<br>1.3 dB @ 2332.5 MHz<br>1.4 dB @ 2345 MHz | These values do not extract PCB losses, etc. resulting from FR4 board an passives used on PCB - these results are at input SMA connector. |
| Input $P_{1dB}$ | -2.1 dBm @ 3.0 V | Measured @ 2332.5 MHz. See **Figure 8** |
| Output $P_{1dB}$ | +13.7 dBm @ 3.0 V | See **Figure 8** |
| Power Added Efficiency (PAE) at 1 dB Compression Point | 32.2% @ 3.0 V | PAE = $(P_{OUT} - P_{IN}) / (V_{CC} \times I_C)$<br>Decent results for a “Class A” amplifier. |
| Input 3rd Order Intercept | +13.0 dBm @ 2332 MHz | Measured at 3.3 V, see **Figure 15** and **Figure 16** |
| Output 3rd Order Intercept | +29.8 dBm @ 2332 MHz | Measured at 3.3 V, see **Figure 15** and **Figure 16** |
| Input Return Loss | 17.8 dB @ 2320 MHz<br>18.1 dB @ 2332.5 MHz<br>15.5 dB @ 2345 MHz | |
| Output Return Loss | 14.6 dB @ 2320 MHz<br>14.2 dB @ 2332.5 MHz<br>13.9 dB @ 2345 MHz | |
| Reverse Isolation | 21.7 dB @ 2320 MHz<br>21.6 dB @ 2332.5 MHz<br>21.6 dB @ 2345 MHz | |

**Noise Figure, Plot, 2232.5 MHz to 2432.5 MHz, Center of Plot (x-axis) is 2332.5 MHz.**

Rohde & Schwarz FSEK3 12 Nov 2004

Noise Figure / Rauschmessung

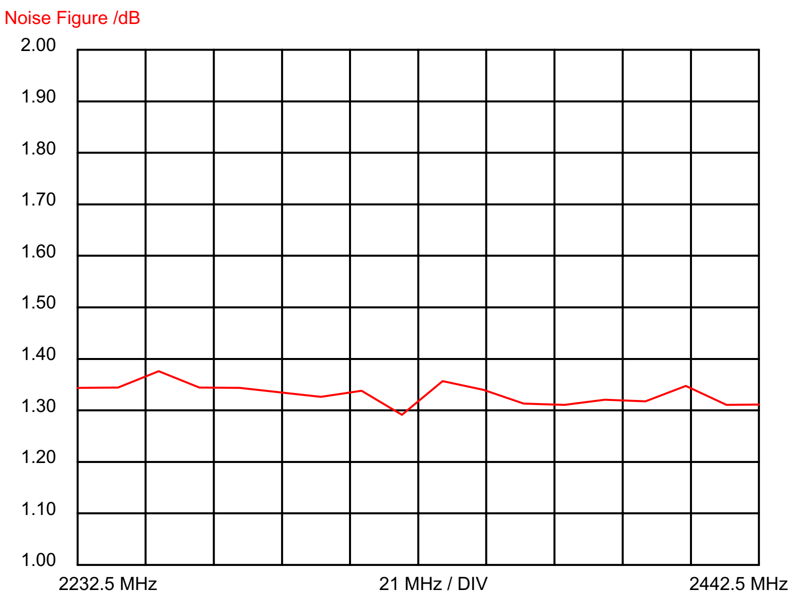
| | |
|---|---|
| EUT Name: | BFP640 2.33 GHz SDARS Active Antenna LNA 2nd Stage |
| Manufacturer: | Infineon Technologies |
| Operating Conditions: | V = 3.0 V, I = 23.6 mA, T = 25 C |
| Operator Name: | Gerard Wevers |
| Test Specification: | LWR_SD00057_LNA_P |
| Comment: | PCB = 740-080704 Rev A |
| | 12 November 2004 |

Analyzer

| | | |
|---|---|---|
| RF Att: 0.00 dB | RBW : 1 MHz | Range: 40.00 dB |
| Ref Lvl: -41.00 dBm | VBW : 100 Hz | Ref Lvl auto: ON |

Measurement

| | | |
|---|---|---|
| 2nd stage corr: ON | Mode: Direct | ENR: HP346A.ENR |




AN136_plot_nf.vsd

**Figure 4 Noise Figure**

**Noise Figure, Tabular Data**

From Rohde & Schwarz FSEK3 + FSEB30
System Preamplifier = MITEQ SMC-02

**Table 2 Noise Figure**

| Frequency | Noise Figure |
|---|---|
| 2232.5 MHz | 1.34 dB |
| 2245 MHz | 1.34 dB |
| 2257.5 MHz | 1.38 dB |
| 2270 MHz | 1.34 dB |
| 2282.5 MHz | 1.34 dB |
| 2295 MHz | 1.33 dB |
| 2307.5 MHz | 1.33 dB |
| 2320 MHz | 1.34 dB |
| 2332.5 MHz | 1.29 dB |
| 2345 MHz | 1.36 dB |
| 2357.5 MHz | 1.34 dB |
| 2370 MHz | 1.31 dB |
| 2382.5 MHz | 1.31 dB |
| 2395 MHz | 1.32 dB |
| 2407.5 MHz | 1.32 dB |
| 2420 MHz | 1.35 dB |
| 2432.5 MHz | 1.31 dB |
| 2442.5 MHz | 1.31 dB |

**Scanned Image of PC Board**

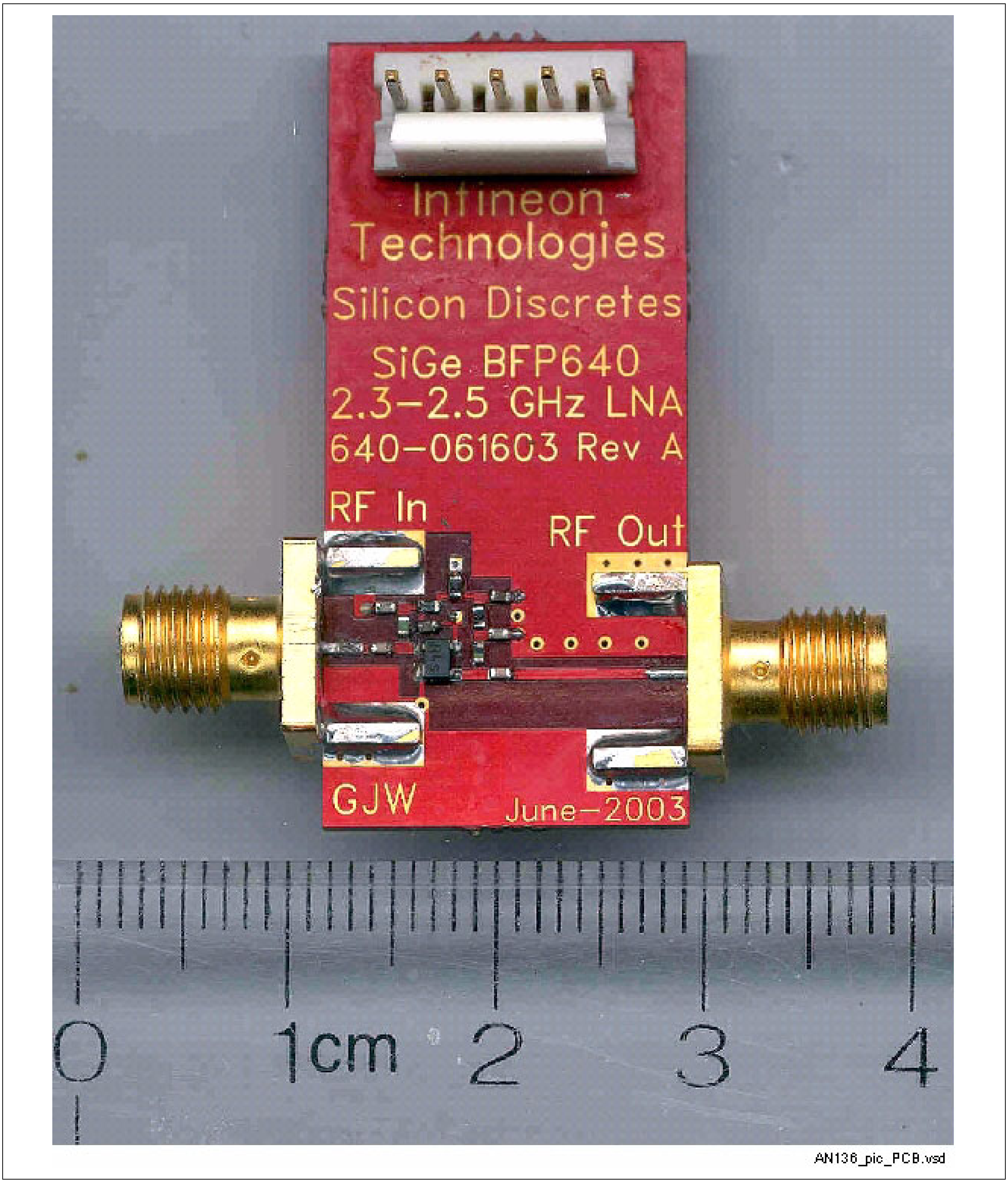



**Figure 5 Image of PC Board**

**Scanned Image of PC Board, Close-In Shot.**

Total PCB area used ≅ 41 mm²

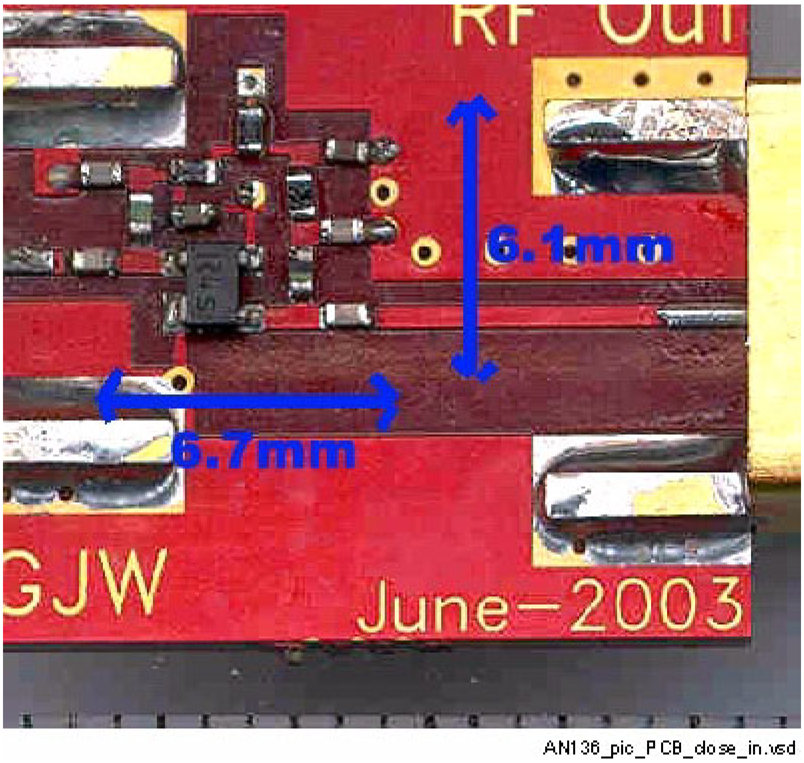



**Figure 6 Image of PC Board, Close-In Shot**

**Stability Factor “K” and Stability Measure “$B_1$” (5 MHz - 6 GHz)**

Plots are generated from real, measured S parameters taken from the demo PC board, NOT a simulation. S parameters are exported from Network Analyzer, then imported into Eagleware GENESYS software, which calculates and plots K and $B_1$. Note K > 1 and $B_1$ > 0, showing unconditional stability.

K is trace in red color (bottom trace) and is assigned to left vertical axis at bottom of page. Note K > 1.

“Glitch" at low frequencies e.g. < 200 MHz is due to lack of dynamic range in network analyzer - S parameter S12 becomes vanishingly small as one moves lower in frequency, which causes expression for calculating "K" to "blow up”.

$B_1$ is trace is blue in color (top trace) and is assigned to right vertical.

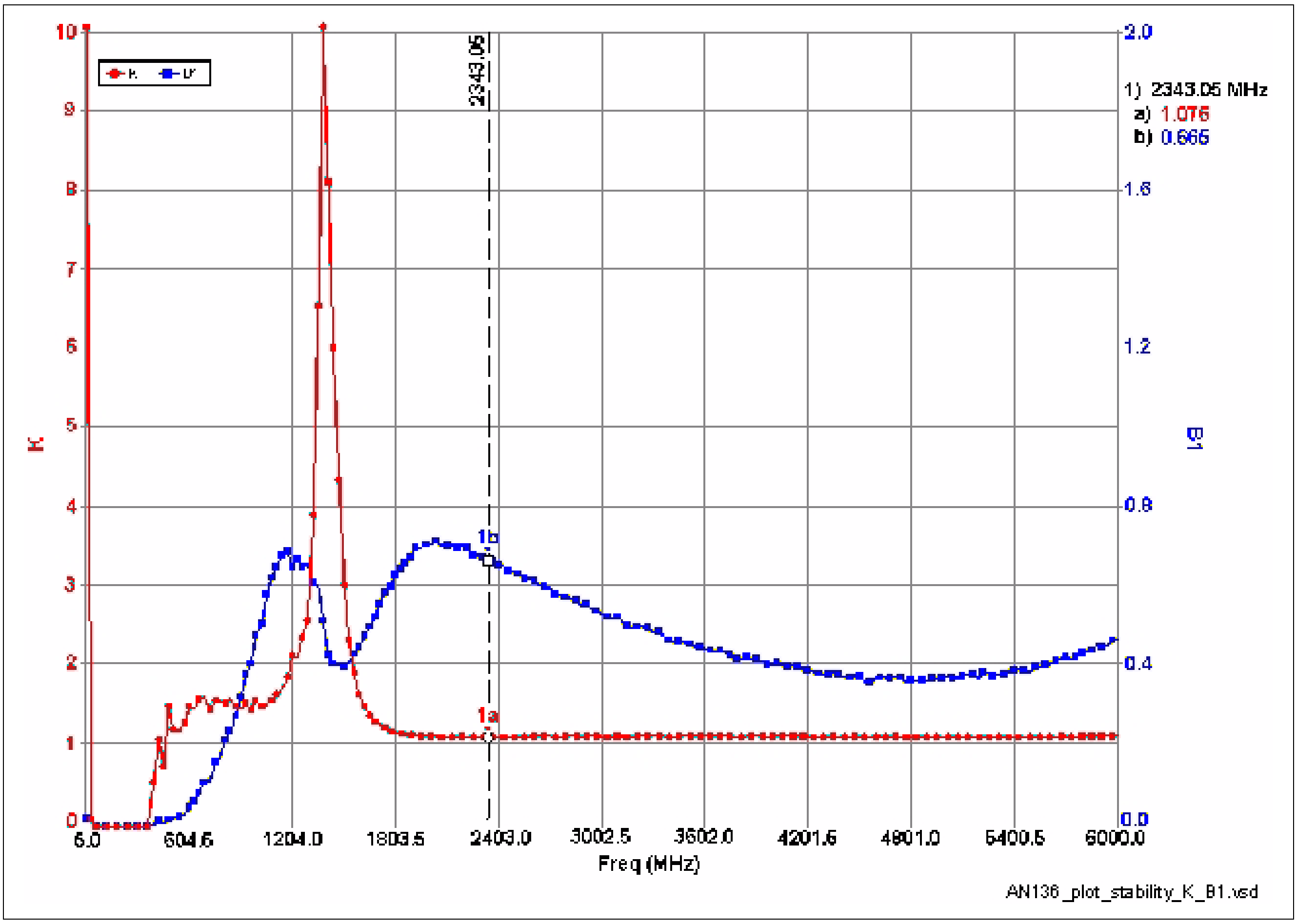



**Figure 7 Plot of K(f) and $B_1$(f)**

## Gain Compression Test

$V_{CC}$ = 3.0 V

Network Analyzer is set to "CW" mode - e.g. set to a single frequency, with power sweep. Input power is swept from -25 dBm to +3 dBm at 2332.5 MHz.Amplifier hits Input 1 dB compression point ($IP_{1dB}$) at - 2.1 dBm input power. Output $P_{1dB}$ = - 2.1 dBm + 15.8 dB gain at $P_{1dB}$ point => +13.7 dBm, or 23.4 mW.

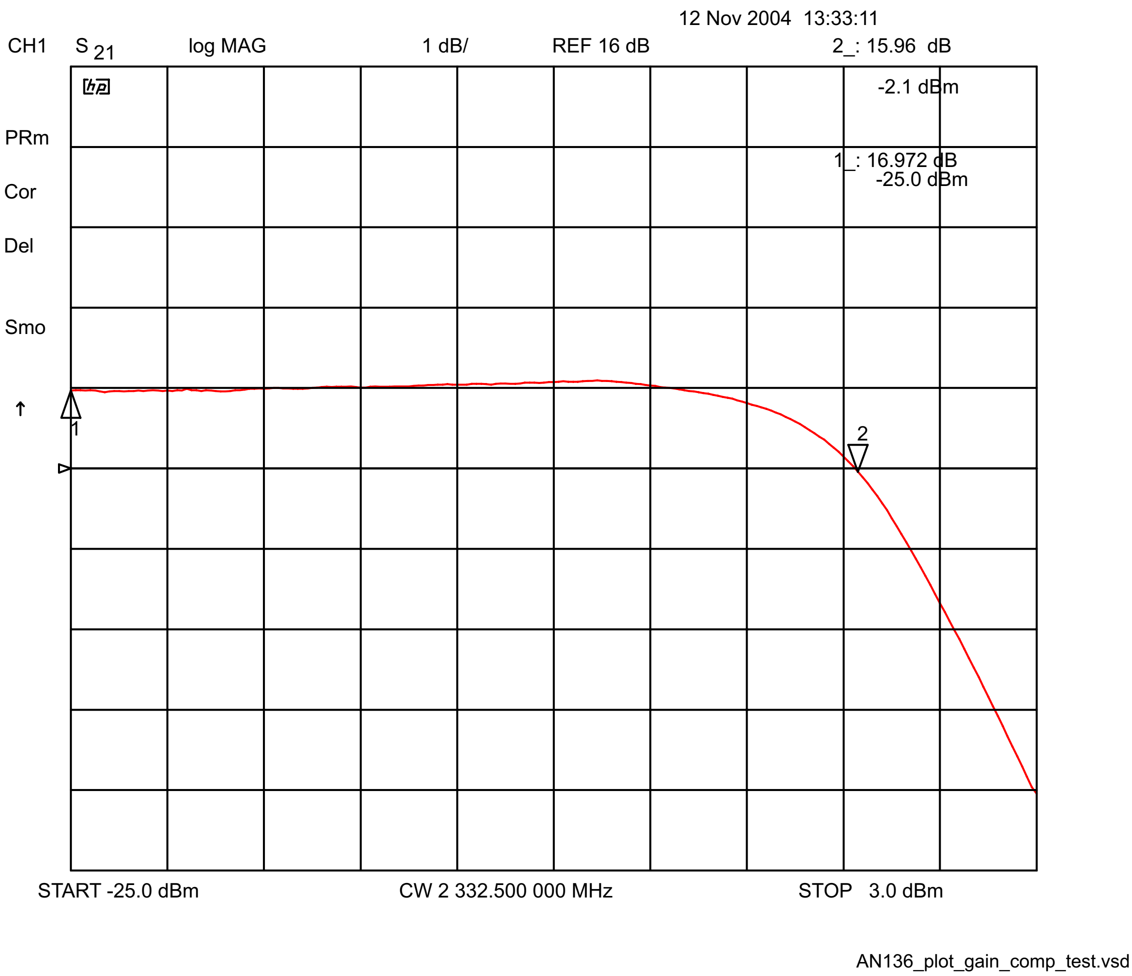



**Figure 8 Plot of Gain Compression Test**

**Input Return Loss, Log Mag**

5 MHz - 6 GHz

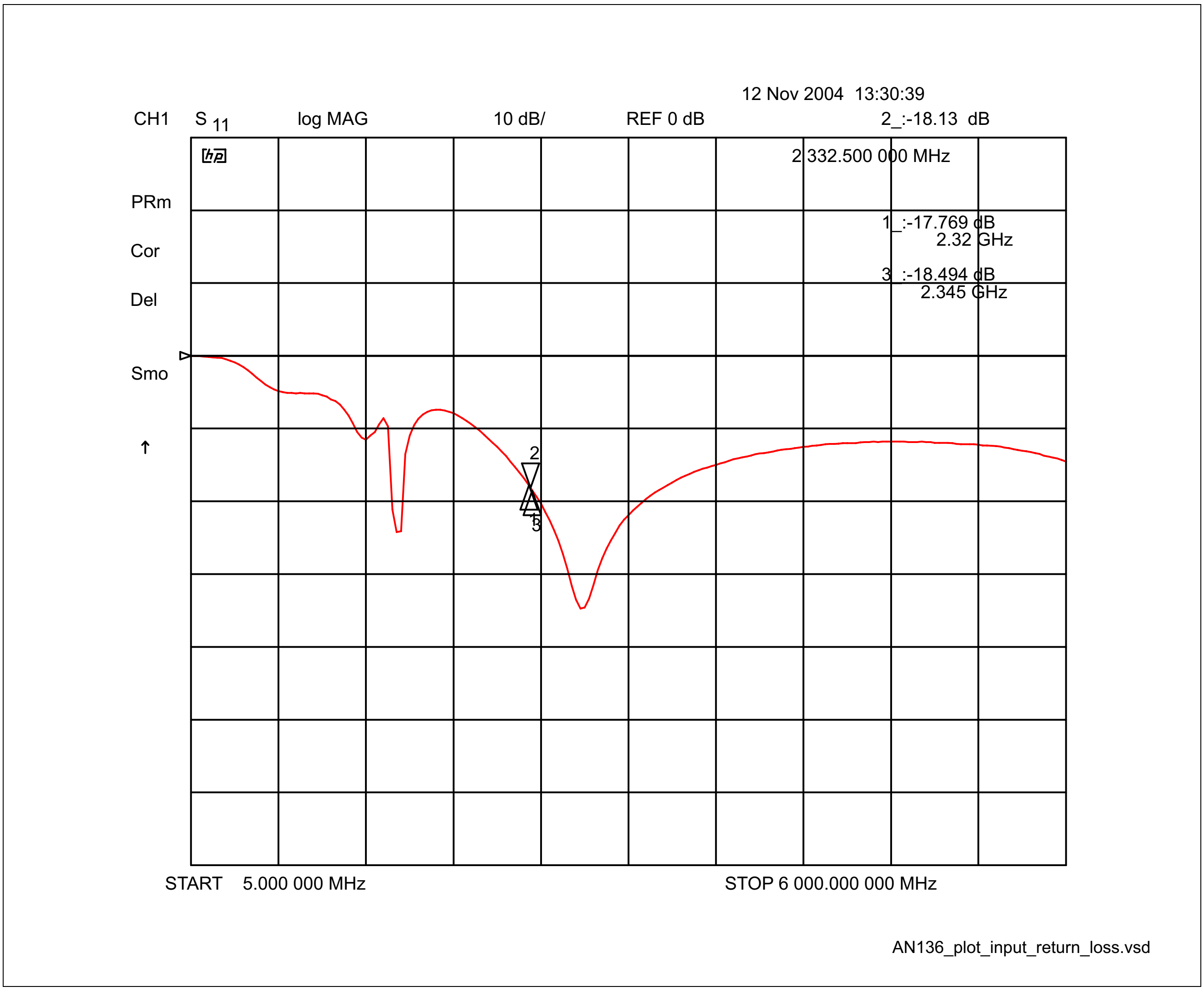



**Figure 9 Plot of Input Return Loss**

**Input Return Loss, Smith Chart**

Reference Plane = Input SMA Connector on PC Board
5 MHz - 6 GHz

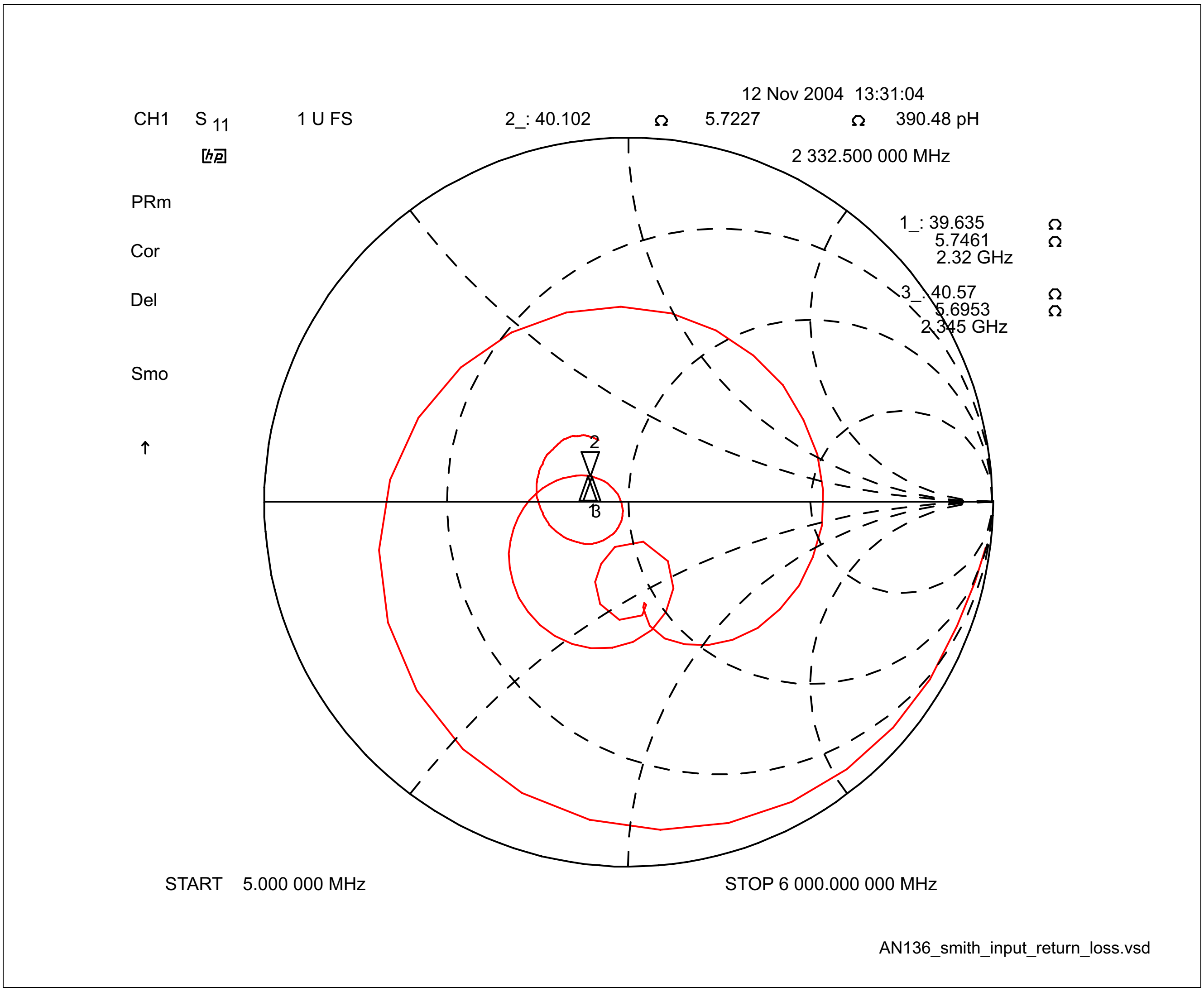



**Figure 10 Smith Chart of Input Return Loss**

**Forward Gain, Wide Sweep**

5 MHz - 6 GHz

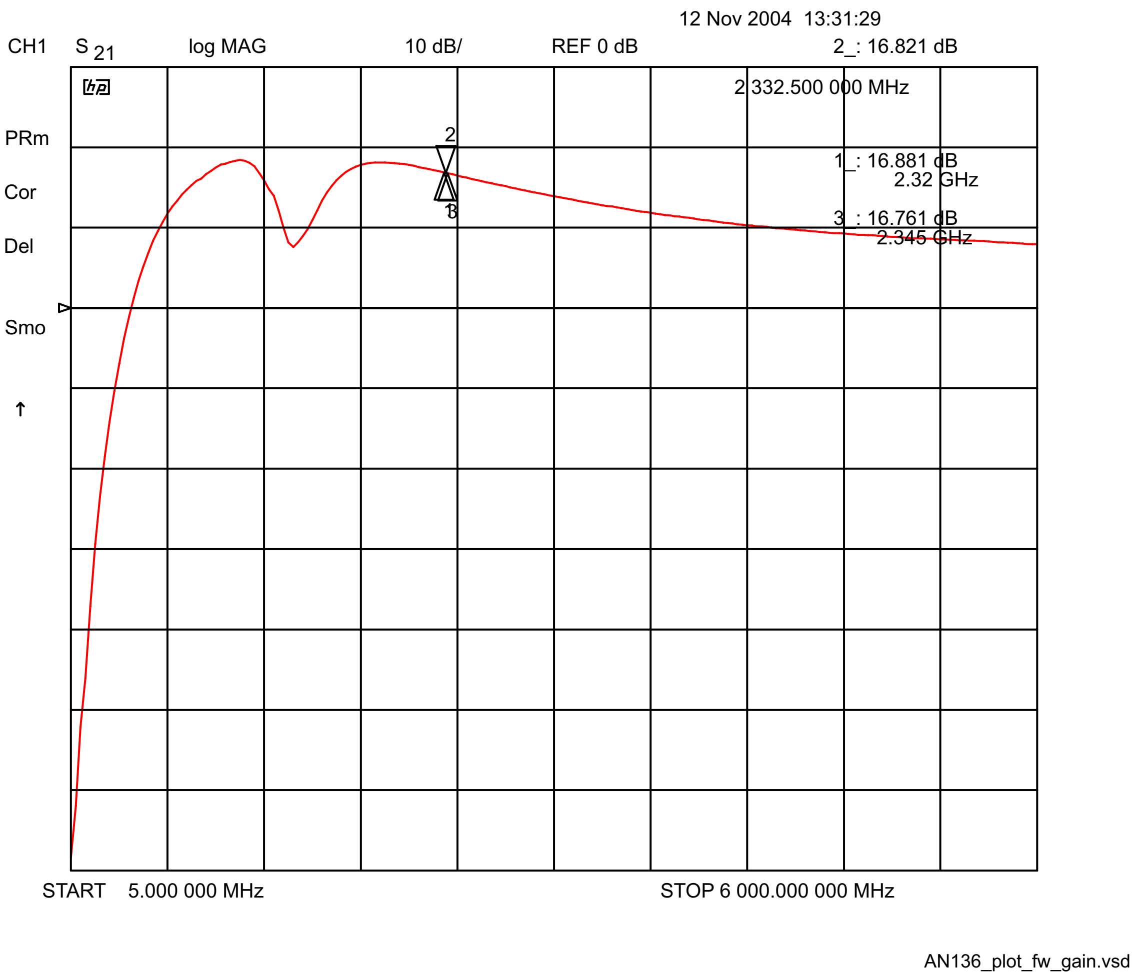



**Figure 11 Plot of Forward Gain**

**Reverse Isolation**

5 MHz - 6 GHz

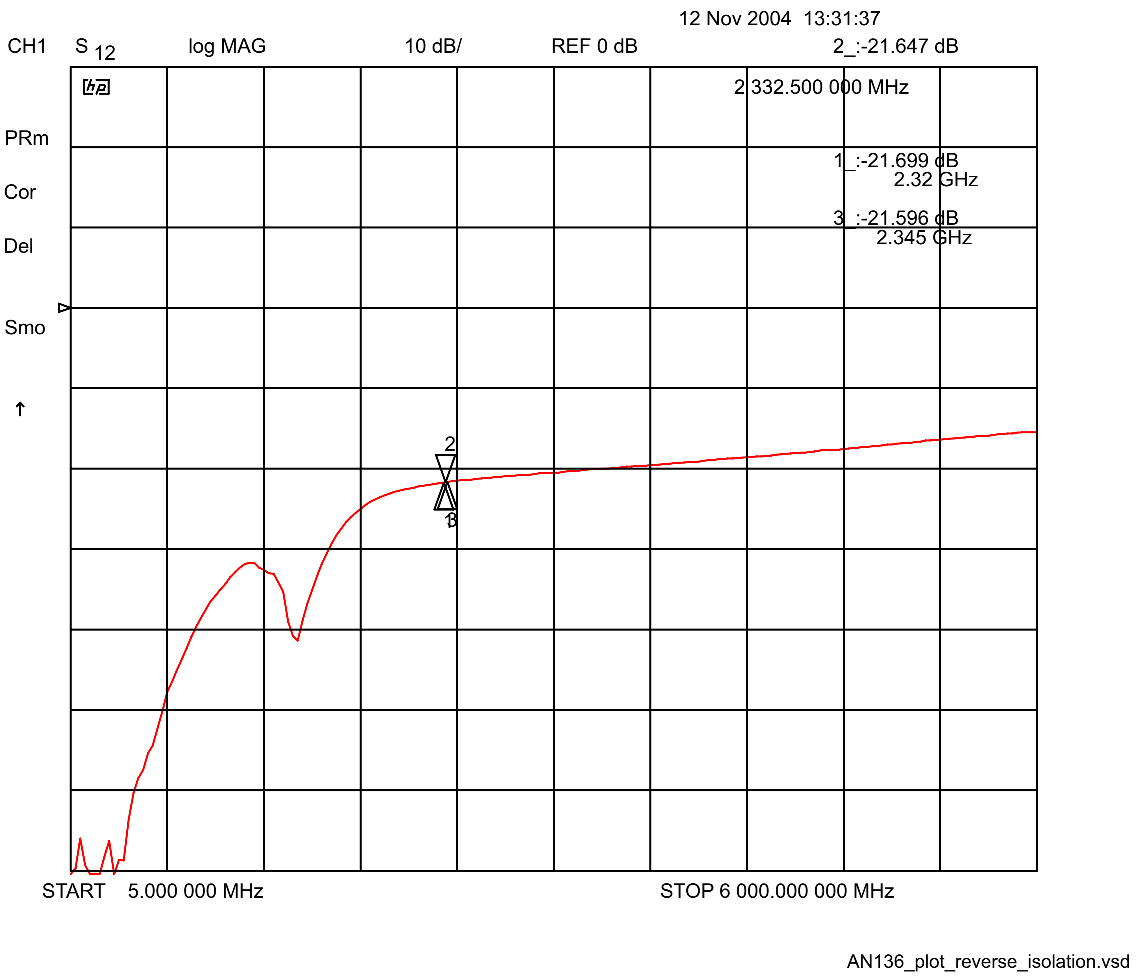



**Figure 12 Plot of Reverse Isolation**

**Output Return Loss, Log Mag**

5 MHz - 6 GHz

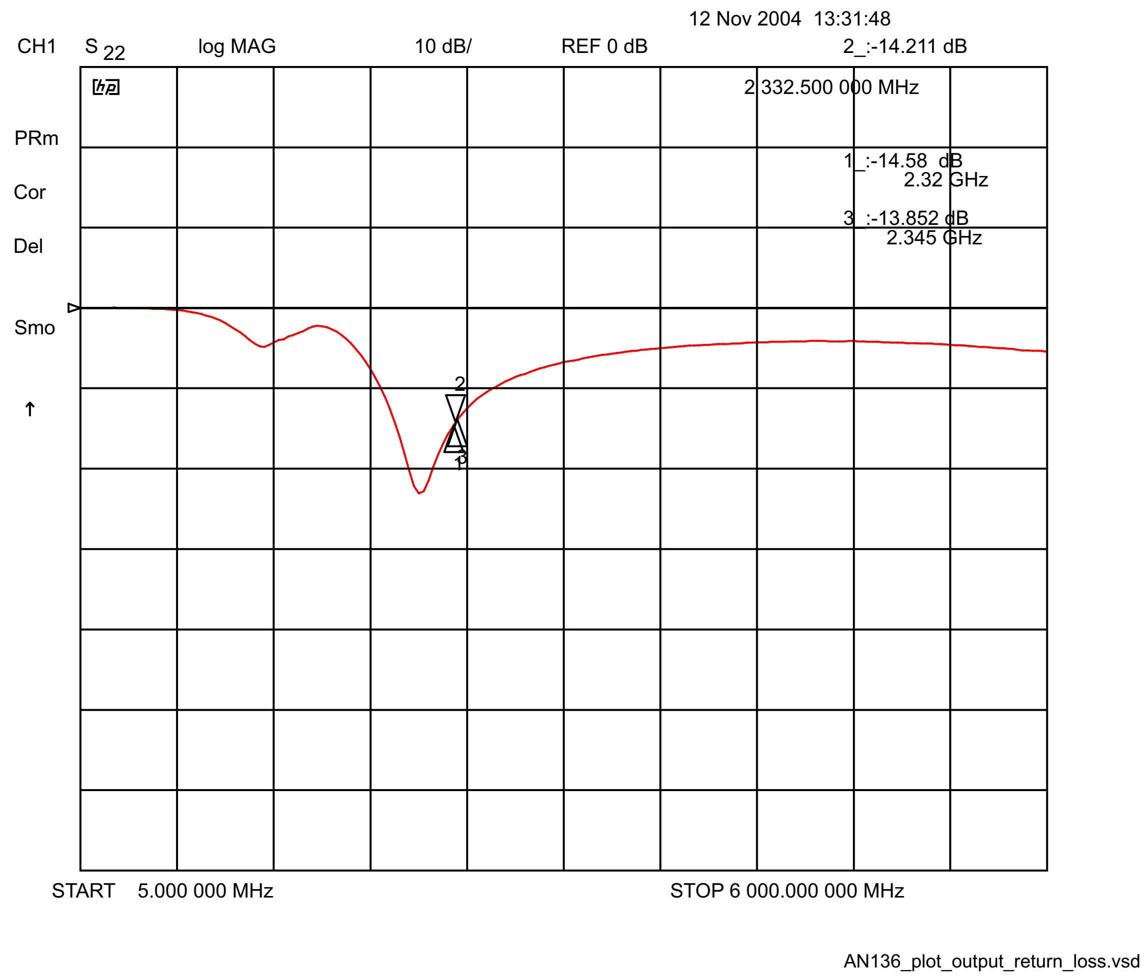



**Figure 13 Plot of Output Return Loss**

**Output Return Loss, Smith Chart**

Reference Plane = Output SMA Connector on PC Board
5 MHz - 6 GHz

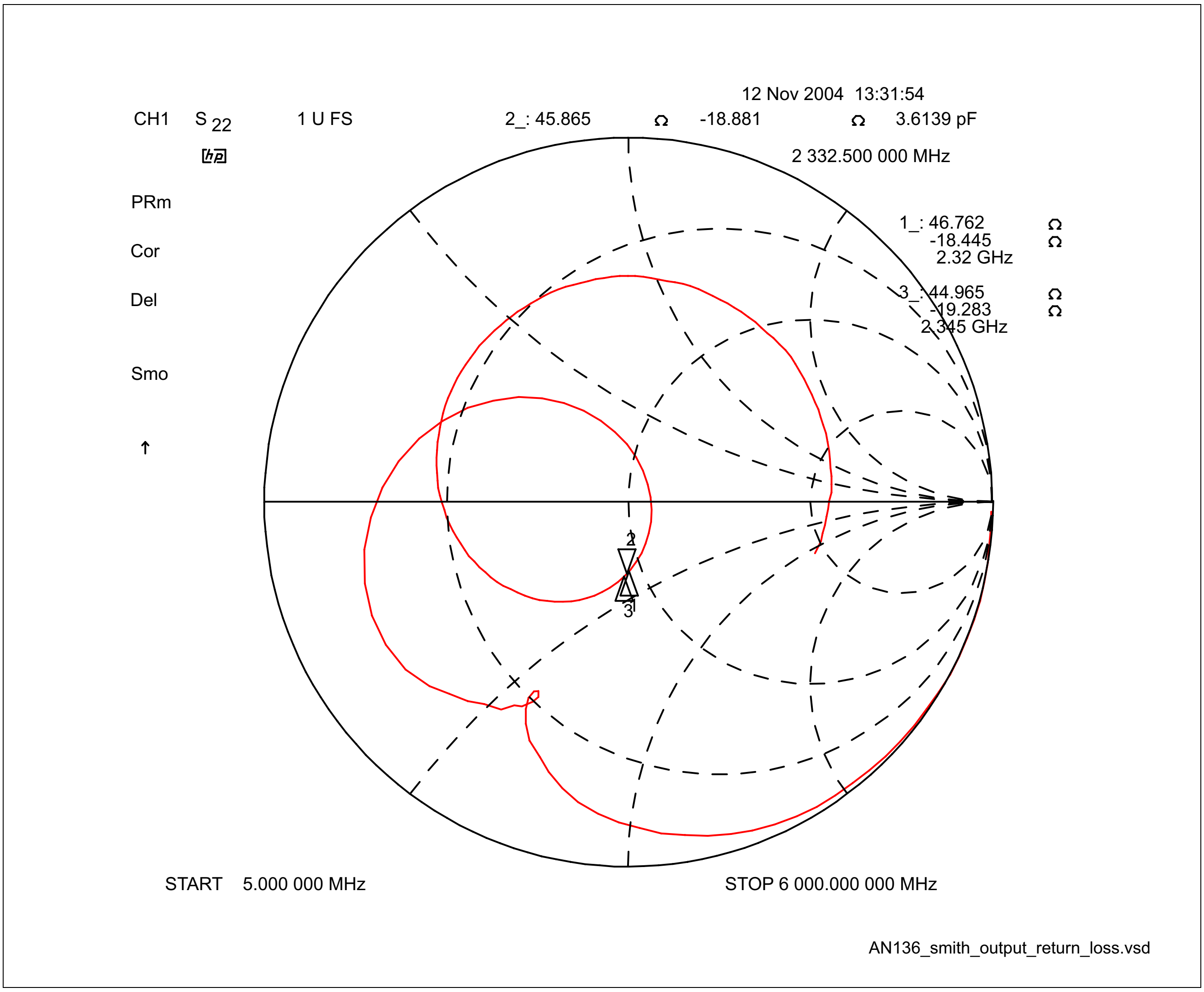



**Figure 14 Smith Chart of Output Return Loss**

**Two-Tone Test, 2332 MHz**

Input Stimulus for Amplifier Two-Tone Test.
$f_1$ = 2332 MHz, $f_2$ = 2333 MHz, -19 dBm each tone.

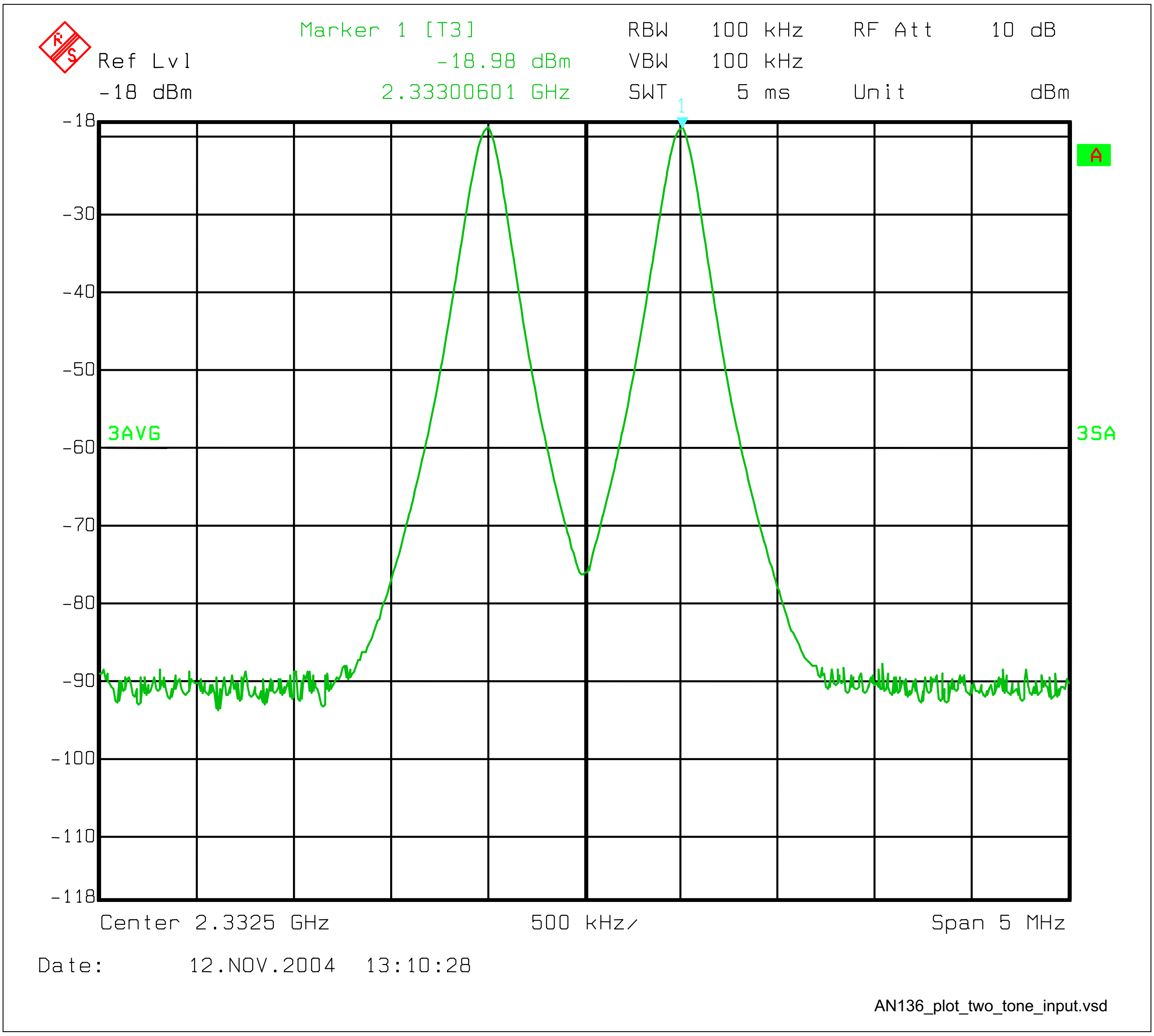



**Figure 15 Tow-Tone Test, Input Stimulus @ 2332 MHz**

**Two-Tone Test, 2332 MHz**

LNA Response to Two-Tone Test.

Input $IP_3$ = -19 + (64.0 / 2) = +13.0 dBm
Output $IP_3$ = +13.0 dBm + 16.8 dB gain = +29.8 dBm

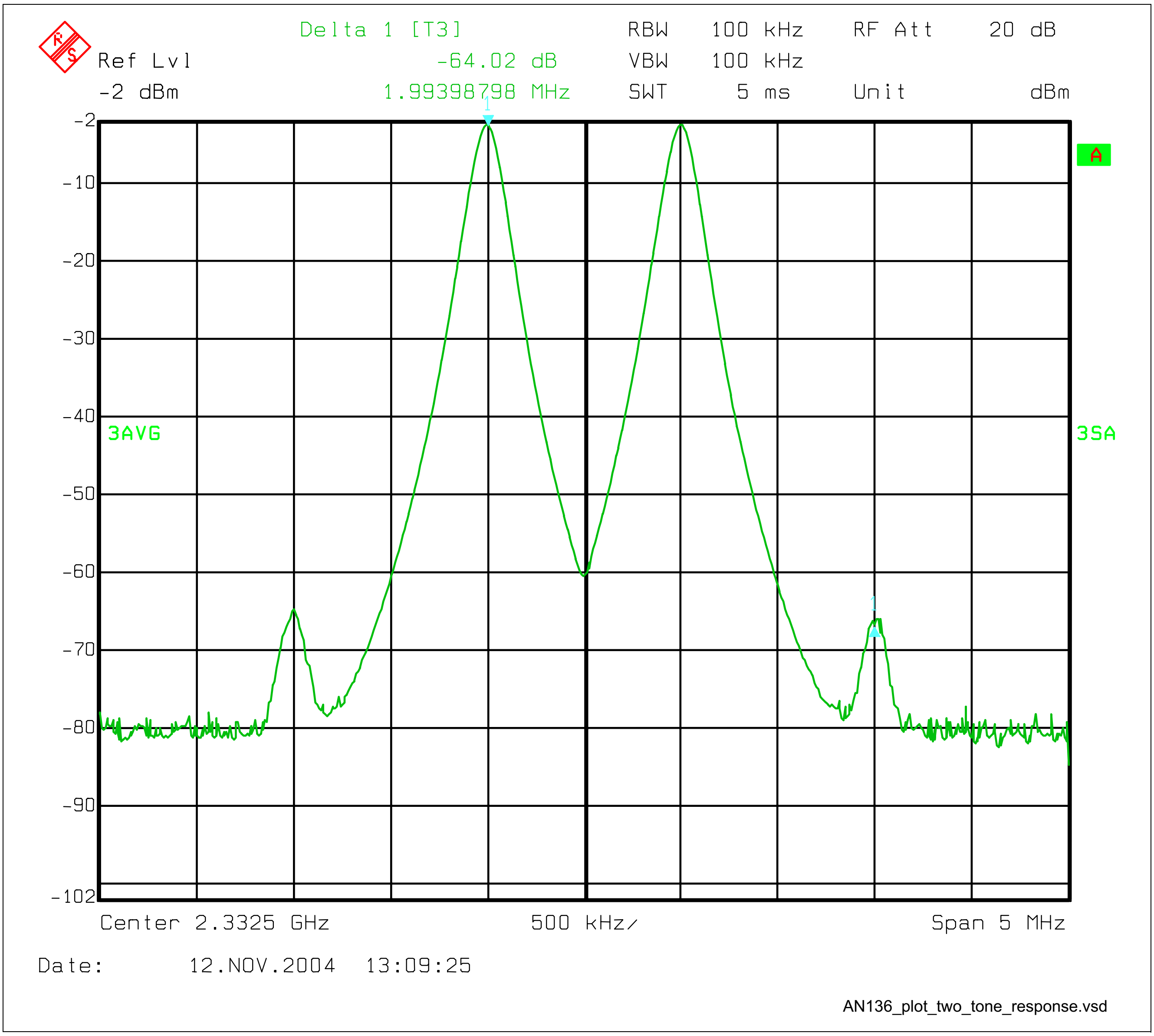



**Figure 16 Tow-Tone Test, LNA Response @ 2332 MHz**