Application Note No. 131

A Low Cost, Two Stage LNA for 5 to 6 GHz "802.11a" Applications using the SiGe BFP640

RF & Protection Devices

Never stop thinking

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Revision History: 2007-11-27, Rev. 1.2

Previous Version: 2002-11-16, Rev. 1.1

Page	Subjects (major changes since last revision)
All	Small changes in figure descriptions

1 A Low Cost, Two Stage LNA for 5 to 6 GHz "802.11a" Applications using the SiGe BFP640

Overview

- The Silicon-Germanium BFP640 is evaluated on a PCB to show the feasibility of a very low-cost, discrete Two-Stage LNA design in the 5 - 6 GHz range.
- The Printed Circuit Board Used is PCB 640-052402 Revision A. Standard FR4 material is used. Note that the PCB allows for the tune / test of each stage separately, prior to integrating the two stages. This is achieved with a third SMA RF connector positioned between the two stages.
- Low-cost, standard SMT passive components are used
- Total PCB area used for both stages is approximately 100 mm². Note that further reduction in PCB area is possible.
- Achieved > 20 dB gain, 1.4 dB Noise Figure at 5450 MHz, on 3.3 V supply, drawing 15.9 mA. Note noise figure result does NOT "back out" FR4 PCB losses - if the PCB loss at LNA input were extracted, Noise Figure Results would be approximately 0.3 dB lower.

PCB Cross - Section Diagram

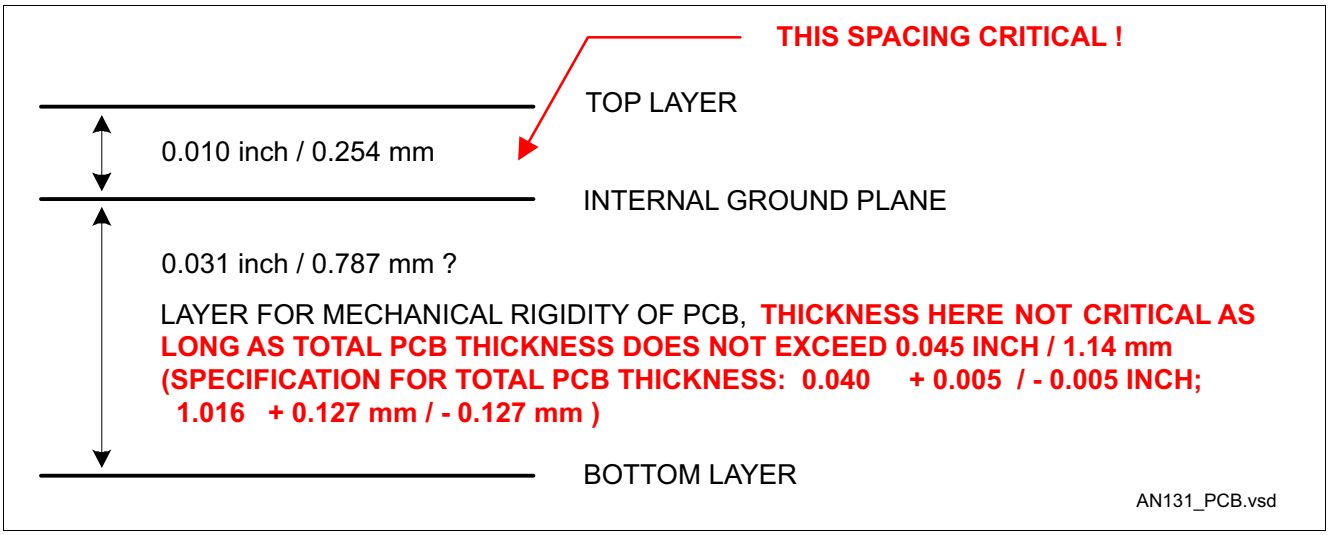


Figure 1 PCB - Cross Sectional Diagram

Summary of Data for Two-Stage Cascade

T = 25 °C, network analyzer source power = -35 dBm

Table 1 Summary of Data for Two-Stage Cascade

Parameter	Result	Comments
Frequency Range	5 - 6 GHz	Various portions of this range are usable on a worldwide basis for 802.11b, HiperLAN
DC Current	15.9 mA	Low current consumption
DC Voltage, V_{CC}	3.3 V	
Collector-Emitter Voltage, V_{CE}	≅ 2.9 V, each stage	BFP640 BV_{CEO} of 4.0 V would permit higher voltage operation. Higher bias voltage would improve linearity and slightly increase gain
Gain	22.7 dB @ 5150 MHz 22.4 dB @ 5250 MHz 22.1 dB @ 5350 MHz 21.6 dB @ 5470 MHz 20.2 dB @ 5825 MHz	
Cascade Noise Figure	1.4 dB @ 5150 MHz 1.4 dB @ 5250 MHz 1.4 dB @ 5350 MHz 1.4 dB @ 5470 MHz 1.5 dB @ 5825 MHz	
Input P_{1dB}	-14.7 dBm @ 5350 MHz	See input power sweep vs. gain plot, **Figure 6**.
Input 3rd Order Intercept	+4.6 dBm @ 5350 MHz	Please see plots **Figure 13** & **Figure 14**
Input Return Loss	12.2 dB @ 5150 MHz 13.3 dB @ 5250 MHz 14.5 dB @ 5350 MHz 16.0 dB @ 5470 MHz 19.9 dB @ 5825 MHz	Good broadband input match
Output Return Loss	9.7 dB @ 5150 MHz 10.5 dB @ 5250 MHz 12.2 dB @ 5350 MHz 13.8 dB @ 5470 MHz 19.9 dB @ 5825 MHz	Good broadband output match
Reverse Isolation	34.9 dB @ 5150 MHz 34.0 dB @ 5250 MHz 34.5 dB @ 5350 MHz 34.7 dB @ 5470 MHz 33.7 dB @ 5825 MHz	

Bill of Material

Table 2 Bill of Material, Complete Two-Stage Cascade

Reference Designator	Value	Manufacturer	Case Size	Function
C1, C2, C7	1.5 pF	Various	0402	DC blocking
C4. C5, C9, C10	1.5 pF	Various	0402	RF bypass / RF block
C3, C6, C8, C11	0.033 µF	Various	0402	Low frequency ground at base (input Third-Order Intercept improvement), low frequency decoupling / blocking
L1, L4	6.2 nH	Murata LQP15M tight tolerance inductor (former Murata part number = LQP10A)	0402	RF choke to DC bias on base of Q1 and Q2
L2, L5	5.6 nH	Murata LQP15M tight tolerance inductor	0402	RF choke to collector of Q1 and Q2; also influences output match of each stage
L3	1.3 nH	Murata LQP15M tight tolerance inductor	0402	Output matching, stage 1
L6	1.5 nH	Murata LQP15M tight tolerance inductor	0402	Output matching, stage 2
R1, R4	10 Ω	Various	0402	For stability, output matching
R2, r5	43 kΩ	Various	0402	DC bias for base of Q1 and Q2
R3, R6	30 Ω	Various	0402	Drop supply voltage by approx. 0.3 V, provide DC feedback for bias compensation (beta variation, temperature, etc.)
Q1, Q2	-	Infineon Technologies	SOT-343	BFP640F SiGe Transistor, f_T = 36 GHz
J1, J2, J3	-	Johnson 142-0701-841	-	RF input / output connectors (J2 only used when testing stages individually)
J4	-	AMP 5 pin header MTA-100 series 640456-5 (standard pin plating) or 641215-5 (gold plated pins)	-	DC connector Pins 1, 5 = ground Pin 3 = V_{CC} Pins 2, 4 = no connection

Schematic Diagram, Two-Stage Cascade

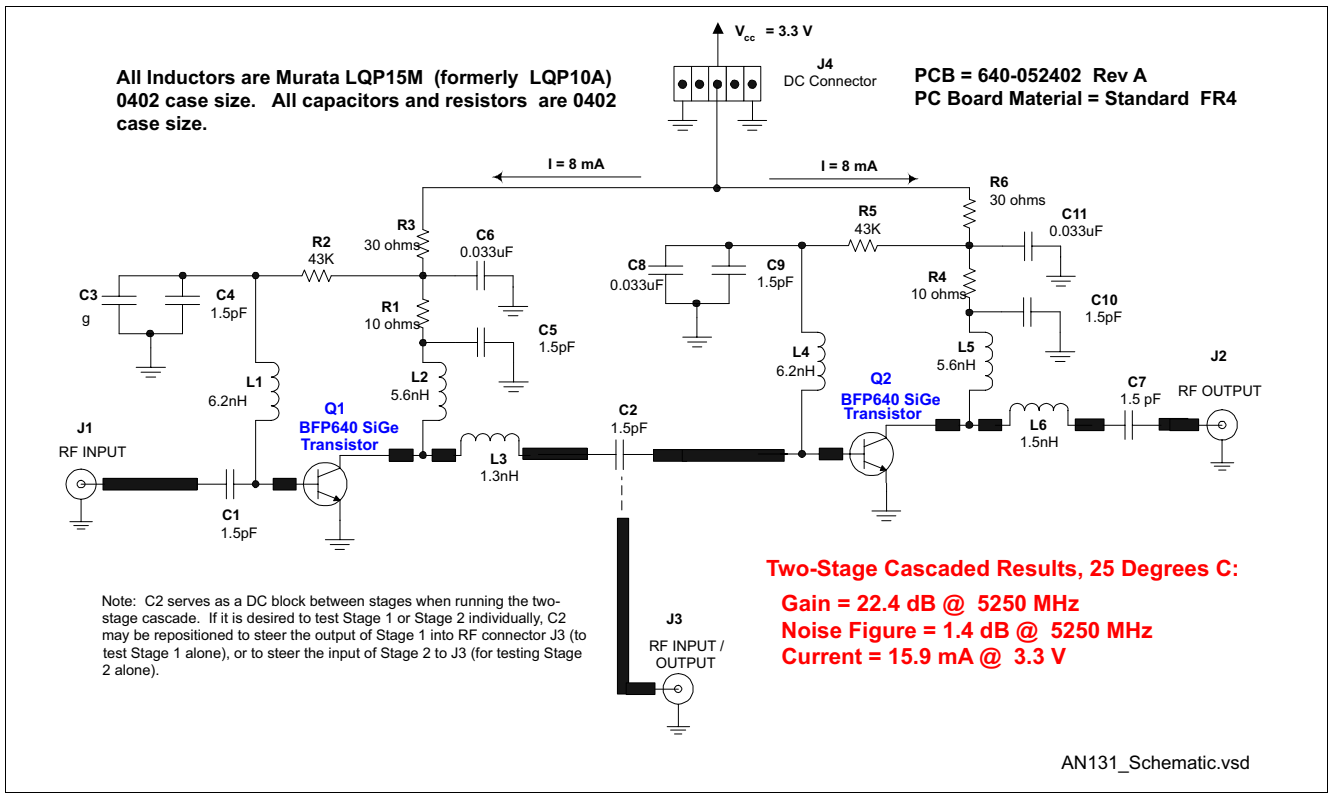


Figure 2 Schematic Diagram

Noise Figure, Plot, Two-Stage Cascade, Center of Plot (x-axis) is 5500 MHz.

Rohde and Schwarz FSEK3 V2.00

16 Nov 2002

BFP640 Noise Figure

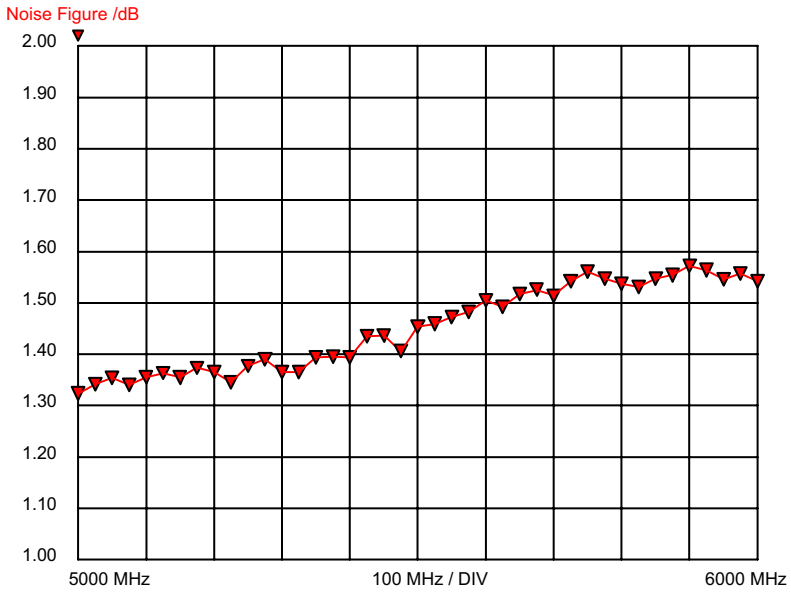
EUT Name:	Two Stage LNA mit BFP640
Manufacturer:	Infineon
Operating Conditions:	V=3.3V,I=15.9mA, T=25C
Operator Name:	Gerard Wevers
Test Specification:	5 - 6 GHz LNA
Comment:	LWR # SD 00020 LNA P 16 Nov 2002

Analyzer

RF Att:	0.00 dB	RBW :	1 MHz	Range:	30.00 dB
Ref Lvl:	-39.00 dBm	VBW :	100 Hz	Ref Lvl auto:	ON

Measurement

2nd stage corr: ON	Mode: Direct	ENR: HP346B



AN131_plot_nf.vsd

Figure 3 Noise Figure

Noise Figure, Tabular Data, Two-Stage

From Rohde & Schwarz SFEK3 + FSEB30
System Preamplifier = MITEQ AFS3-04000800-10-ULN

Table 3 Noise Figure

Frequency	Noise Figure
5000 MHz	1.32 dB
5025 MHz	1.34 dB
5050 MHz	1.35 dB
5075 MHz	1.34 dB
5100 MHz	1.36 dB
5125 MHz	1.36 dB
5150 MHz	1.36 dB
5175 MHz	1.37 dB
5200 MHz	1.37 dB
5225 MHz	1.35 dB
5250 MHz	1.38 dB
5275 MHz	1.39 dB
5300 MHz	1.37 dB
5325 MHz	1.37 dB
5350 MHz	1.39 dB
5375 MHz	1.40 dB
5400 MHz	1.39 dB
5425 MHz	1.44 dB
5450 MHz	1.44 dB
5475 MHz	1.41 dB
5500 MHz	1.45 dB
5525 MHz	1.46 dB
5550 MHz	1.47 dB
5575 MHz	1.48 dB
5600 MHz	1.50 dB
5625 MHz	1.49 dB
5650 MHz	1.52 dB
5675 MHz	1.53 dB
5700 MHz	1.51 dB
5725 MHz	1.54 dB
5750 MHz	0.56 dB
5775 MHz	1.55 dB
5800 MHz	1.54 dB
5825 MHz	1.53 dB
5850 MHz	1.55 dB
5875 MHz	1.55 dB
5900 MHz	1.57 dB

Table 3 Noise Figure (cont'd)

Frequency	Noise Figure
5925 MHz	1.56 dB
5950 MHz	1.55 dB
5975 MHz	1.56 dB
6000 MHz	1.54 dB

Scanned Image of PC Board, Two-Stage Cascade

By swinging a capacitor tacked to the output of Stage 1 down or to the right, the individual stages may be tested alone prior to integration. To test Stage 1 by itself, signal flow is from leftmost RF connector (input) to bottom RF connector [output]; to test Stage 2 alone, signal flow is from bottom RF connector [input] to rightmost RF connector [output]. The DC block between stages, C2, can be swung from output of Stage 1 down to lower RF connector to test Stage 1 alone; likewise C2 can be swung from track leading to lower RF connector up to right at a 45 degree angle to connect to input of Stage 2, to test Stage 2 alone.

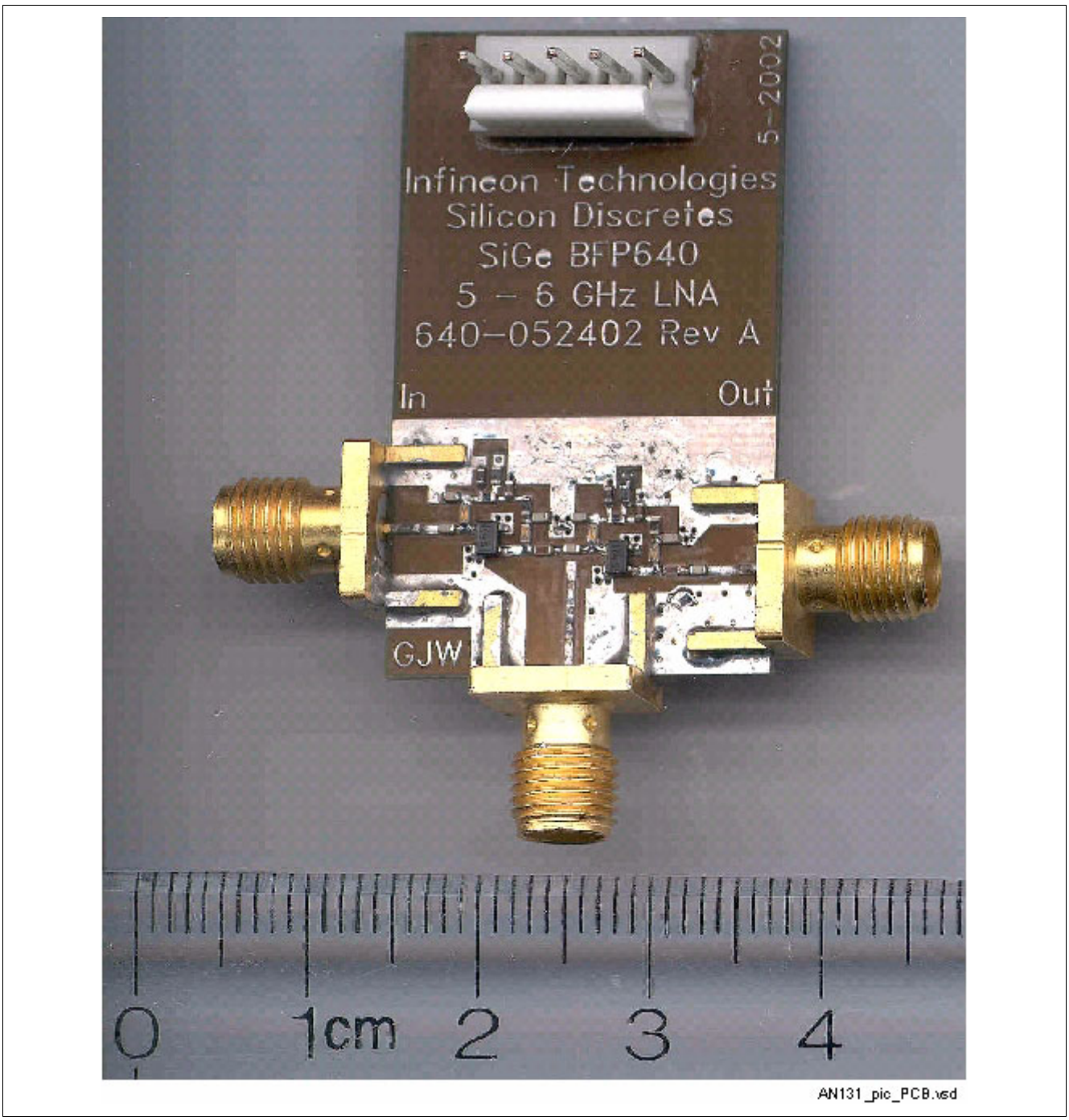


Figure 4 Image of PC Board

Scanned Image of PC Board, Two-Stage Cascade, Close-In Shot

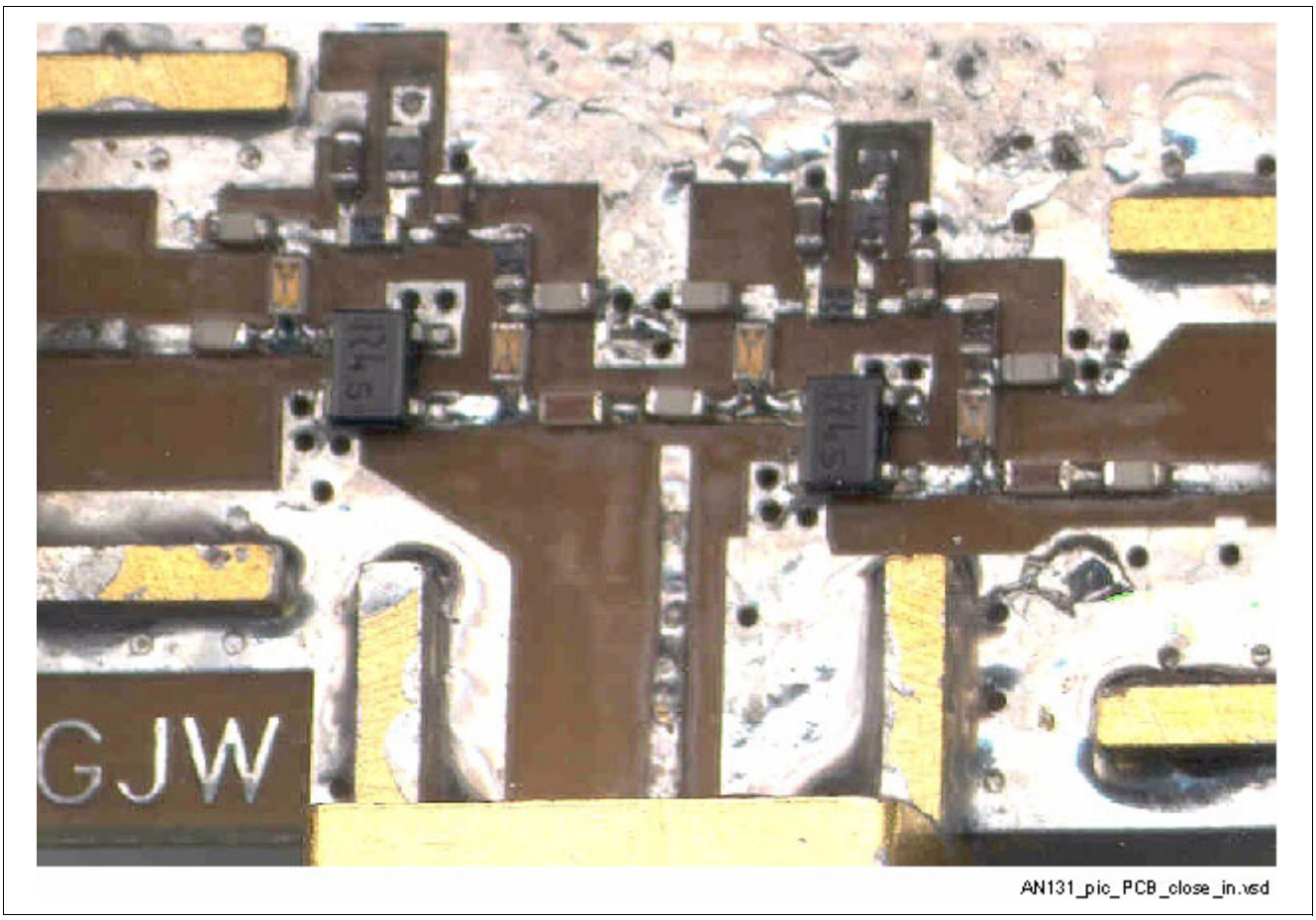


Figure 5 Image of PC Board, Close-In Shot

Power Sweep at 5350 MHz (CW)

Source Power (Input) swept from -25 to 0 dBm
Input P_{1dB} ≅ -15.7 dBm

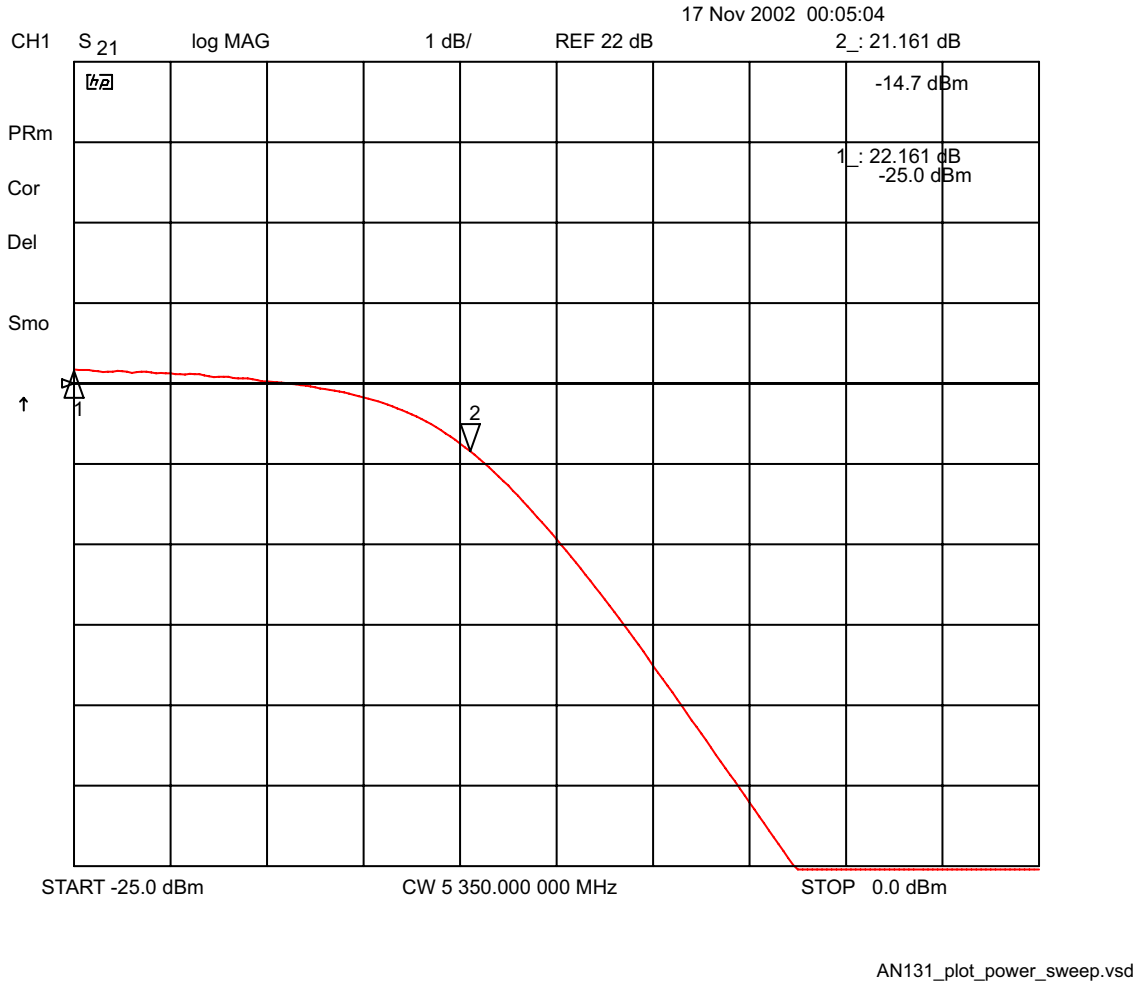


Figure 6 Plot of Power Sweep at 5350 MHz

Input Return Loss, Log Mag

Cascade, 2 Stages

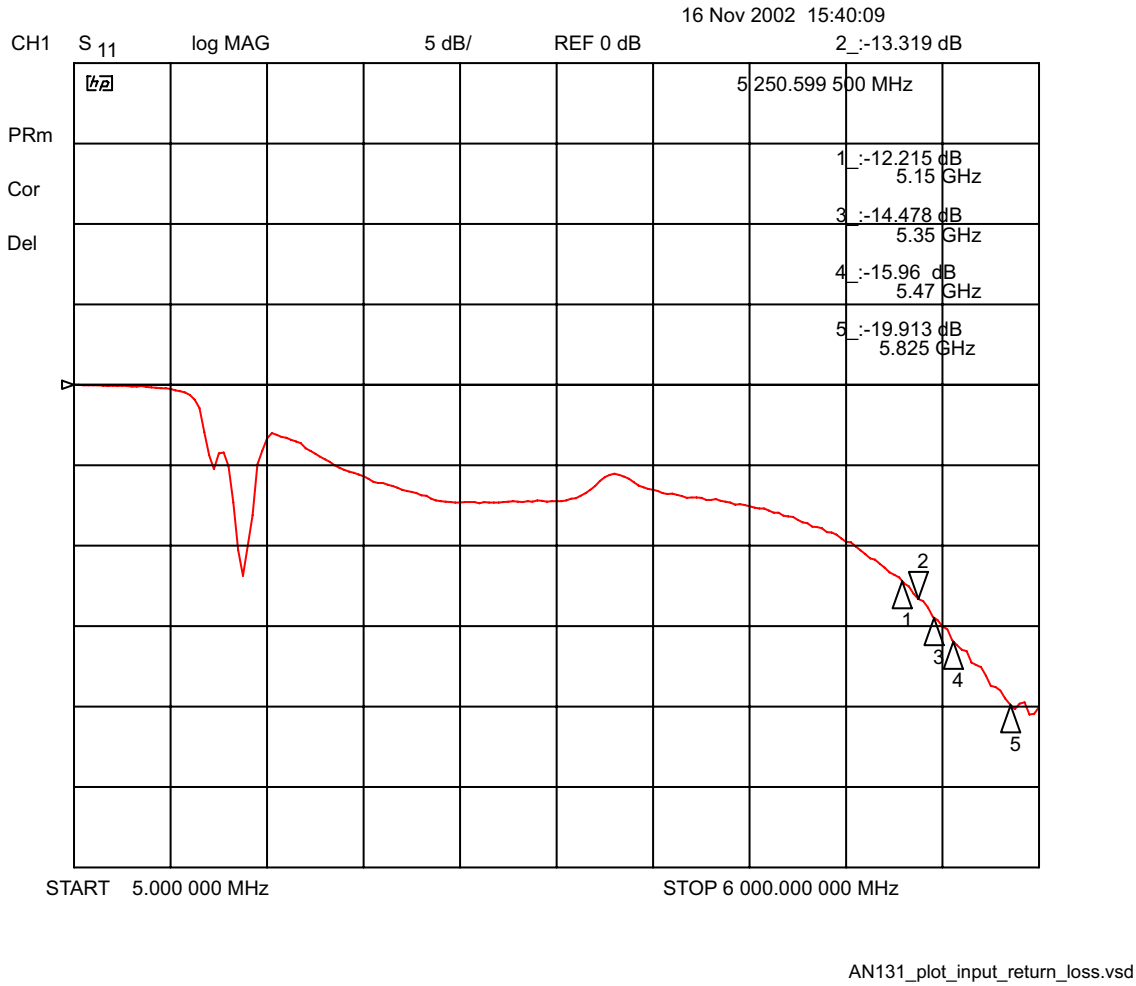


Figure 7 Plot of Input Return Loss

Input Return Loss, Smith Chart

Cascade, 2 Stages
Reference Plane = PCB Input SMA Connector

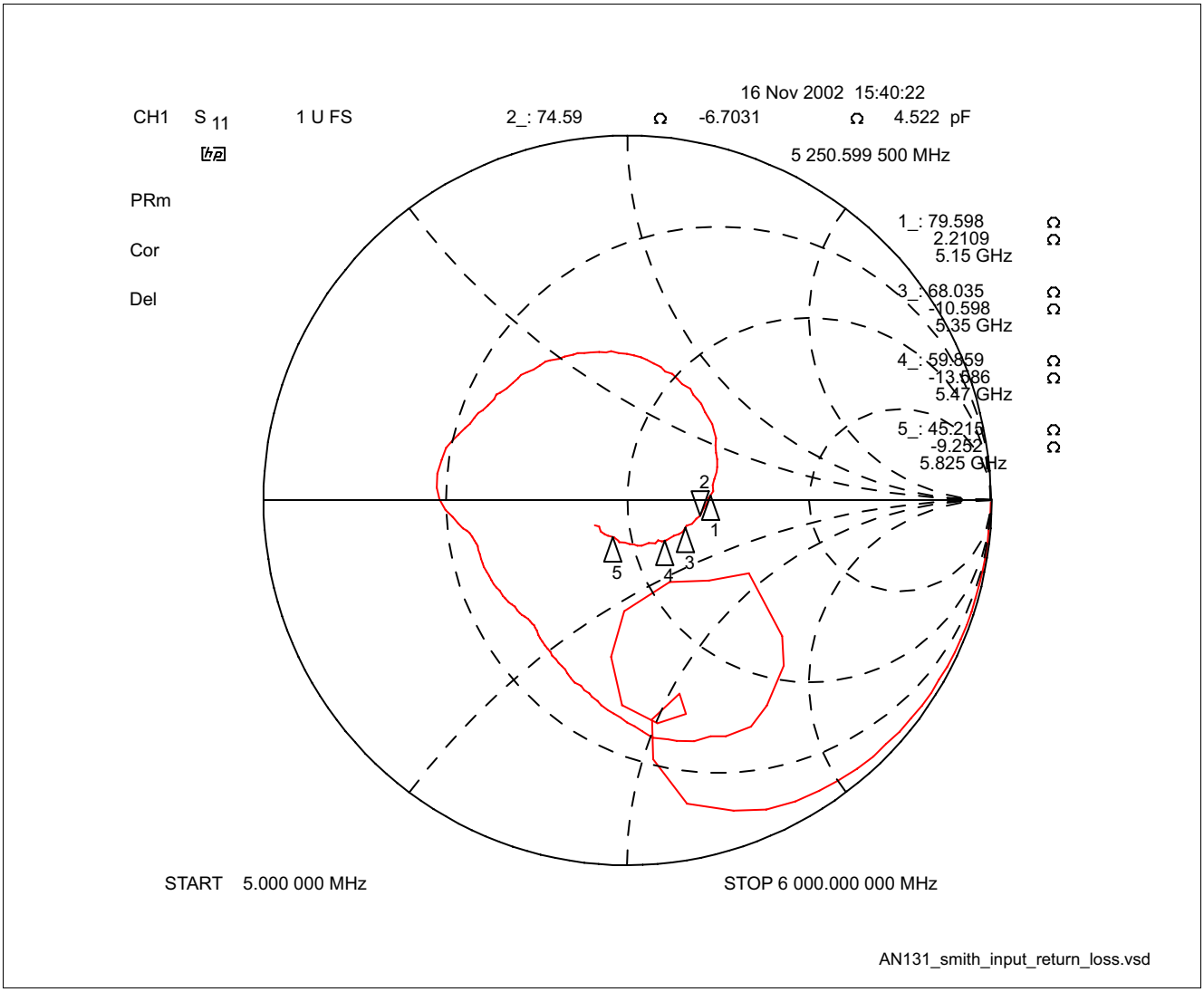


Figure 8 Smith Chart of Input Return Loss

Forward Gain

Cascade, 2 Stages

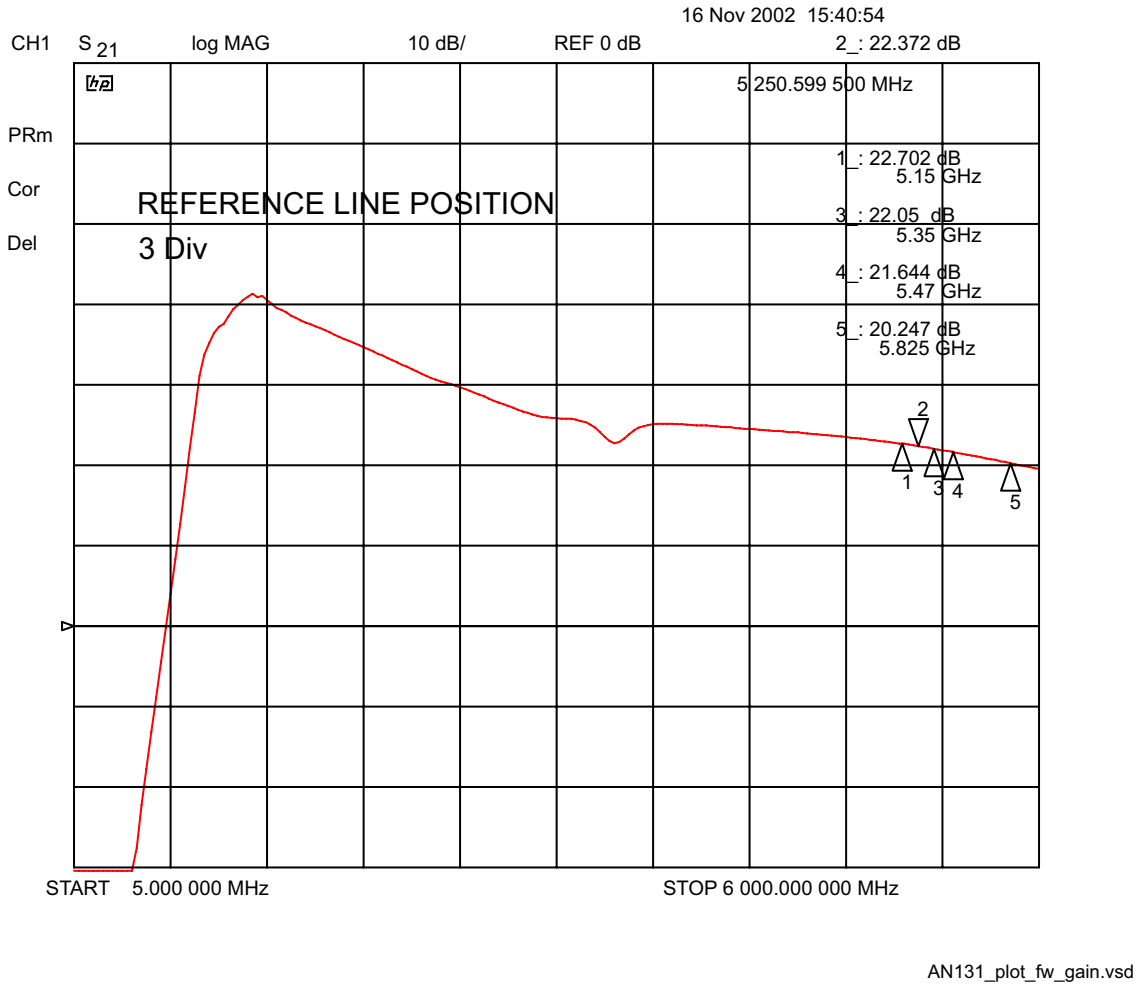


Figure 9 Plot of Forward Gain

Reverse Isolation

Cascade, 2 Stages

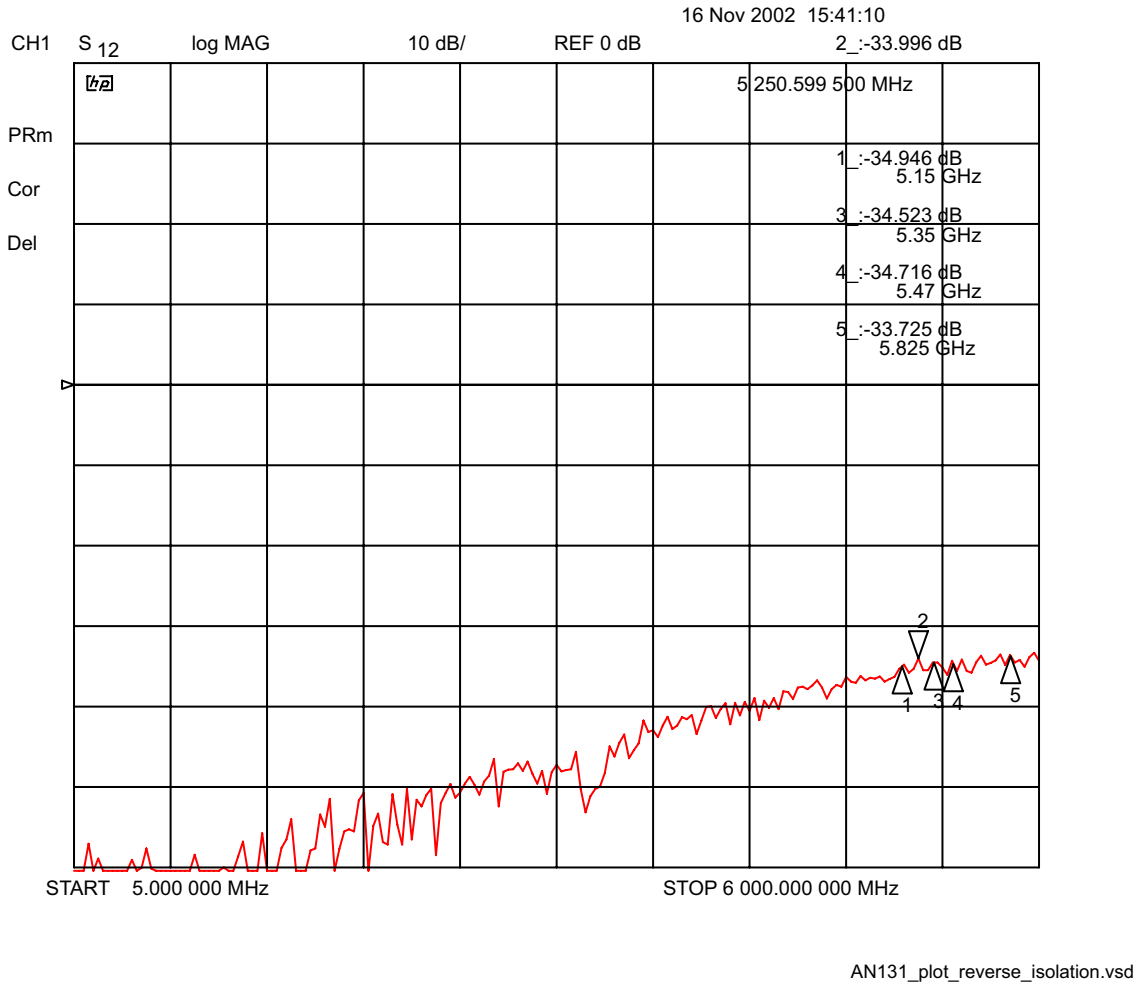


Figure 10 Plot of Reverse Isolation

Output Return Loss, Log Mag

Cascade, 2 Stages

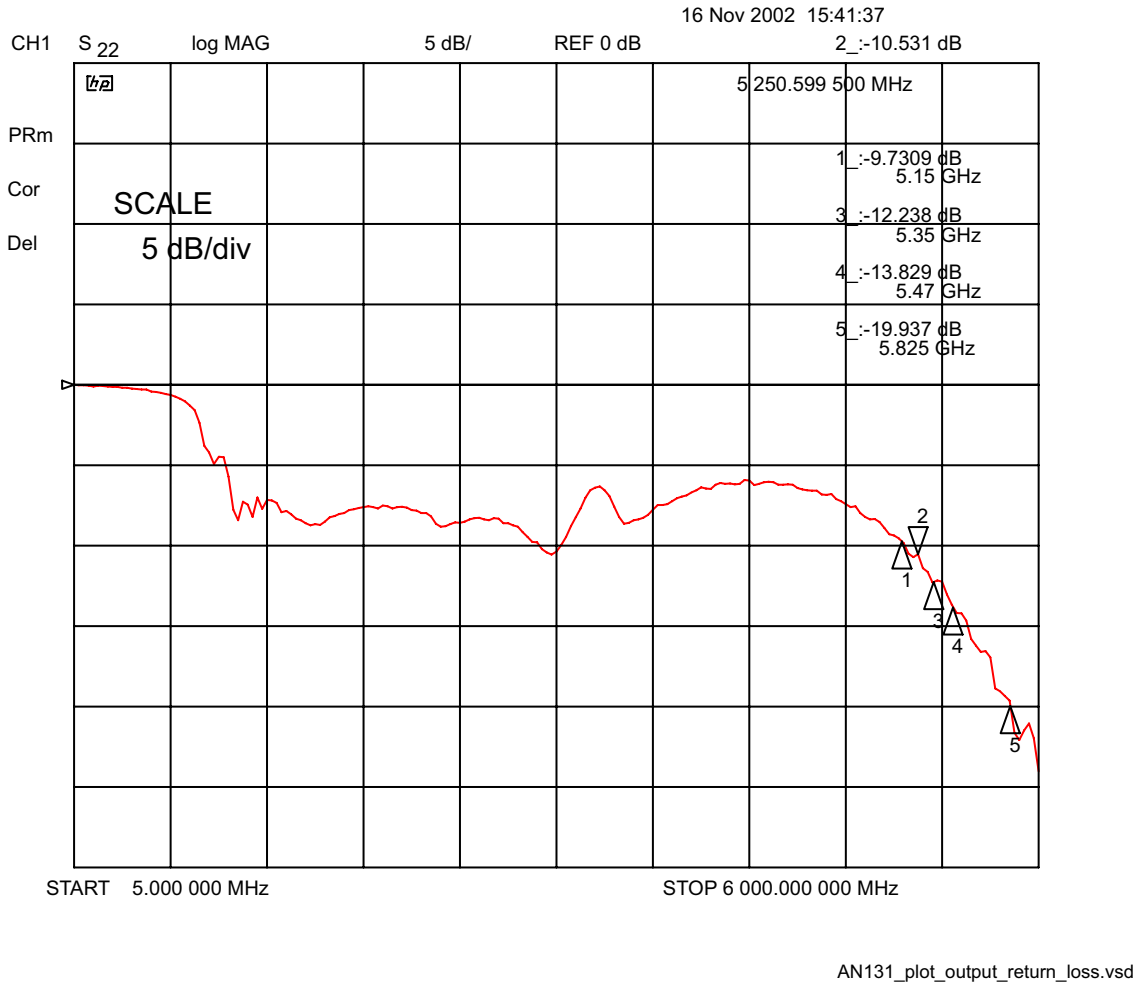


Figure 11 Plot of Output Return Loss

Output Return Loss, Smith Chart

Cascade, 2 Stages
Reference Plane = PCB Output SMA Connector

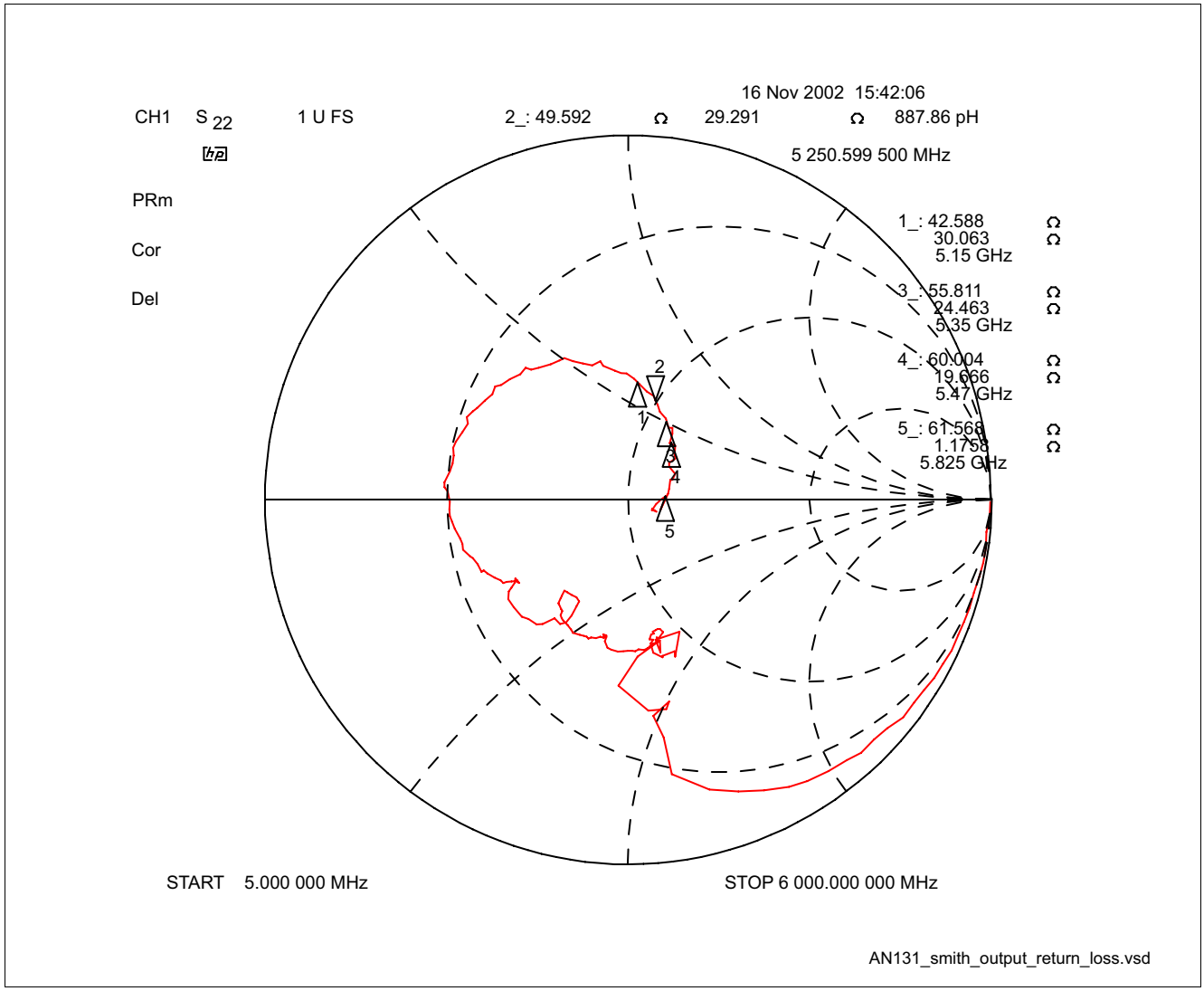


Figure 12 Smith Chart of Output Return Loss

Two-Tone Third Order Intercept Test, 5350 MHz

Input Stimulus for Two-Tone Third Order Intercept Test.
f_1 = 5349 MHz, f_2 = 5350 MHz, -23 dBm each tone.

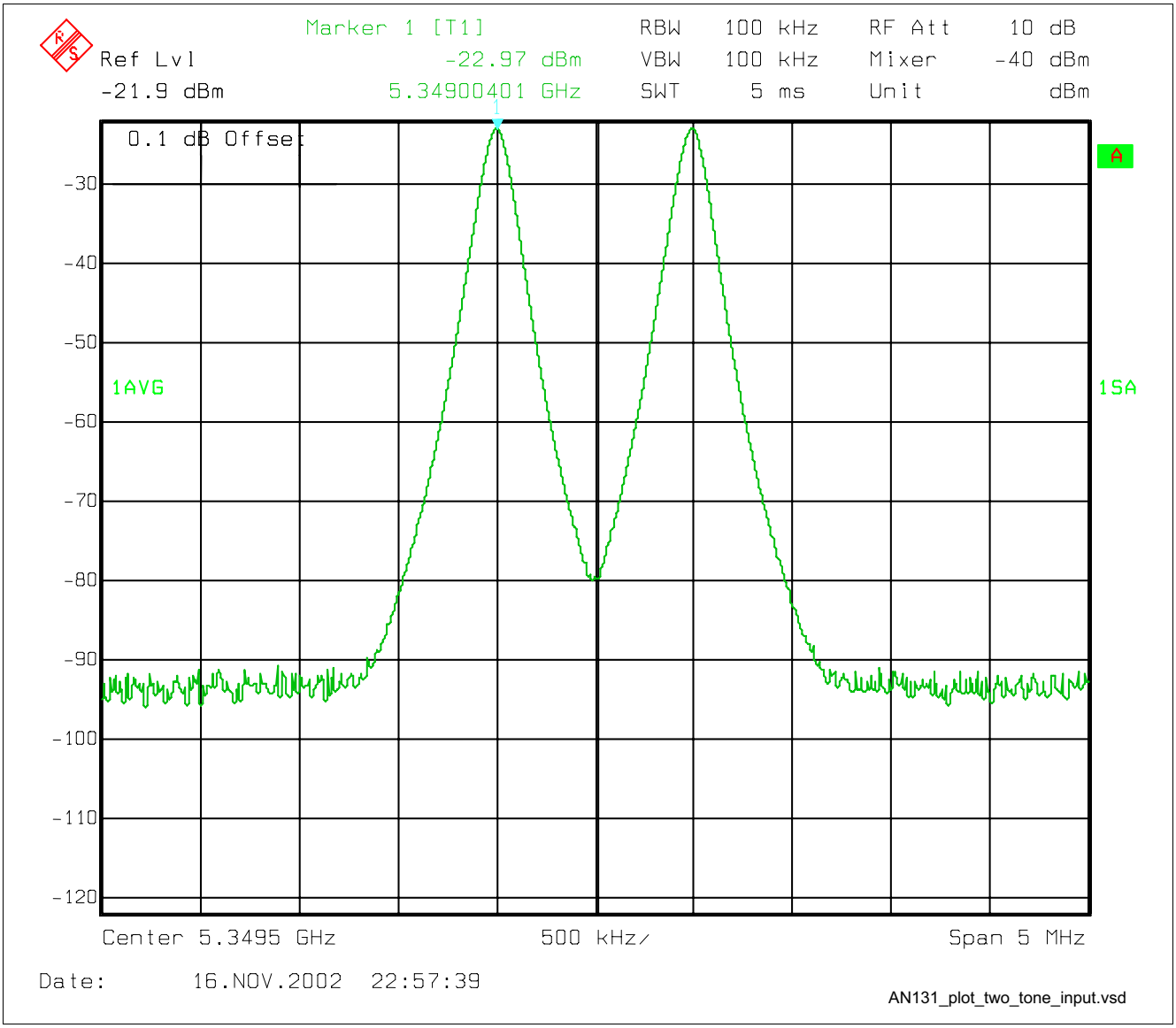


Figure 13 Tow-Tone Test, Input Stimulus @ 5350 MHz

Two-Tone Third Order Intercept Test, 5350 MHz

LNA Output Response to Two-Tone Test.
Input 3rd Order Intercept = -23 + (55.2 / 2) = +4.6 dBm

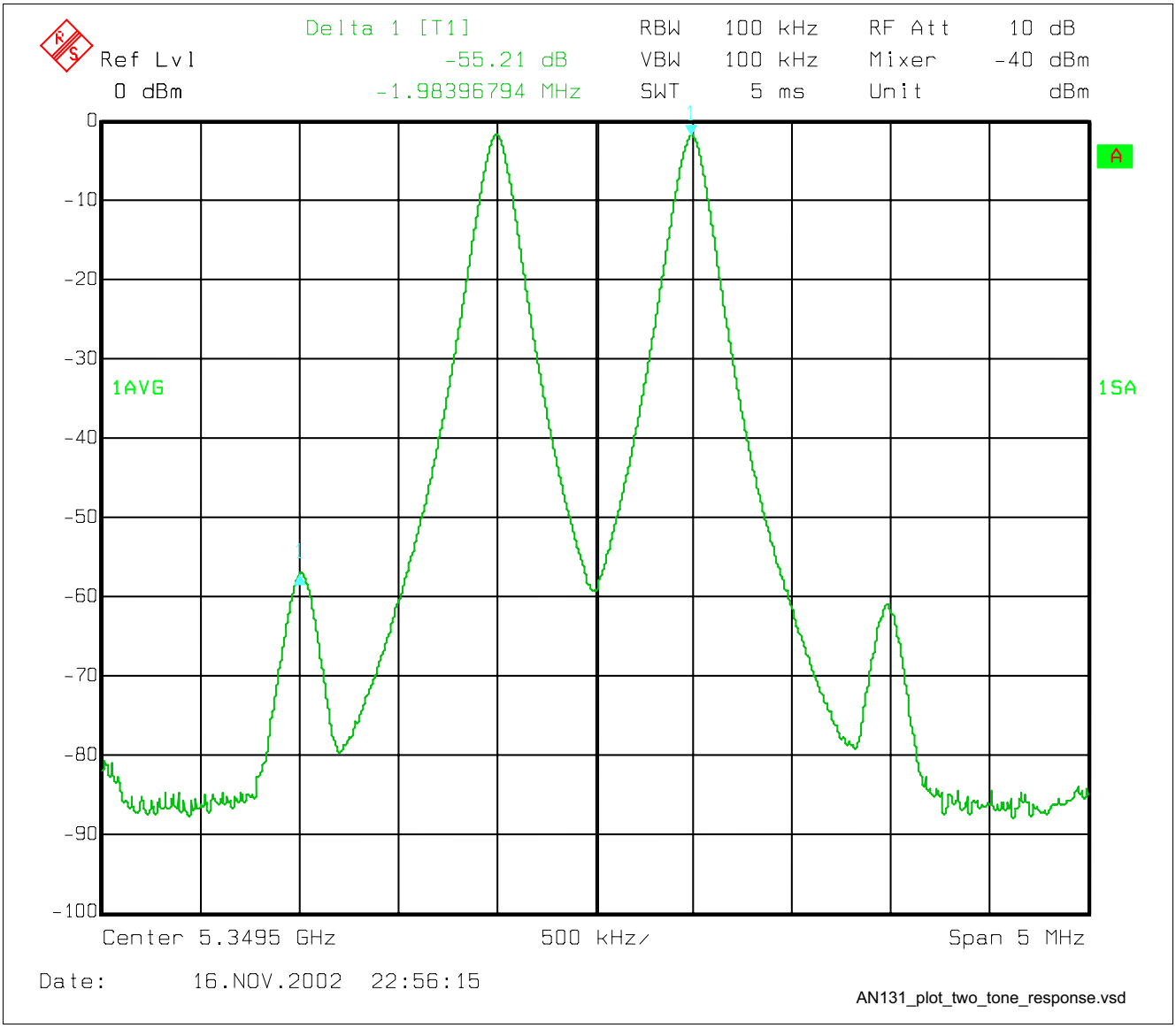


Figure 14 Tow-Tone Test, LNA Response @ 5350 MHz