

Application Note No. 126

BFP640F Low-Noise Silicon-Germanium Transistor as 5 -6 GHz Single-Stage Low Noise Amplifier (LNA), with reduced external component count and reduced gain at 2.4 GHz

RF & Protection Devices



Never stop thinking

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Application Note No. 126

Revision History: 2007-10-17, Rev. 1.2

Previous Version: 2005-04-14, Rev. 1.1

Page	Subjects (major changes since last revision)
All	Small changes in figure descriptions

BFP640F Low-Noise Silicon-Germanium Transistor as 5 -6 GHz Single-Stage

1 BFP640F Low-Noise Silicon-Germanium Transistor as 5 -6 GHz Single-Stage Low Noise Amplifier (LNA), with reduced external component count and reduced gain at 2.4 GHz

Overview

- The Silicon-Germanium BFP640F in TSFP-4 package is shown in a modified 5 - 6 GHz LNA circuit derived from the BFP640 application shown in Applications Note AN082 (attached). This modified circuit is targeted for WLAN module manufacturers and reduces external component count to the absolute minimum. Note some performance is sacrificed to achieve reduced component count, most notably third-order intercept performance. Please also note, an attempt was made to reduce out-of-band gain, specifically to reduce gain at 2.4 GHz per customer request.
- In order to preserve input & output impedance match with reduced component count, a "trick" was used: DC blocking capacitors had their values increased such that they are used above their "self-resonant frequency" (SRF). C1 changes from 1.5 to 5.6 pF, C2 changes from 1.5 to 12 pF. Doing this makes these capacitors show some slight net inductive reactance in the 5 GHz frequency range, as opposed to these capacitors either appearing as a straight "short" or a capacitive reactance. The chip capacitors can be modeled as a series R-L-C with the capacitor's self-inductance being on the order of 0.5 nH. By using the chip's self-inductance, one can tailor the reactance of the chip capacitor by selecting the appropriate value of capacitance, and the R-L-C combination can be made to have resonance above the frequency of interest (normal case) or below the frequency of interest (done here in this "Trick").

Table 1 Comparison of Component Count for Original and Modified Circuits, for Single LNA Stage

Component Type	Number in Original Circuit	Number in Modified Circuit (new)	Comments
Chip Capacitor	6	3	C3, C4, C6 eliminated
Chip Resistor	3	3	
Chip Inductor	3	1	L1, L3 eliminated

- 3 capacitors, 2 inductors have been eliminated, reducing external components from 12 pieces to 7 pieces. Please refer to schematic diagrams on page 4.
- Note gain at 2.4 GHz has been reduced from ≈ 15 dB to ≈ 8 dB (e.g. 7 dB gain reduction in 2.4 GHz range with this new, reduced parts count design).

Applications

- Wireless LAN (802.11a)
- Cordless Telephones (5.8 GHz)
- Other 5 -6 GHz systems

BFP640F Low-Noise Silicon-Germanium Transistor as 5 -6 GHz Single-Stage

Summary

Achieved $\cong 10$ dB gain, 1.3 dB Noise Figure over the 4900 - 6000 MHz band, drawing 8.9 mA @ 3 V. Input 3rd Order Intercept = +8.7 dBm. Output $P_{1dB} = +6.9$ dBm. Total external component count (L, C, R) has been reduced from 12 pieces to 7 pieces. Please note noise figure result does not extract PC board losses, if PCB loss were extracted, noise figure result would improve by approximately 0.2 - 0.3 dB (e.g. if loss is extracted, noise figure would be 1.1 to 1.3 dB).

Cross Sectional Diagram of PC Board

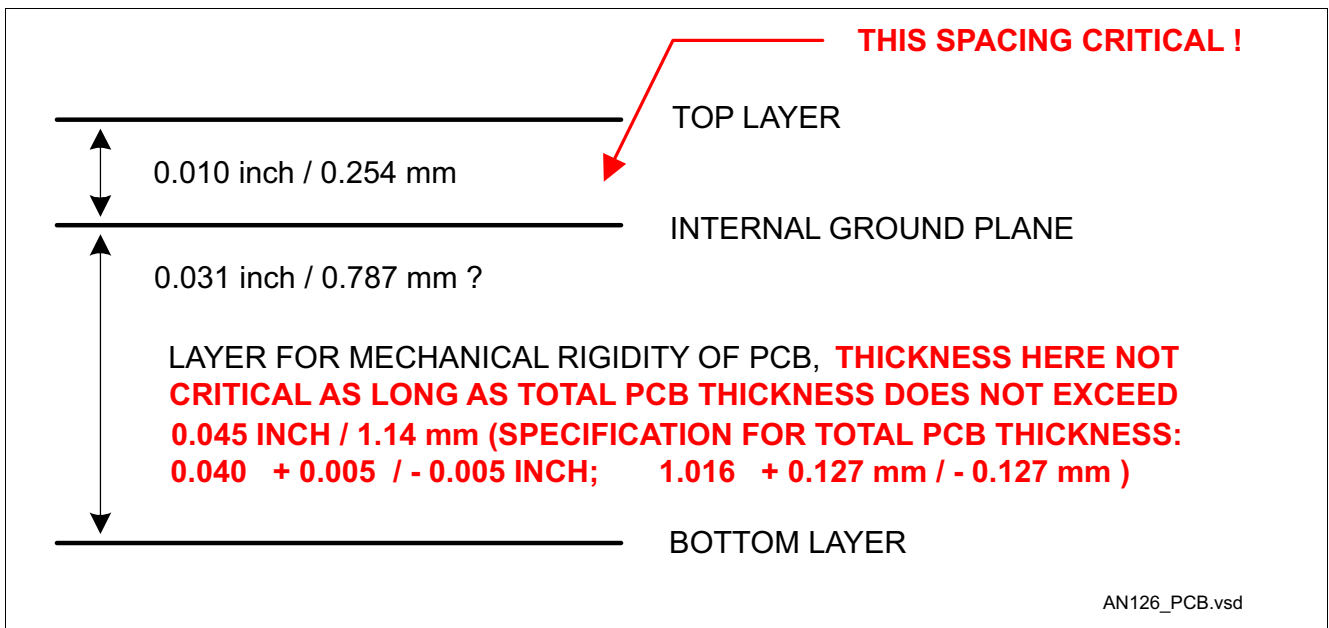


Figure 1 PCB - Cross Sectional Diagram

BFP640F Low-Noise Silicon-Germanium Transistor as 5 -6 GHz Single-Stage
Summary of Data

$T = 25\text{ }^{\circ}\text{C}$, network analyzer source power = -30 dBm

Table 2 Summary of Data

Parameter	Result	Comments
Frequency Range	Under 4.9 - 6 GHz	
DC Current	8.9 mA @ 3.0 V supply voltage ($V_{CE} = 2.7\text{ V}$)	Note power supply voltage is measured directly across PCB supply line and ground, to eliminate voltage drop across wire harness
Gain	11.0 dB @ 4900 MHz 10.1 dB @ 5500 MHz 9.7 dB @ 6000 MHz	Gain at 5150 MHz = 10.7 dB
Noise Figure	1.3 dB @ 4900 MHz 1.4 dB @ 5500 MHz 1.5 dB @ 6000 MHz	These values do NOT extract PCB losses, etc. resulting from FR4 board and passives used on PCB - these results are at input SMA connector
Input P_{1dB}	-2.2 dBm @ 5500 MHz	
Output P_{1dB}	+6.9 dBm @ 5500 MHz	
Input 3 rd Order Intercept	+8.7 dBm @ 5150 MHz	Figure 16 and Figure 17 . IP_3 could be improved by 6 to 10 dB by putting L1 and C3 back into the circuit.
Output 3 rd Order Intercept	+19.4 dBm @ 5150 MHz	
Input Return Loss	9.3 dB @ 4900 MHz 11.6 dB @ 5500 MHz 14.0 dB @ 6000 MHz	
Output Return Loss	10.4 dB @ 4900 MHz 11.9 dB @ 5500 MHz 12.7 dB @ 6000 MHz	
Reverse Isolation	17.7 dB @ 4900 MHz 16.4 dB @ 5500 MHz 15.5 dB @ 6000 MHz	

BFP640F Low-Noise Silicon-Germanium Transistor as 5 -6 GHz Single-Stage

Schematic Diagram, Original Circuit

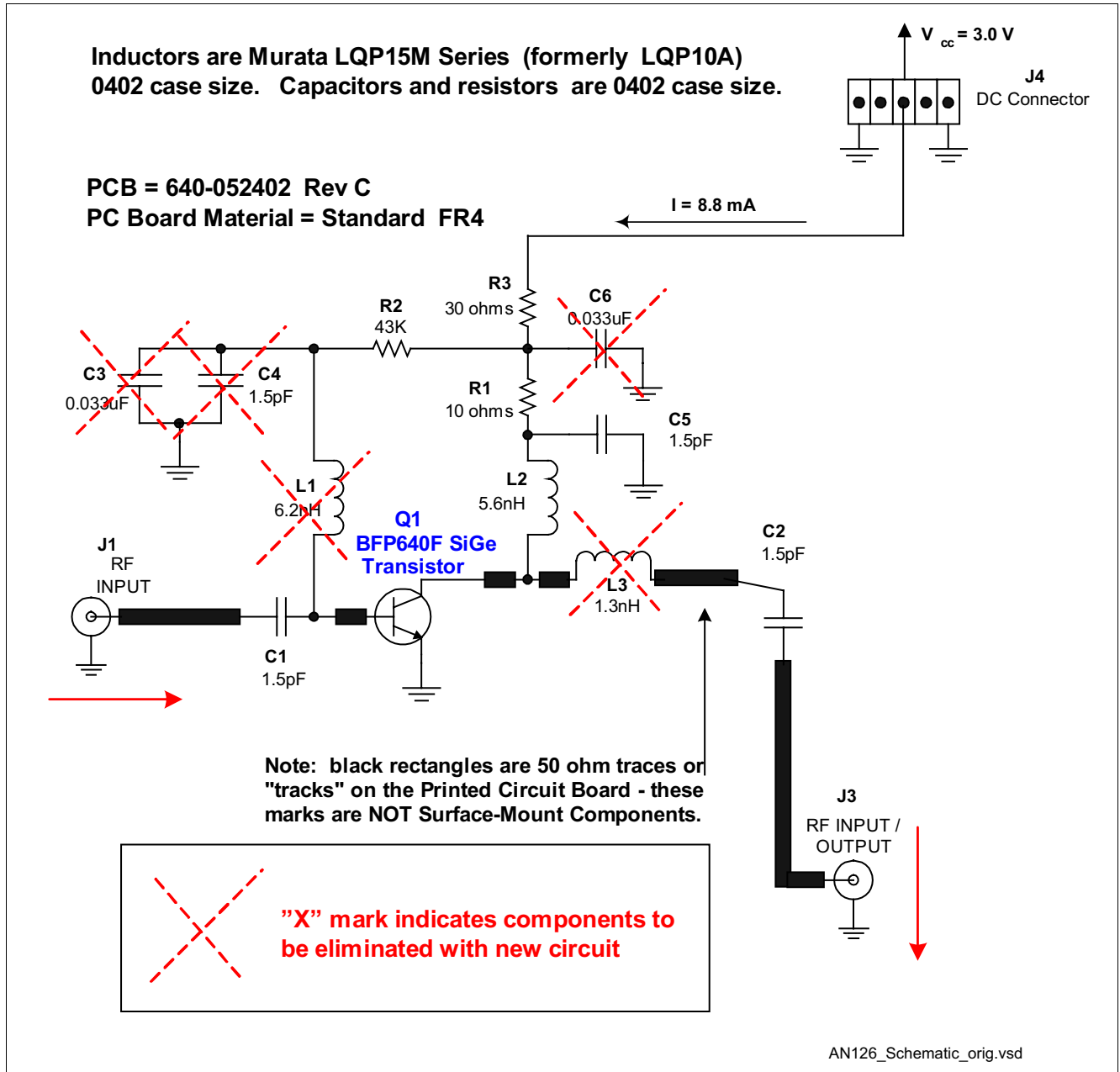


Figure 2 Schematic Diagram

BFP640F Low-Noise Silicon-Germanium Transistor as 5 -6 GHz Single-Stage

Schematic Diagram, NEW Circuit with Reduced Parts Count

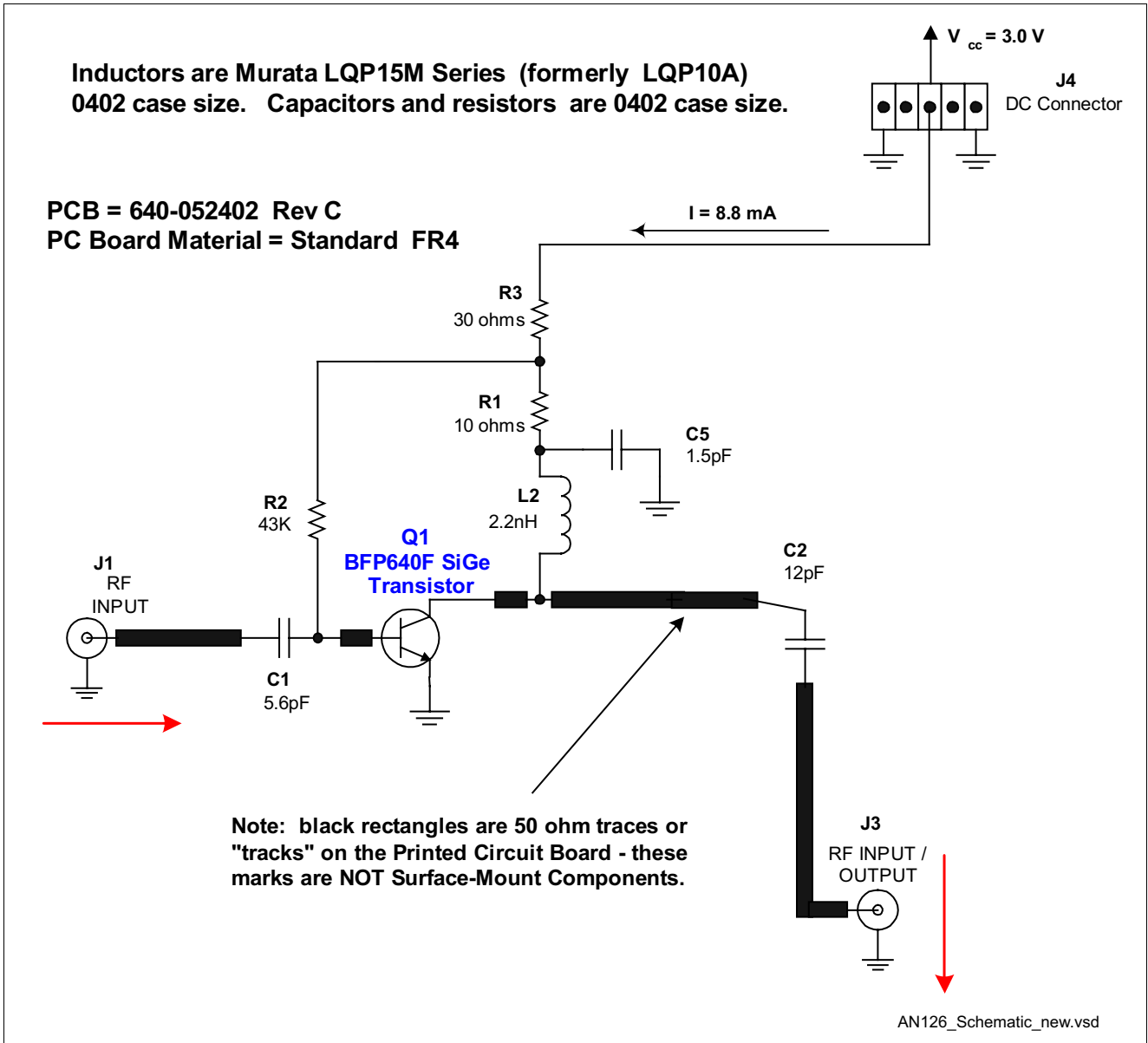


Figure 3 Schematic Diagram

BFP640F Low-Noise Silicon-Germanium Transistor as 5 -6 GHz Single-Stage

Details on TSFP-4 Package (“Thin Small Flat Pack”). Dimensions in millimeters (mm).

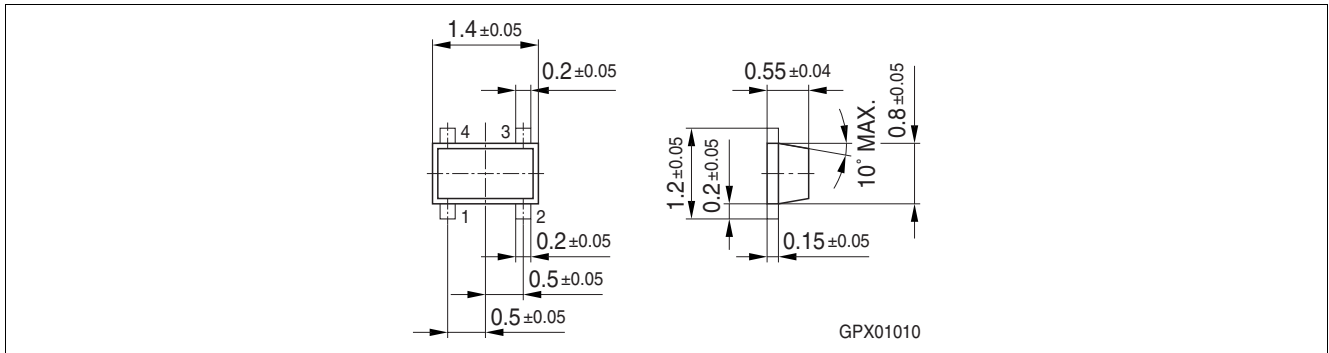


Figure 4 Package Details of TSFP-4

Recommended Soldering Footprint for TSFP-4 (dimensions in millimeters).

Device package is to be oriented as shown in above drawing (e.g. orient long package dimension horizontally on this footprint).

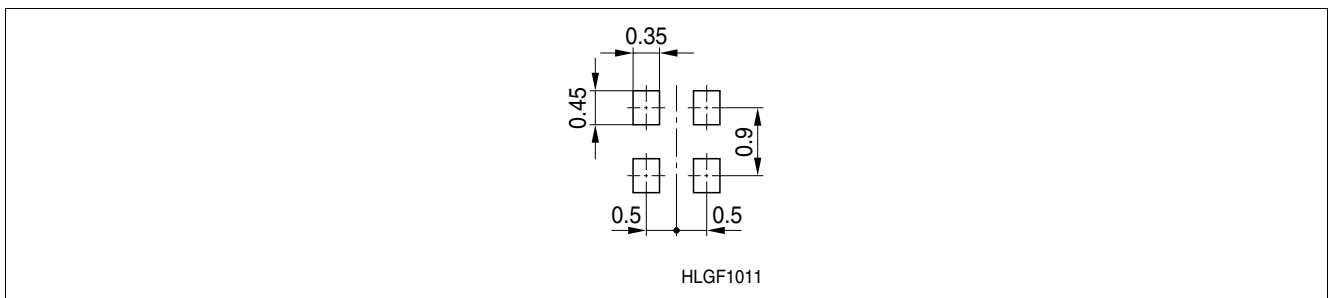


Figure 5 Package Footprint of TSFP-4

BFP640F Low-Noise Silicon-Germanium Transistor as 5 -6 GHz Single-Stage

Noise Figure, Plot, 4.5 GHz to 6.5 GHz. Center of Plot (x-axis) is 5.5 GHz.

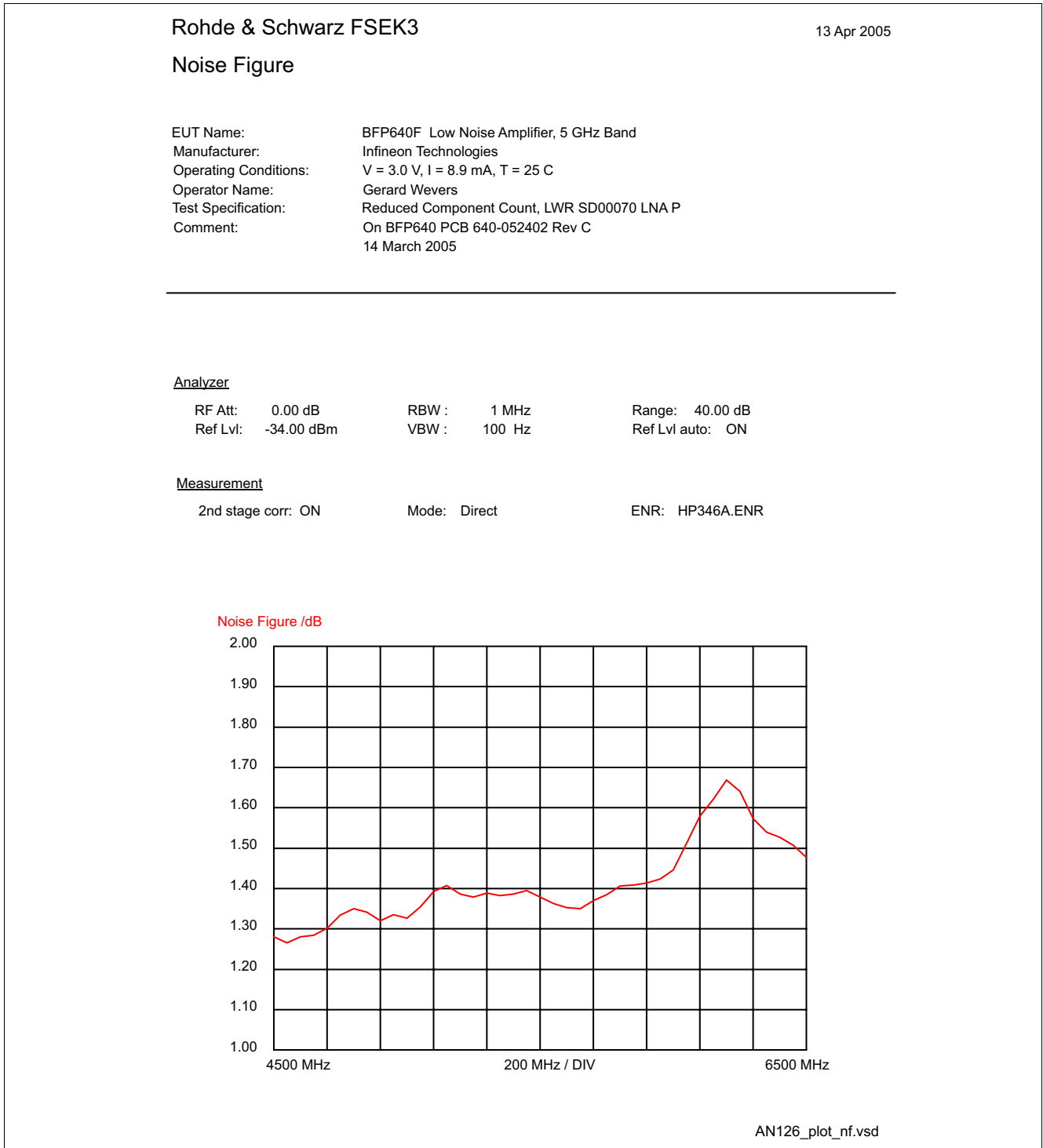


Figure 6 Noise Figure

BFP640F Low-Noise Silicon-Germanium Transistor as 5 -6 GHz Single-Stage

Noise Figure, Tabular Data

From Rhode & Schwarz FSEK3 + FSEM30 + System PreAmp

Table 3 Noise Figure

Frequency	Noise Figure
4500 MHz	1.17 dB
4550 MHz	1.27 dB
4600 MHz	1.27 dB
4650 MHz	1.29 dB
4700 MHz	1.29 dB
4750 MHz	1.28 dB
4800 MHz	1.28 dB
4850 MHz	1.30 dB
4900 MHz	1.31 dB
4950 MHz	1.32 dB
5000 MHz	1.32 dB
5050 MHz	1.35 dB
5100 MHz	1.37 dB
5150 MHz	1.35 dB
5200 MHz	1.39 dB
5250 MHz	1.40 dB
5300 MHz	1.39 dB
5350 MHz	1.35 dB
5400 MHz	1.35 dB
5450 MHz	1.37 dB
5500 MHz	1.37 dB
5550 MHz	1.33 dB
5600 MHz	1.32 dB
5650 MHz	1.34 dB
5700 MHz	1.34 dB
5750 MHz	1.34 dB
5800 MHz	1.38 dB
5850 MHz	1.38 dB
5900 MHz	1.39 dB
5950 MHz	1.43 dB
6000 MHz	1.45 dB
6050 MHz	1.49 dB
6100 MHz	1.56 dB
6150 MHz	1.63 dB
6200 MHz	1.69 dB
6250 MHz	1.61 dB
6300 MHz	1.56 dB
6350 MHz	1.51 dB

BFP640F Low-Noise Silicon-Germanium Transistor as 5 -6 GHz Single-Stage**Table 3** Noise Figure (cont'd)

Frequency	Noise Figure
6400 MHz	1.48 dB
6450 MHz	1.46 dB
6500 MHz	1.47 dB

BFP640F Low-Noise Silicon-Germanium Transistor as 5 -6 GHz Single-Stage

Scanned Image of PC Board

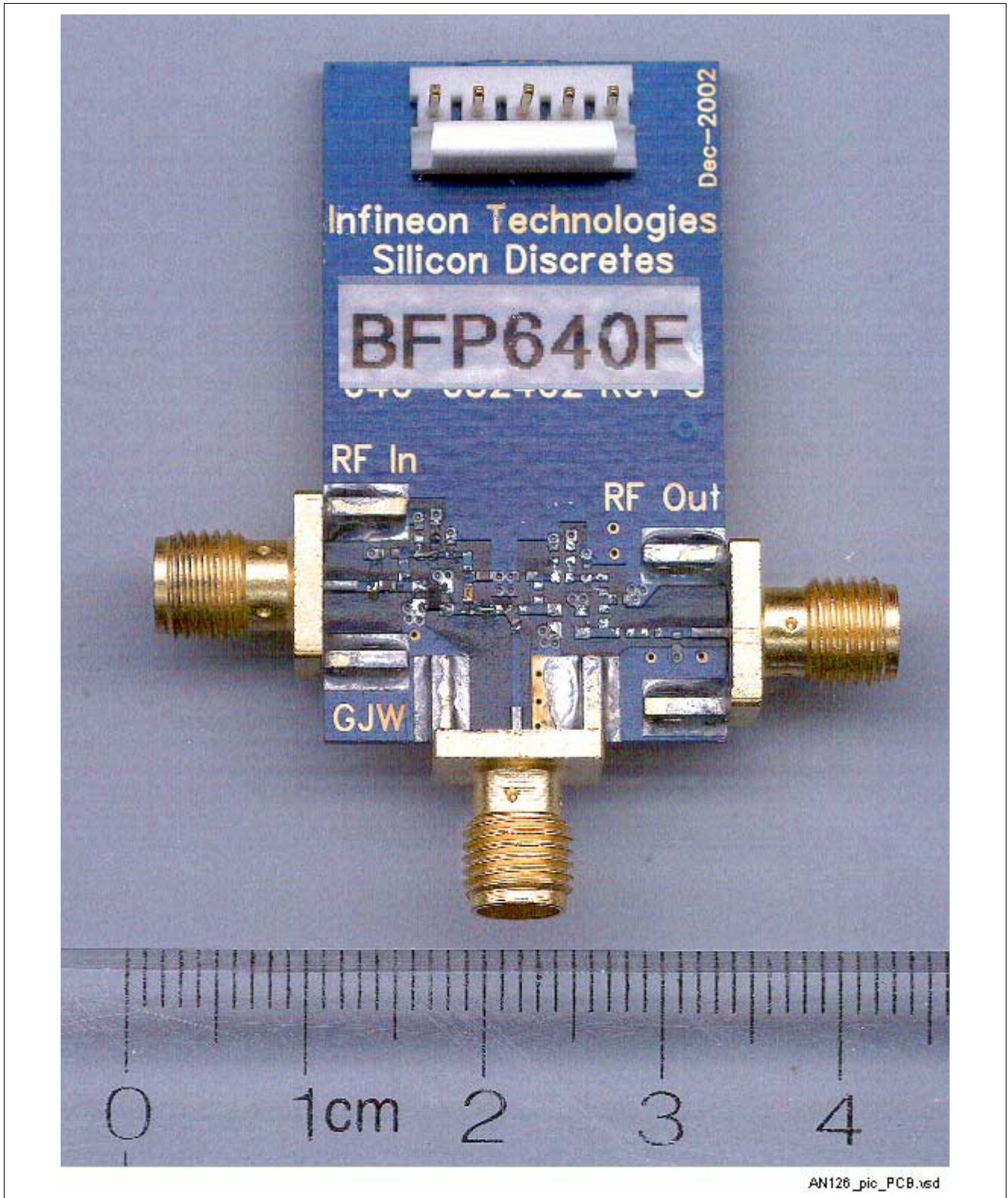


Figure 7 Image of PC Board

BFP640F Low-Noise Silicon-Germanium Transistor as 5 -6 GHz Single-Stage

Scanned Image of PC Board, Close-In Shot

Total PCB area used $\cong 40 \text{ mm}^2$

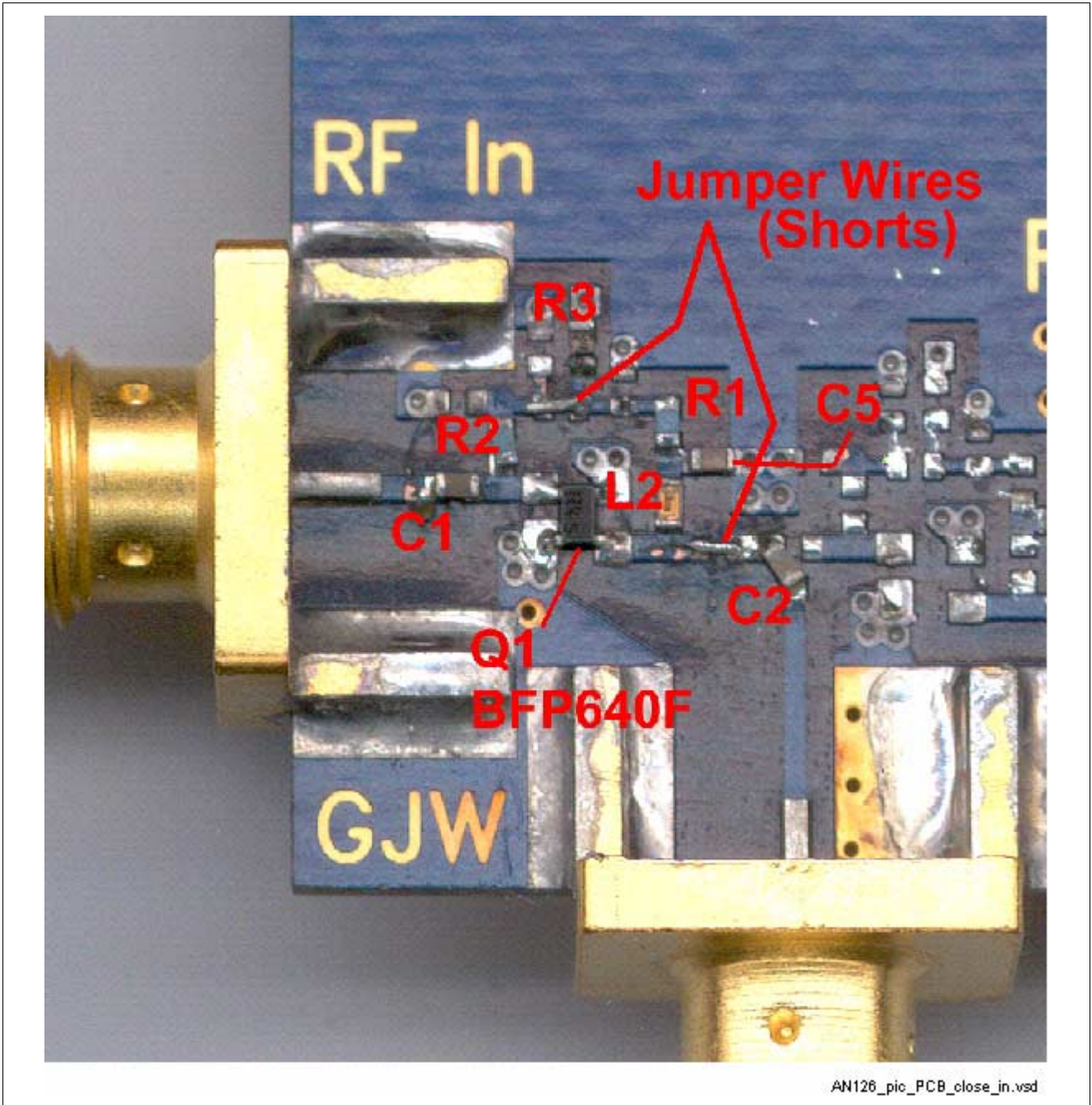


Figure 8 Image of PC Board, Close-In Shot

BFP640F Low-Noise Silicon-Germanium Transistor as 5-6 GHz Single-Stage

Stability

Rohde and Schwarz ZVC Network Analyzer calculates and plots Stability Factor "K" in real time, from 5 MHz to 8 GHz. Note $K > 1$ over entire range except at ≈ 260 MHz. Further work is needed to bring $K > 1$ here. Suggest varying / tuning value of resistor R1 to improve K in 260 MHz range, or putting capacitor C6 back into the circuit, in order to improve "K" at low frequencies.

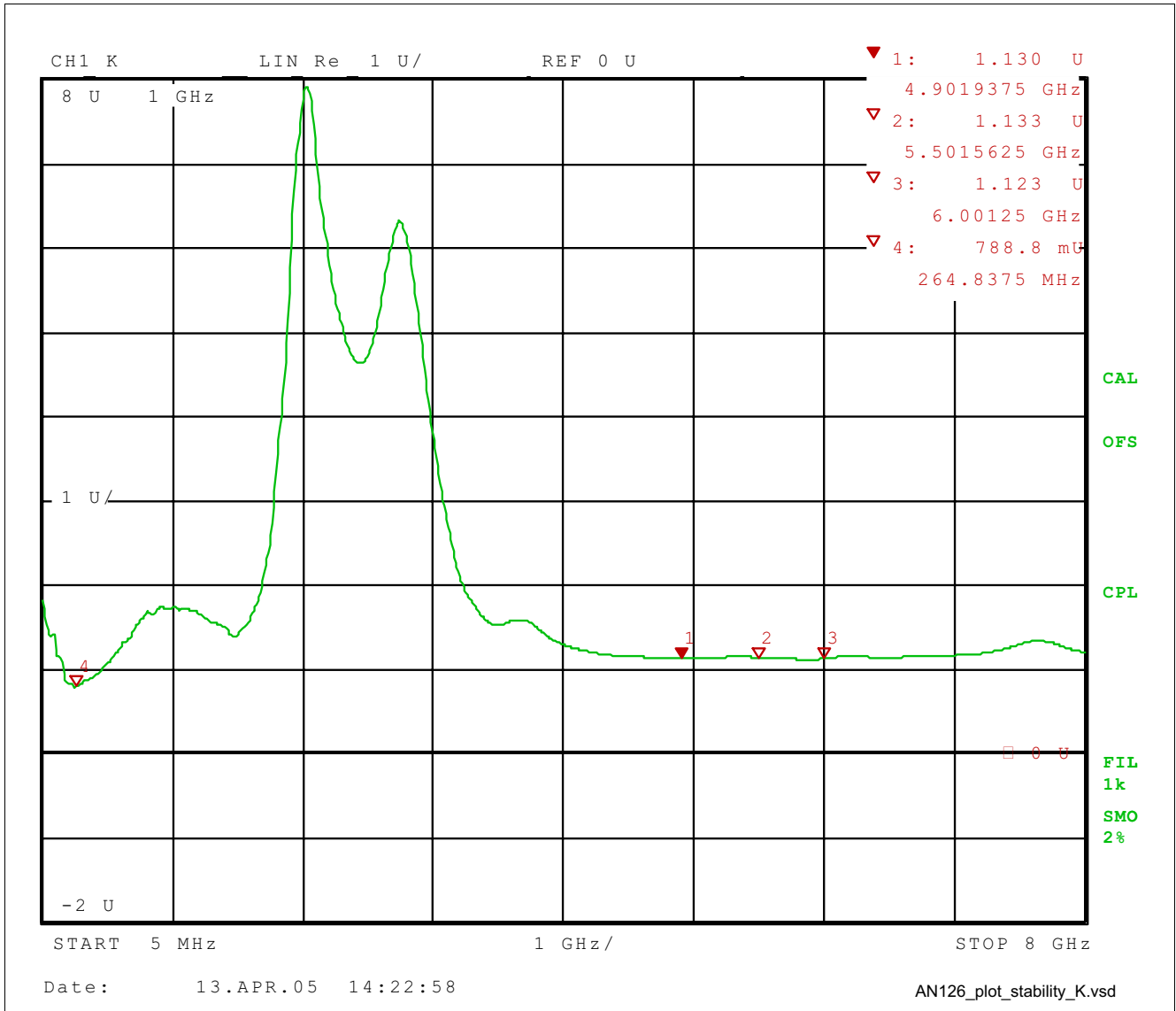


Figure 9 Plot of K(f)

 BFP640F Low-Noise Silicon-Germanium Transistor as 5 -6 GHz Single-Stage

Gain Compression at 5500 MHz

Amplifier is checked for 1 dB compression point at $V_{CC} = 3.0$ V, $I_C = 8.9$ mA (with $V_{CE} = 2.7$ V). An Agilent power meter was used to ensure accurate power levels are measured (as opposed to using Vector Network Analyzer in "Power Sweep" mode).

Input $P_{1dB} \cong -2.2$ dBm

Output $P_{1dB} \cong -2.2$ dBm + (Gain - 1 dB) = -2.2 dBm + (10.1 - 1) dB = +6.9 dBm

Table 4 Gain Compression

P_{in} , dBm	P_{out} , dBm	Gain
-11.0	-0.9	10.1
-10.0	+0.1	10.1
-9.0	+1.0	10.0
-8.0	+2.0	10.0
-7.0	+2.9	9.9
-6.0	+3.8	9.8
-5.0	+4.7	9.7
-4.0	+5.6	9.6
-3.0	+6.4	9.4
-2.0	+7.0	9.0
-1.0	+7.6	8.6
0.0	+8.1	8.1

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PLEASE NOTE - all plots are taken from Rohde And Schwarz ZVC Network Analyzer

Input Return Loss, Log Mag

5 MHz to 8 GHz Sweep

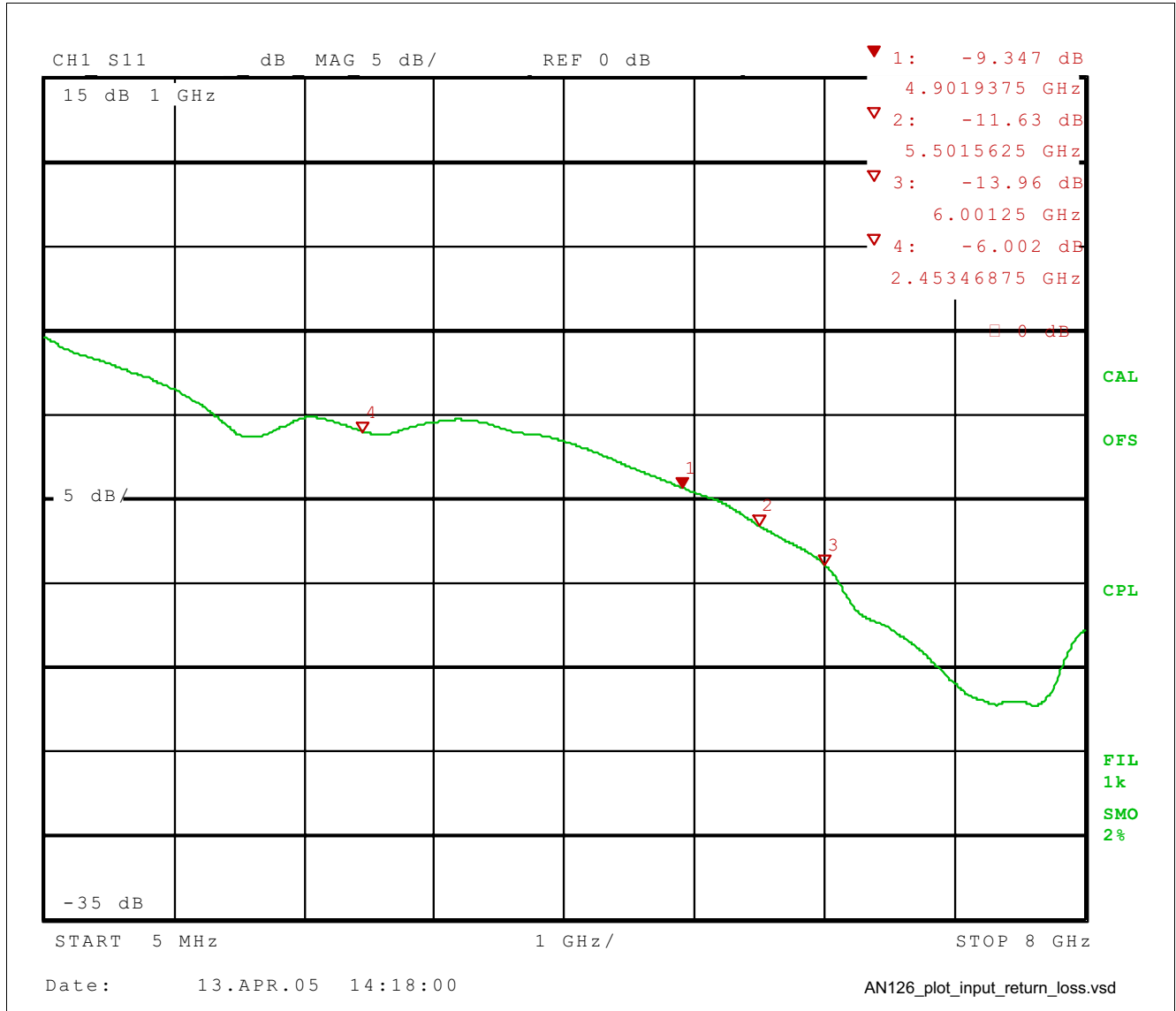


Figure 10 Plot of Input Return Loss

BFP640F Low-Noise Silicon-Germanium Transistor as 5 -6 GHz Single-Stage

Input Return Loss, Smith Chart

Reference Plane = Input SMA Connector on PC Board
 5 MHz to 8 GHz Sweep

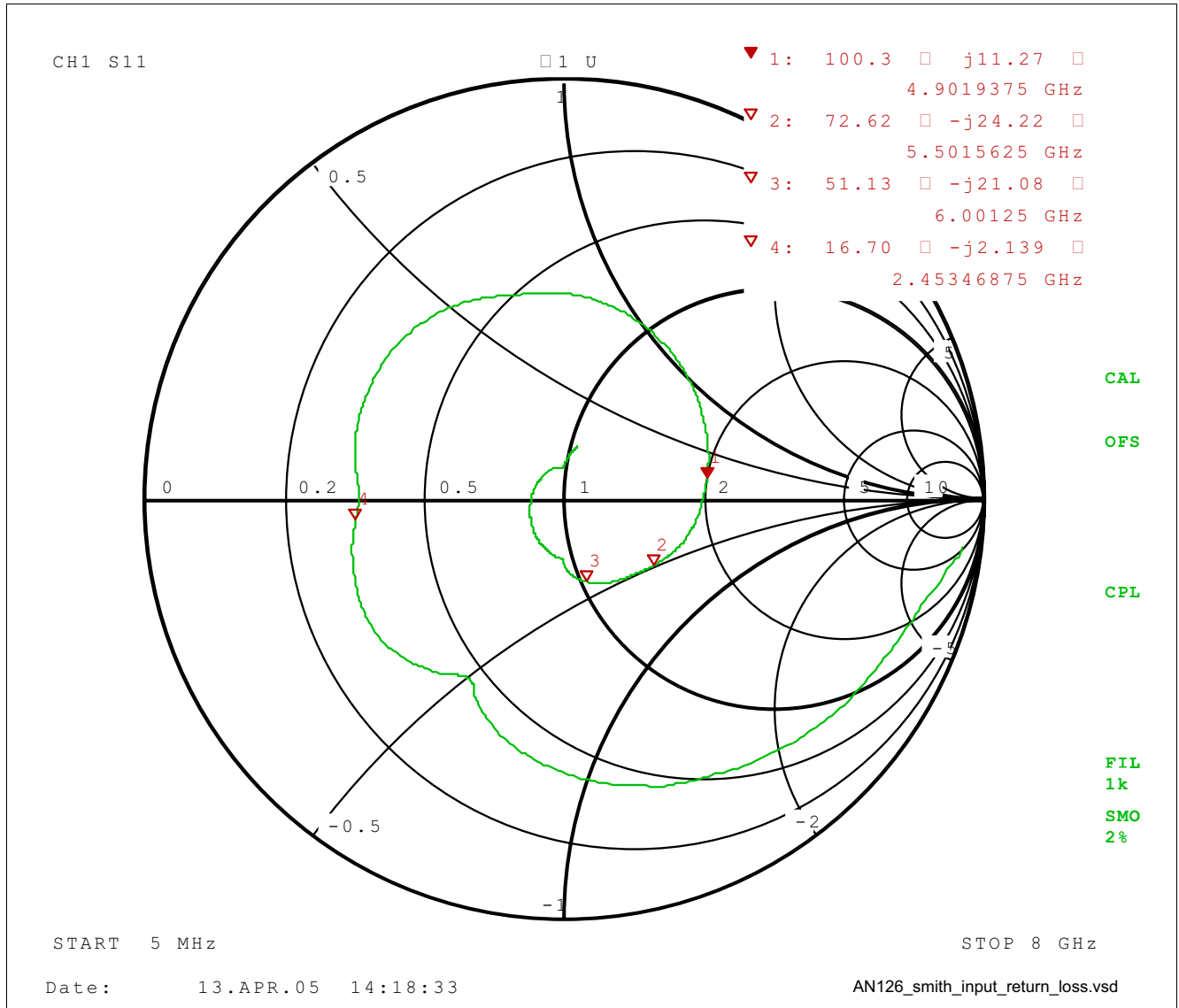


Figure 11 Smith Chart of Input Return Loss

BFP640F Low-Noise Silicon-Germanium Transistor as 5 -6 GHz Single-Stage

Forward Gain

5 MHz to 8 GHz Sweep

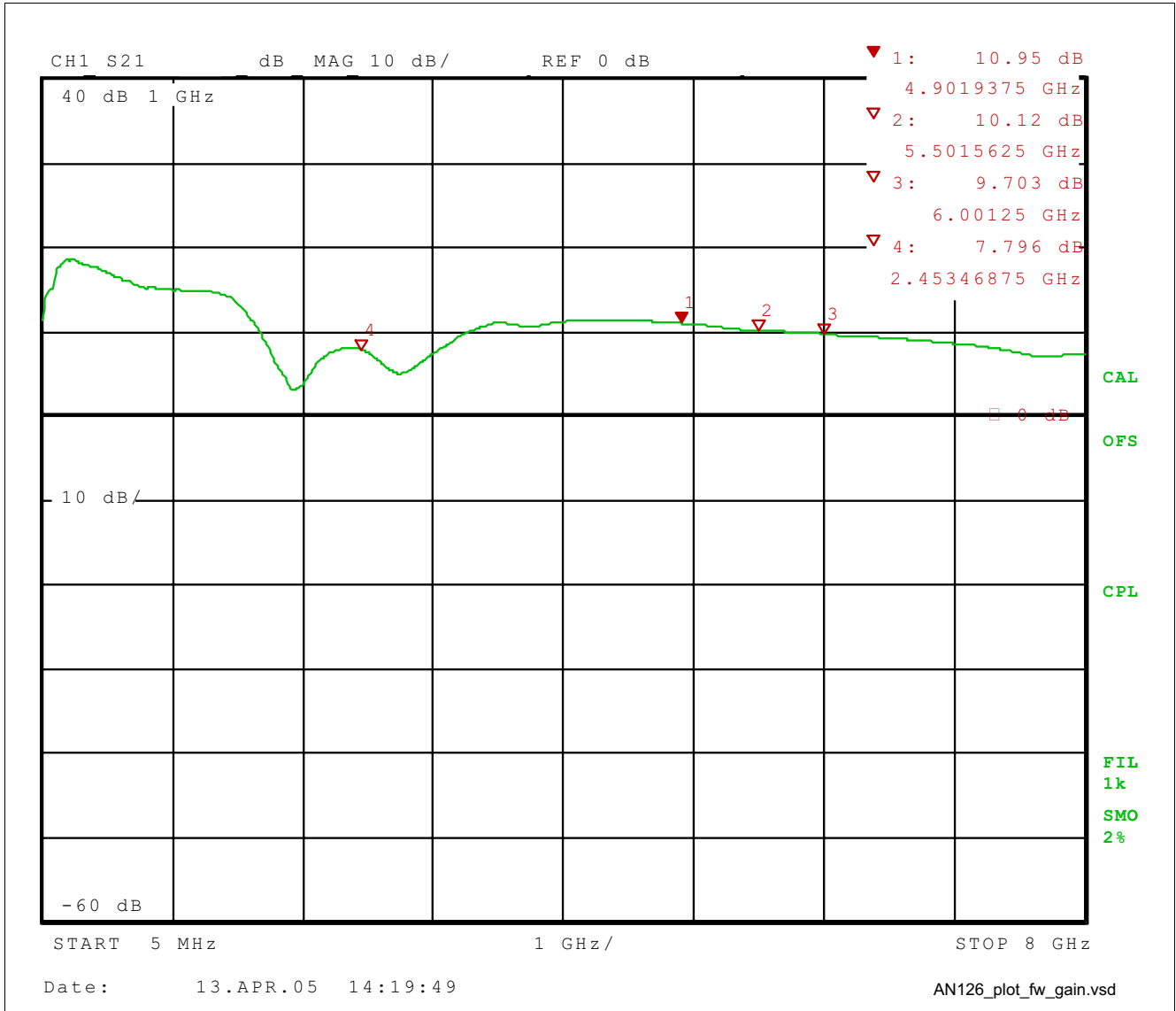


Figure 12 Plot of Forward Gain

BFP640F Low-Noise Silicon-Germanium Transistor as 5 -6 GHz Single-Stage

Reverse Isolation
5 MHz to 8 GHz Sweep

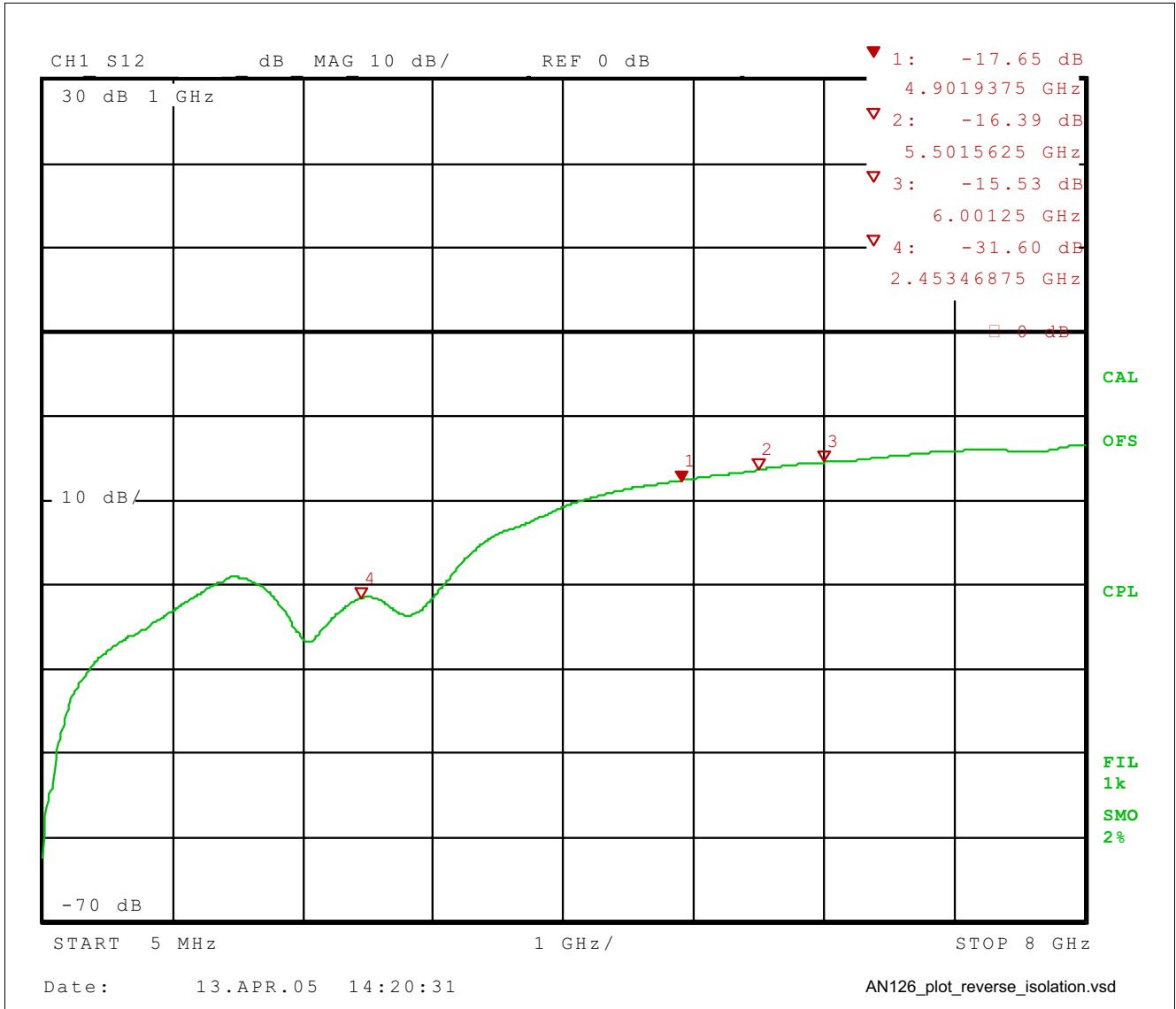


Figure 13 Plot of Reverse Isolation

BFP640F Low-Noise Silicon-Germanium Transistor as 5 -6 GHz Single-Stage

Output Return Loss, Log Mag

5 MHz to 8 GHz Sweep

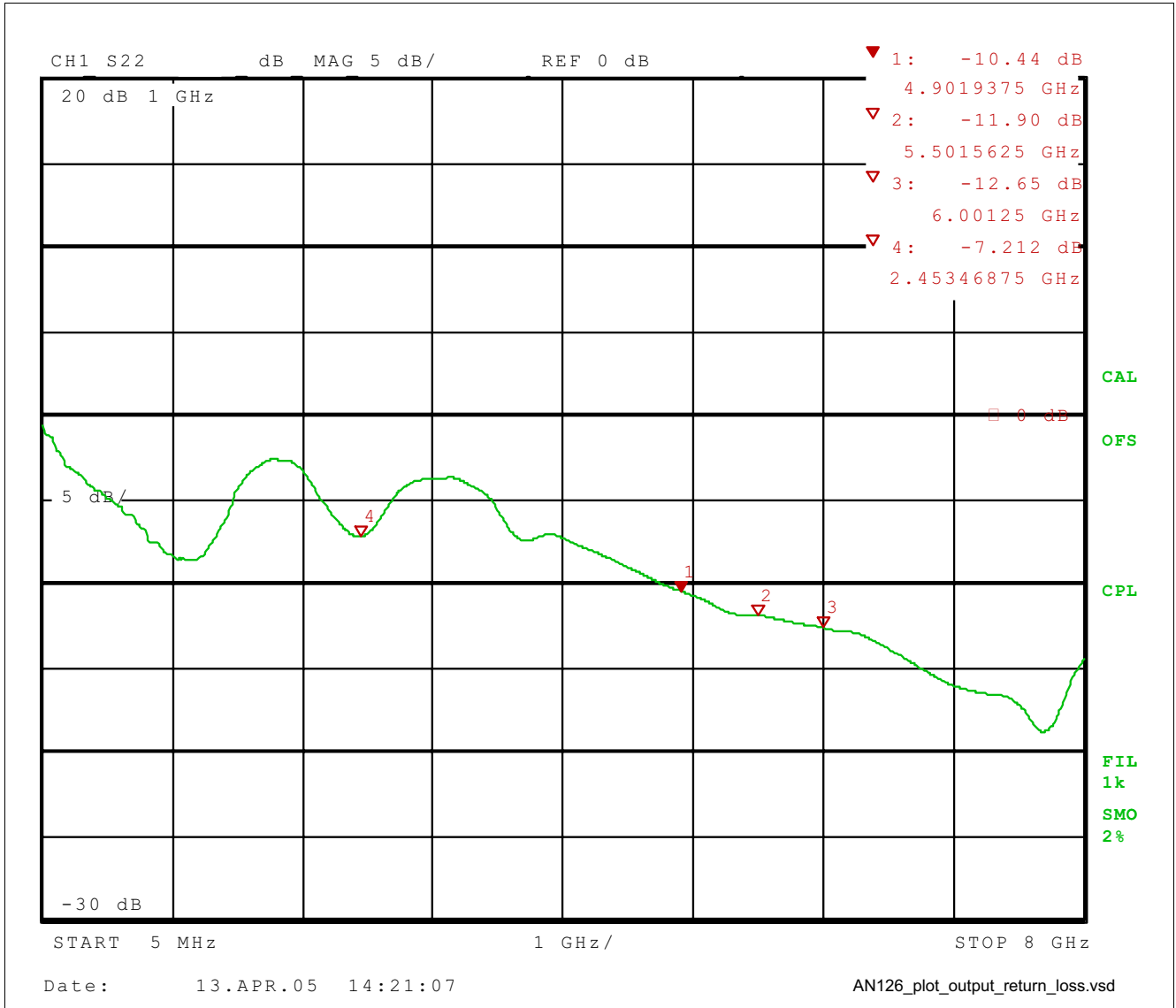


Figure 14 Plot of Output Return Loss

BFP640F Low-Noise Silicon-Germanium Transistor as 5-6 GHz Single-Stage

Output Return Loss, Smith Chart

Reference Plane = Output SMA Connector on PC Board
5 MHz to 8 GHz Sweep

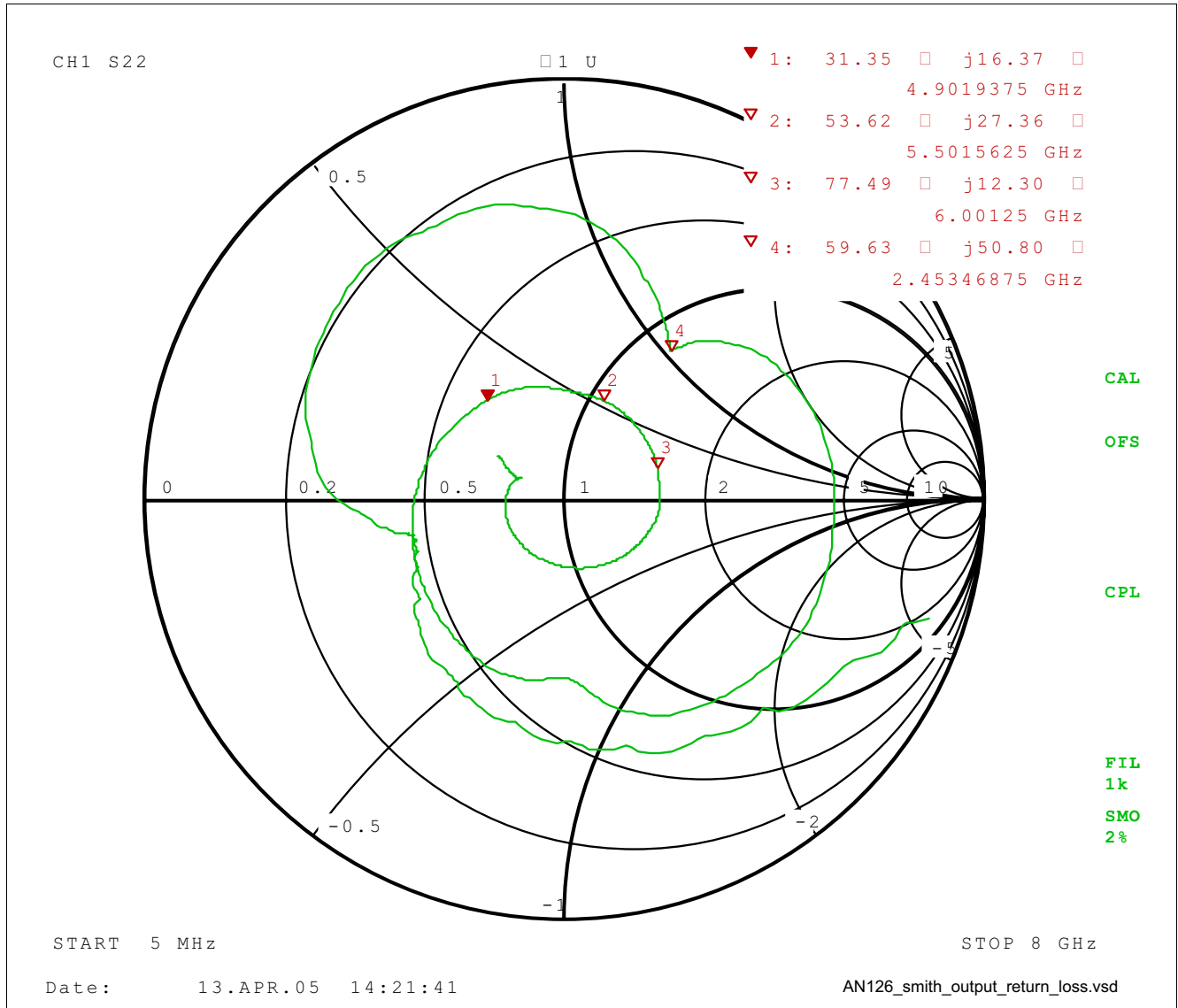


Figure 15 Smith Chart of Output Return Loss

BFP640F Low-Noise Silicon-Germanium Transistor as 5 -6 GHz Single-Stage

Input Stimulus for Amplifier Two-Tone Test

$f_1 = 5150$ MHz, $f_2 = 5151$ MHz, -23 dBm each tone.

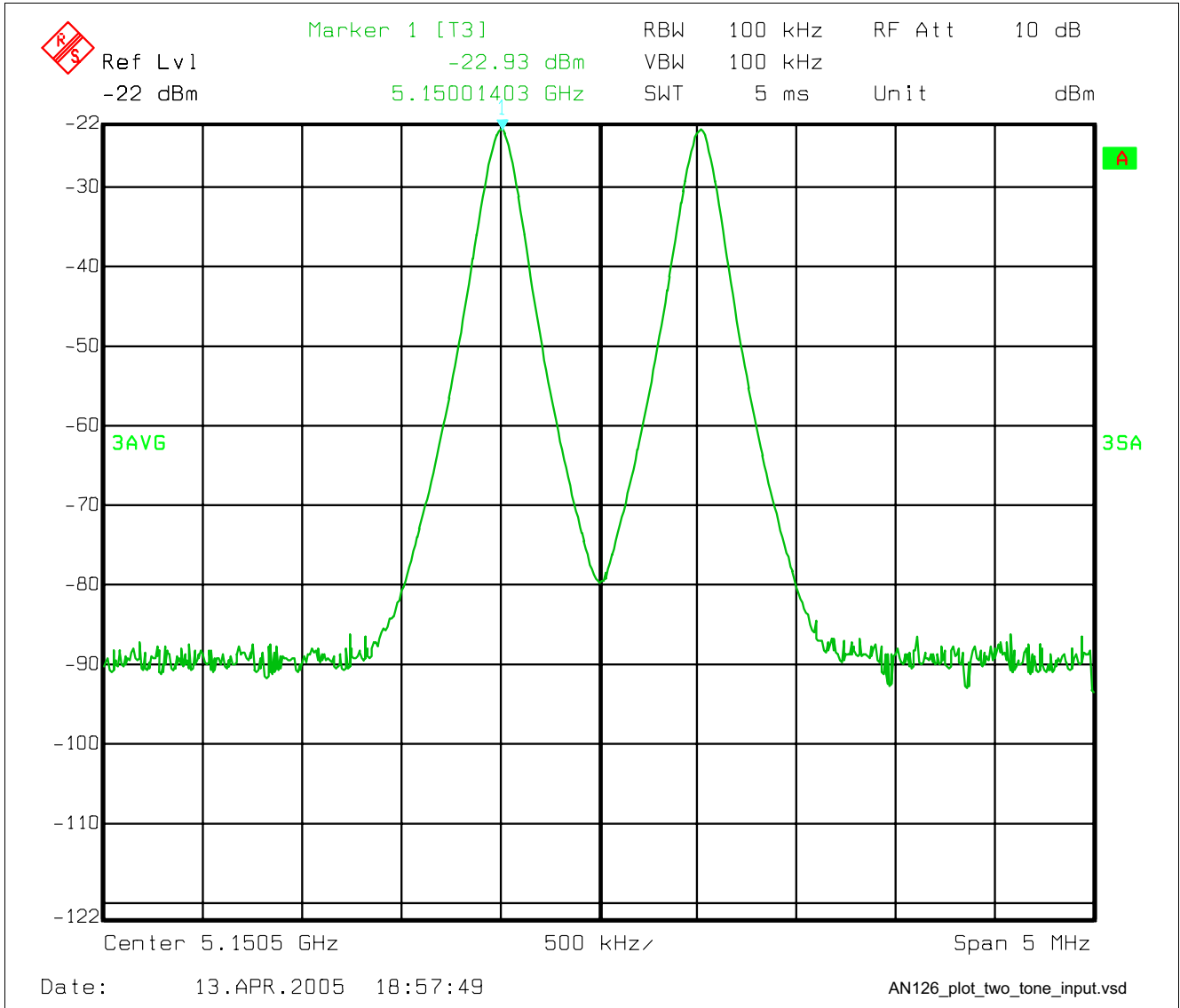


Figure 16 Two-Tone Test, Input Stimulus

BFP640F Low-Noise Silicon-Germanium Transistor as 5 -6 GHz Single-Stage

LNA Response to Two-Tone Test

Input $IP_3 = -23 + (63.3/2) = +8.7$ dBm

Output $IP_3 = +8.7$ dBm + 10.7 dB gain = + 19.4 dBm

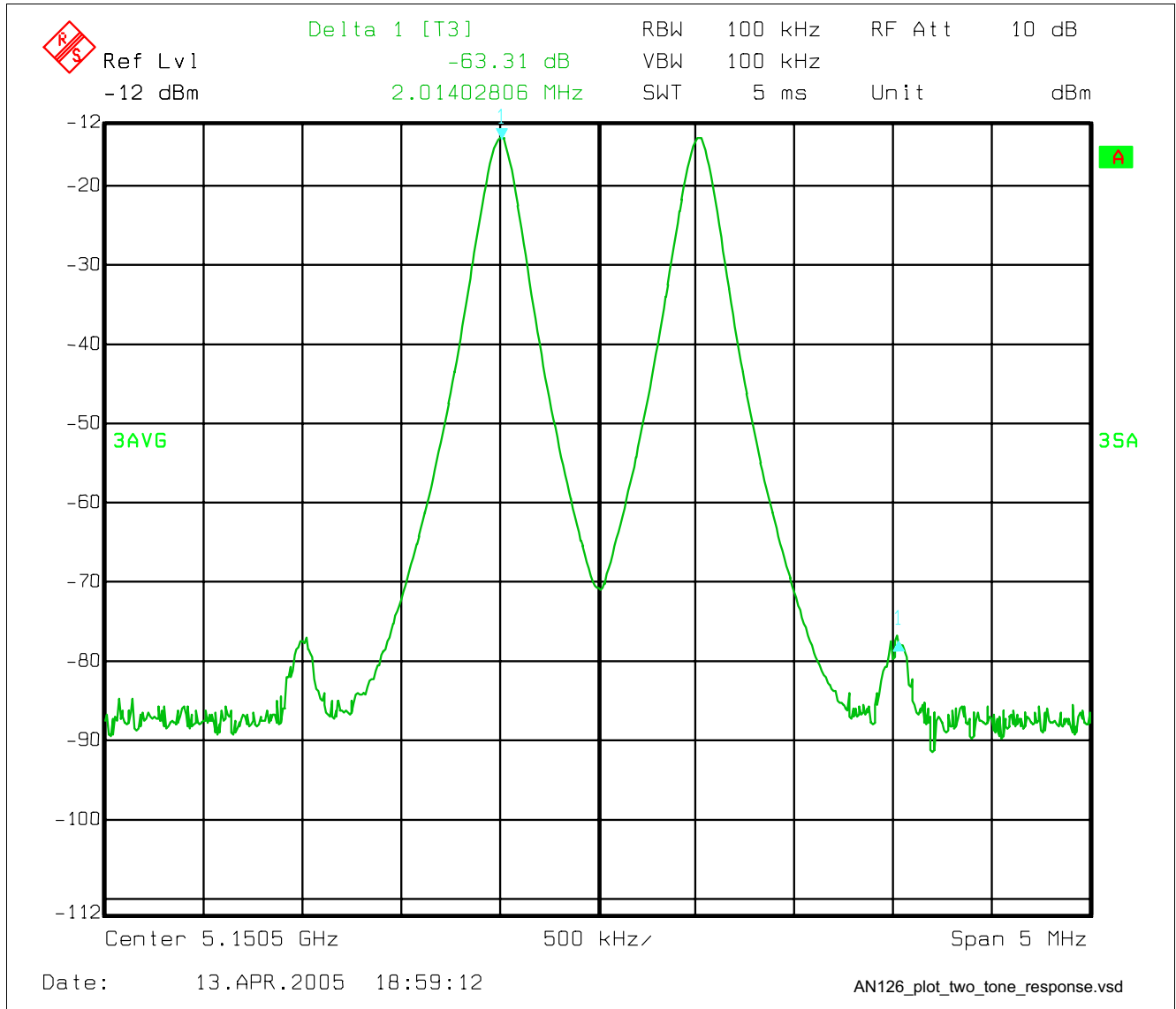


Figure 17 Two-Tone Test, LNA Response