Application Note No. 103

ESD and Antenna Protection using Infineon ESD0P8RFL

RF & Protection Devices

Never stop thinking

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1 Introduction

Electrostatic discharge (ESD) plays an important role when ESD sensitive devices are connected to exposed interfaces or antennas that can be touched by humans. This is usually applicable to low noise amplifiers (LNAs) and therefore LNAs must be properly protected against ESD in order to avoid irreversible damage of the LNA. For mobile applications low voltage supply and low current consumption is a major issue that requires new technologies with smaller transistor structures. However, the smaller the transistor structure the more sensitive the transistor is to ESD events.

Therefore, RF-LNAs and RF-MMICs based on new front-end technologies have already ESD protection elements integrated on-chip. These on-chip ESD protection techniques are always a compromise between good ESD protection and RF performance. Therefore, integrated RF ESD concepts hardly ever achieve an ESD protection above ±2 kV as defined by the human body model (HBM). An on-chip ESD protection of ±1 kV (HBM) is quite sufficient to protect the chip from ESD events in the manufacturing environment where stringent measures are taken to prevent electrostatic buildup. However, external interfaces for USB and memory cards, for example, as well as exposed antennas require always higher ESD protection levels of at least ±8kV contact protection as per the IEC 61000-4-2 specification.

For this reason an additional ESD protection device must be placed between antenna and LNA. As we will see later on, this is often not sufficient because even state-of-the-art ESD protection devices do not absorb ESD events completely. It will be shown that diodes provide much lower clamping voltages and therefore better ESD protection capabilities than polymer-based ESD protection devices and varistors. With regards to this, it is important to keep in mind that an ESD protection device which can withstand 15kV or even higher ESD events, may not protect the following device (LNA, ASIC, etc.) from the same ESD event.

In order to achieve at least ±8kV contact protection on an exposed antenna, an additional filter between the ESD protection device and the LNA is required. The purpose of this filter is to reduce the energy of the ESD pulse by filtering out as much energy as possible. The input matching network that is often needed in order to provide minimum noise figure of the LNA is nothing else than a filter and helps therefore to enhance the ESD protection capability. Because most of the energy of an ESD pulse is located at lower frequencies and since the operating frequency of LNAs is often at frequencies above 1GHz, a high-pass (or even band-pass) matching network is the first class to protect the LNA from high voltage ESD events.

It is self-evident that an input match (or filter) is not suitable for either wideband LNAs or ultra low noise amplifiers with noise figures as little as 0.5 dB. Both wideband and ultra low noise amplifiers are realized using discrete transistors without any input match. Unlike MMICs, discrete transistors do not have an additional ESD protection integrated on-chip. Because of this, high performance RF transistors (Infineon SiGe BFP6xx, BFP7xx) can only withstand ESD events of several 100 V without integrated and external ESD protection as defined by the HBM. But the SiGe-transistor ESD robustness is still even higher as the ESD performance of single low noise GaAs PHEMT devices. Just by using state-of-the-art SiGe RF transistors (BFP6xx, BFP7xx) it is only possible to achieve an adequate ESD protection by using Infineon's ESD protection devices. A slight degradation in RF performance (noise figure) could be possible at higher operational frequencies. Polymer-based ESD protection devices with very low capacitance suffer from too high trigger voltages, so that ESD sensitive high performance RF transistors are not protected by them at all.

2 Standards

While the IEC 61000-4-2 standard **[1]** relates to systems and sub-systems the JEDEC standard no. 22-A114D (JESD22-A114D) **[2]** establishes a standard procedure for testing and classifying microcircuits according to their susceptibility to damage or degradation by exposure to a defined electrostatic Human Body Model (HBM) discharge. This means that devices such as discrete transistors and MMICs are tested as per JEDEC standard (device-level characterization) while the printed circuit board or the whole system is then tested as per IEC

standard (system-level tests). Most of the devices in a system will not be affected by electrostatic discharges, because either they are surrounded by insulating materials or there are external circuits that will absorb ESD events. Only when pins of the device are connected to the outside world, for example a LNA that is connected to an exposed antenna, the electrostatic discharge will affect the device. Because both standards use different electrostatic discharge models the results are not directly comparable. The typical equivalent ESD circuit for the measurement setup (without parasitics) is shown in **Figure 1** and **Table 1** shows some general parameters of the ESD generators. First the storage capacitor C1 is charged to the desired ESD test voltage by the high voltage pulse generator and then the stored energy

$$W_{\mathrm{charge}} = \frac{C_1 \cdot V_{\mathrm{ESD}}^2}{2} \tag{1}$$

is discharged over the resistor R1 and the device under test (DUT). According to **Equation (1)** the 150 pF storage capacitor used as per the IEC 61000-4-2 standard stores 50% more energy than the 100 pF capacitor used as per the JESD22-A114D standard when both capacitors are charged to the same ESD test voltage. Furthermore, the 1500 Ω discharge resistor dissipates more energy than the 330 Ω resistor, so that the dissipated energy in the DUT calculates as follows:

$$W_{\mathrm{DUT}} = \frac{C_1 \cdot V_{\mathrm{ESD}}^2}{2} \cdot \frac{R_{\mathrm{DUT}}}{R_{\mathrm{DUT}} + R_1}. \tag{2}$$

Therefore, with a discharge model as per the IEC 61000-4-2 standard approximately six times more energy is dissipated in a 50 Ω load compared to the JESD22-A114D standard for a given ESD test voltage. Moreover, there is a high current peak of up to 4 A/kV ESD test voltage within the first 2 ns of the discharge waveform as per the IEC 61000-4-2 standard (see **Figure 2** and **Figure 3**), which can result in breakdown of dielectrics. **Figure 2** shows a typical contact discharge waveform of an ESD generator as per the IEC 61000-4-2 standard through a shorting wire. **Figure 3** on the other hand shows a typical current waveform of an ESD generator as per the JESD22-A114D standard through a shorting wire.

To sum up, we can say that the IEC 61000-4-2 standard makes greater demands on the ESD robustness of the device than the JESD22-A114D standard. Nevertheless, if failures are only due to thermal overload but not due to breakdown of dielectrics, both standards can be compared by estimating the thermal energy absorbed in the device:

$$W_{\mathrm{el}} = \int_0^t V_{\mathrm{dev}}(t) I_{\mathrm{dev}}(t)\,\mathrm{d}t\,. \tag{3}$$

For all measurements presented in this application note ESD events were generated with a hand-held ESD gun as per IEC 61000-4-2 specification (contact discharge).

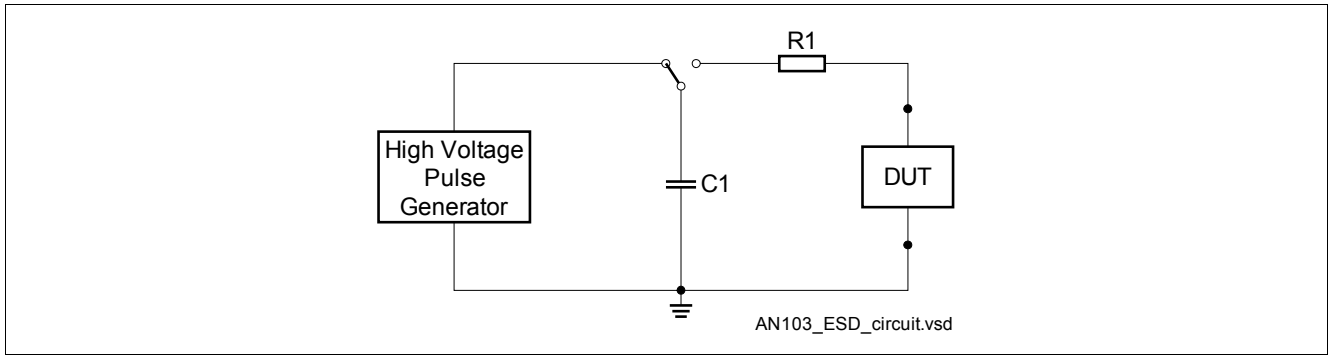

Figure 1 Typical equivalent ESD circuit

Table 1 General ESD generator parameters

	IEC 61000-4-2	JESD22-A114D
Typical storage capacitance (C1)	150 pF	100 pF
Typical discharge resistance (R1)	330 Ω	1500 Ω
Rise time for short	0.7–1 ns	2–10 ns
Peak current for short	3.75 A/kV (±10%)	0.6–0.74 A/kV

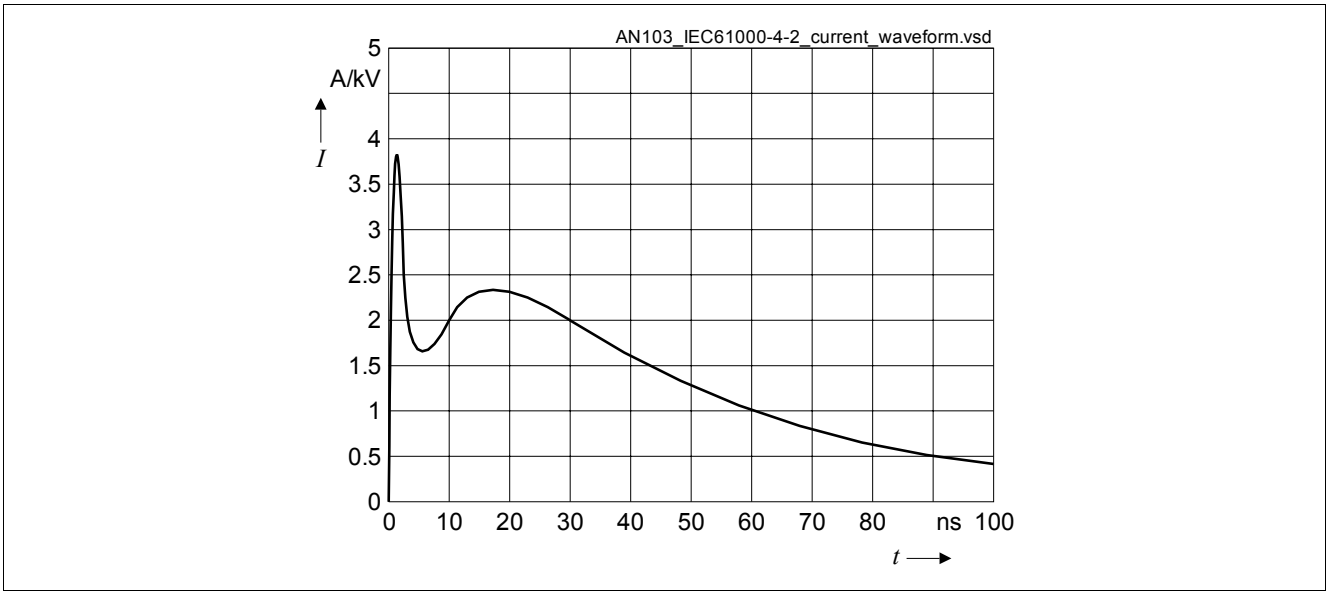

Figure 2 Contact discharge waveform of ESD generator, charge voltage = 1 kV (IEC 61000-4-2)

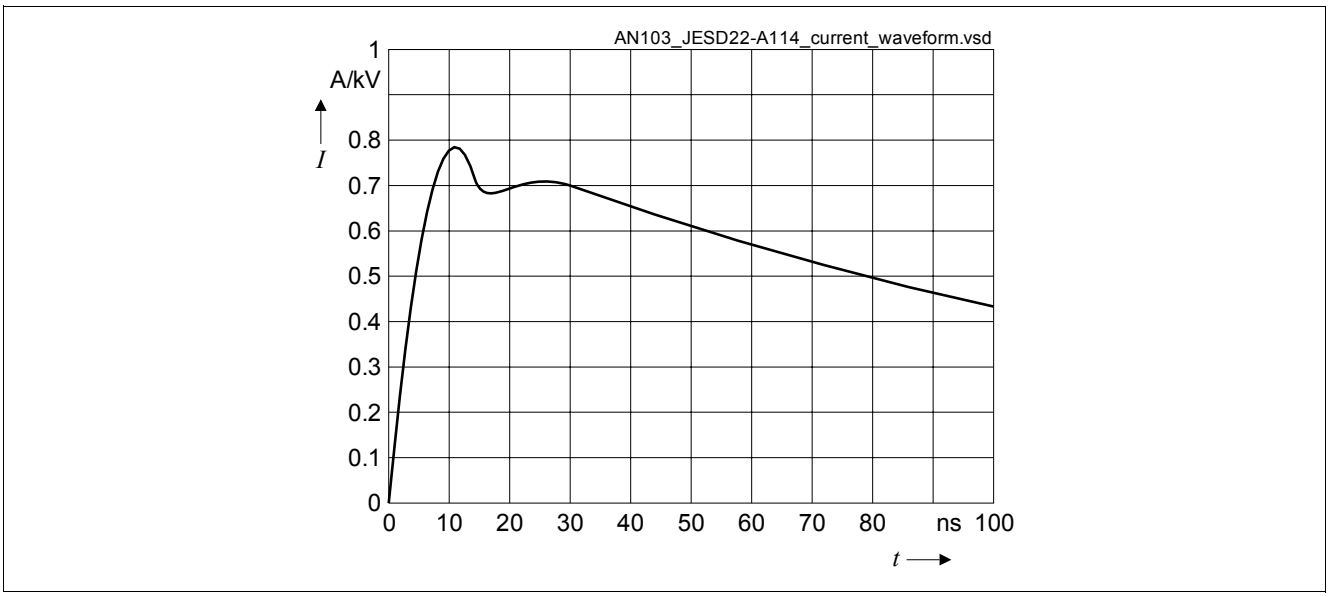

Figure 3 Current waveform through a shorting wire, charge voltage = 1 kV (JESD22-A114D)

3 Basic concepts of ESD protection

There are primarily four different concepts on how diodes can be used for ESD protection:

- PIN diodes optimized for fast switching time (for applications requiring low capacitances)
  - Anti-parallel configuration
  - Rail-to-rail configuration
- Zener diodes optimized for high currents
  - Uni-directional configuration
  - Bi-directional configuration

The appropriate configuration depends on the superimposed DC voltage level on the prote cted signal line and the peak voltage of the RF signal. Since silicon diodes start conducting at approximately 0.5 V (0.1 mA at 25 °C), the anti-parallel configuration shown in **Figure 4 (a)** is only appropriate for DC-free signal lines and low RF signal levels as it can be found for instance at antennas of GPS receivers, remote keyless entry (RKE) receivers and receivers for wireless broadcasting services like satellite radio, DVB, DAB, DMB and so on. The anti-parallel configuration also provides the lowest clamping voltage out of all the above listed configurations, because either of the two diodes operates in forward direction in the case of an ESD event. This makes it the preferred configuration when it comes to antenna protection for RF receivers. PIN diodes allow very low capacitances of less than 1 pF, but can not be operated in reverse direction like Zener diodes. Since both diodes are in parallel the total capacitance of an ESD protection diode in anti-parallel configuration, also referred to as line capacitance C_T, is twice the capacitance of either diode (both diodes are of equal size).

For high RF signal levels or in general for RF signals or digital high-speed data lines with superimposed DC voltage levels from 0 V up to the supply voltage (V_{CC}) on the protected signal line (USB 2.0, HDMI, …) the rail-to-rail configuration as shown in **Figure 4 (b)** can be used. However, this configuration demands for an additional ESD protection diode to provide a path to ground for positive ESD events. Since also the power supply line (V_{CC}) should always be protected by an ESD protection diode, this is not a disadvantage.

Figure 4 (c) shows a bi-directional configuration with two diodes in series but reverse order so it can be used at any voltage level between -V_{RWM} and +V_{RWM} (maximum reverse working voltage of the diode). Since both diodes are in series the line capacitance of the ESD protection diode in bi-directional configuration is only half the capacitance of either diode (if both diodes are of equal size which may not necessarily be true). This is the preferred configuration for applications using bipolar signals (CAN, AF signal lines, …). Since either diode operates in both directions in the case of an ESD event, the clamping voltage of an ESD protection diode in bi-directional configuration is higher than the clamping voltage of an ESD protection diode in anti-parallel configuration. Furthermore, in order to enable operation in reverse direction, the active area of Zener diodes must be of larger size and therefore Zener diodes have higher capacitance than PIN diodes.

Figure 4 (d) finally shows an ESD protection diode in uni-directional configuration with only one single diode that operates in either direction in the case of an ESD event. This configuration is only applicable at voltage levels between 0V and +V_{RWM} and has the highest line capacitance out of all the four configurations. However, in uni-directional configuration the clamping voltage is lower than in bi-directional configuration. Therefore, uni-directional ESD protection diodes are primarily used to protect power supply lines and are therefore optimized for very high currents rather than low capacitance.

In the following we will address **RF antenna protection** with Infineon's low-capacitance ESD protection diode ESD0P8RFL in anti-parallel configuration as shown in **Figure 4 (a)**. This diode has a line capacitance C_T of only 0.8 pF at 1 GHz and a series inductance of only 0.2 nH. Since it is used in anti-parallel configuration this means that either diode has a capacitance of 0.4 pF and a series inductance of 0.4 nH. This low series inductance is possible because the ESD0P8RFL protection diode is packaged in the 4-pin Thin Small Leadless Package (TSLP-4-7) with an overall size of only 1.2 mm x 0.8 mm x 0.39 mm, so only bond wires make a major contribution to the unwanted inductance. The low capacitance allows it to protect RF signal lines up to approximately 1 GHz without any need for compensation for the diode's capacitance. For frequencies above

1 GHz the diode's capacitance must be compensated with an additional inductance in parallel to the diode. More details about how this is done are shown in **Chapter 6** later on in this application note and in the application note AN086 on Infineon's home page.

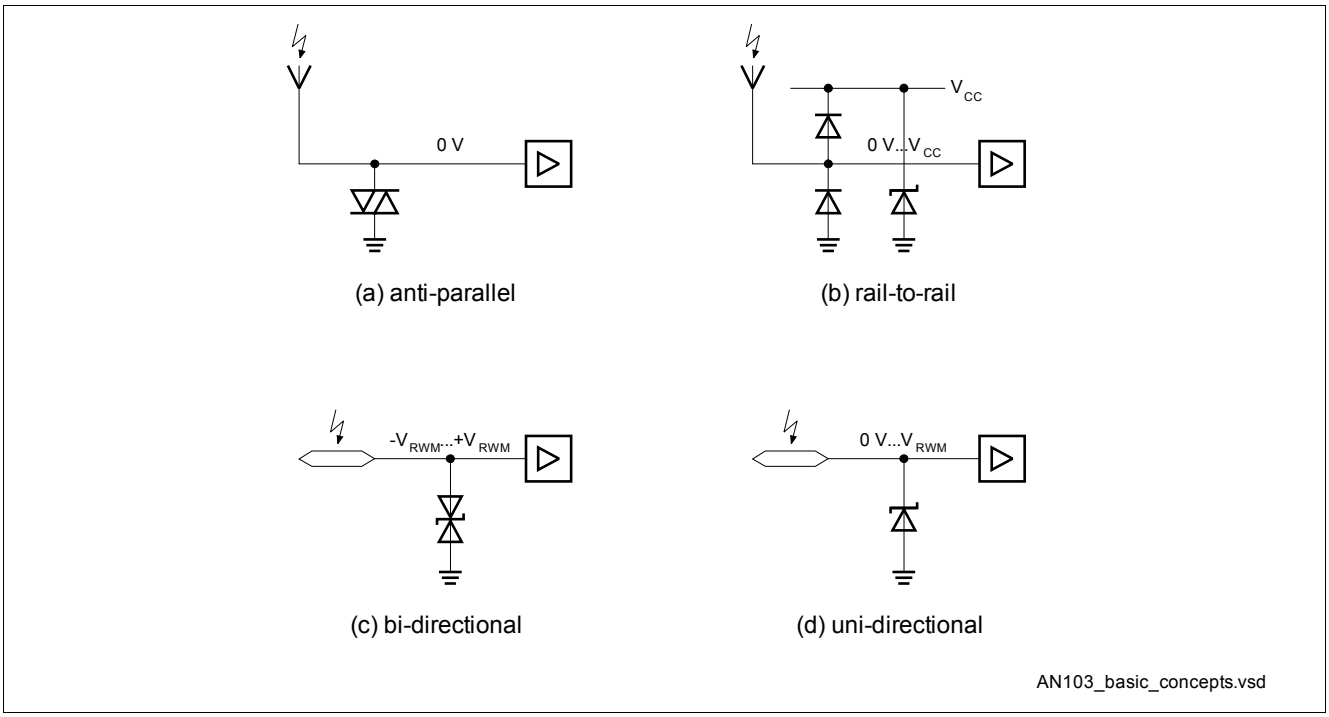

Figure 4 Four basic concepts of ESD protection with diodes depending on the superimposed DC voltage level on the protected signal line

4 Overview on ESD protection devices

Today several different ESD protection devices are available on the market that can be split into three distinct technologies:

- Semiconductors (ESD protection diodes)
- Varistors (ceramic based on zinc-oxide)
- Polymer-based ESD protection devices

An ideal ESD protection device has zero capacitance, zero inductance, clamps the transient voltage to a sufficient low voltage level and is highly linear. Unfortunately, non of the above technologies can meet all of these requirements of an ideal ESD protection device. Though polymer-based ESD protection devices have very low capacitances (typically less than 0.15 pF), they suffer from high trigger voltages and high clamping voltages so that the thermal energy of the ESD event is either not or only partially absorbed by the polymer-based ESD protection device. Varistors with low capacitance (less than 1 pF) suffer from high varistor voltages, which is the voltage at 1 mA current flow, and therefore also from very high clamping voltages.

Infineon's state-of-the-art ESD protection diode ESD0P8RFL offers a capacitance of only 0.8 pF at 1 GHz as well as a fast switching time of less than 200 ps and clamps an 8 kV ESD event as per the IEC 61000-4-2 specification

to only 10 V. This makes the ESD0P8RFL a first-class ESD protection device for RF antennas and high speed data lines (HDMI, S-ATA, Gbit Ethernet, …).

A comparison between a polymer-based ESD protection device, a low-capacitance varistor and Infineon's low-capacitance ESD protection diode ESD0P8RFL is shown in **Table 2** which points out the peak voltage (V_{peak}), the clamping voltage (V_{cl}) after 30 ns and the dissipated thermal energy (W_{el}) at a 50 Ω load. The measurement setup for clamping voltage measurements is shown in **Figure 5**. Since the peak voltage of 2 kV ESD events (at 50 Ω) is still below the trigger voltage of the polymer-based ESD protection device, ESD events up to 2 kV will not be absorbed by the polymer-based ESD protection device (see **Figure 8** and **Figure 9**). Low-capacitance varistors on the other hand have very high clamping voltages far in excess of 100 V and are therefore unsuitable for ESD protection (see **Figure 10** and **Figure 11**) of ESD sensitive devices.

The clamping voltage of Infineon's ESD0P8RFL protection diode is shown in **Figure 6** and **Figure 7**. Both peak voltage and clamping voltage and therefore also the thermal energy dissipated in the load is much lower than for a polymer-based ESD protection device or a low-capacitance varistor.

Table 2 Comparison between different ESD protection devices and ESD test voltages (IEC 61000-4-2)

ESD Protection Device	ESD Test Voltage (kV)	V_{peak} (V)	V_{cl} @ 30 ns (V)	W_{el} @ 50 Ω (nWs)
Infineon ESD0P8RFL	2	23	3	20
	8	43	10	200
Polymer-based ESD protection device	2	306	150	33,200
	8	486	64	17,000
Varistor with capacitance of typical 0.5 pF	2	245	120	22,700
	8	528	300	151,000

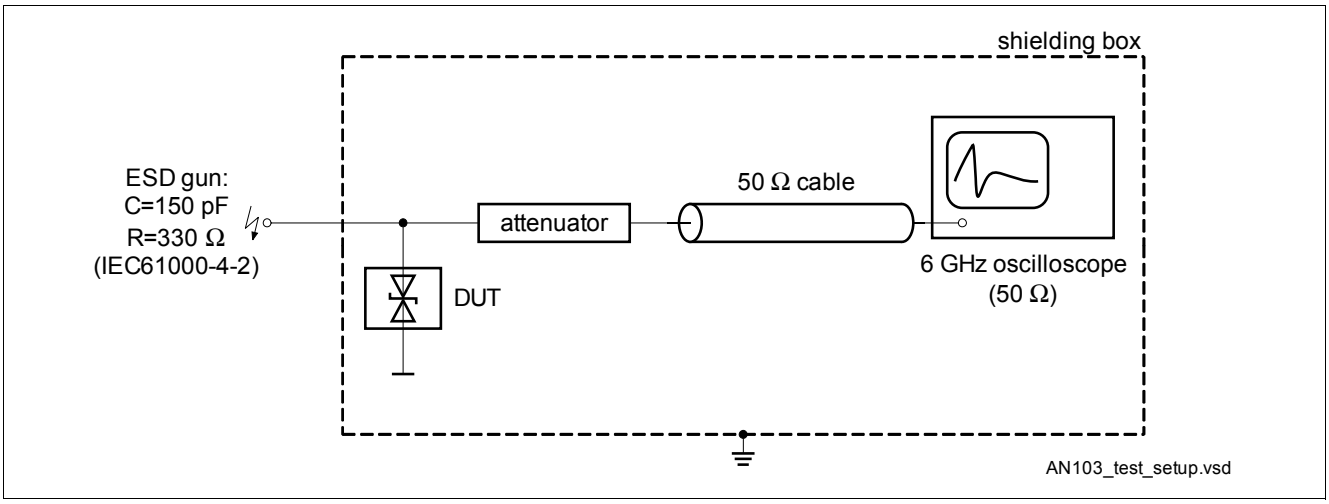

Figure 5 Measurement setup for clamping voltage

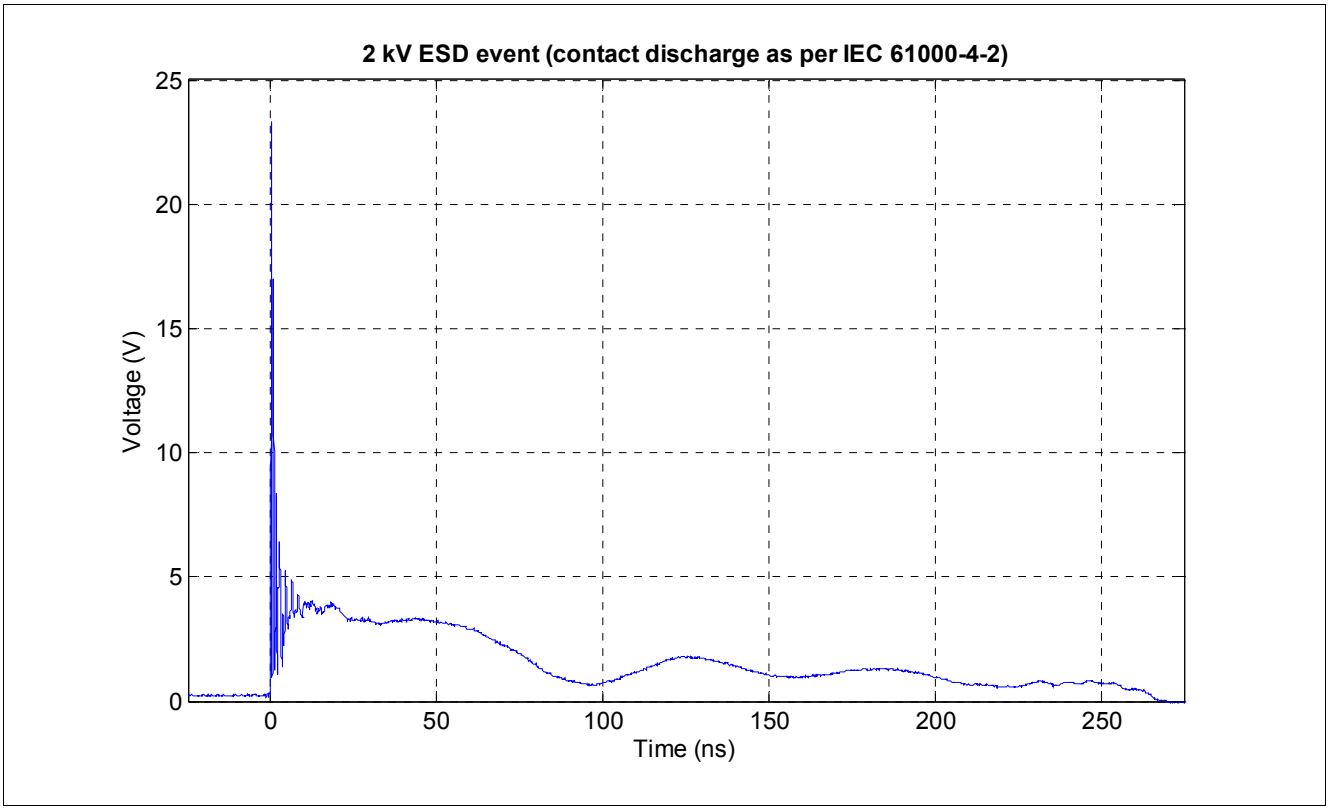

Figure 6 2 kV contact discharge ESD event applied to ESD0P8RFL diode and 50 Ω

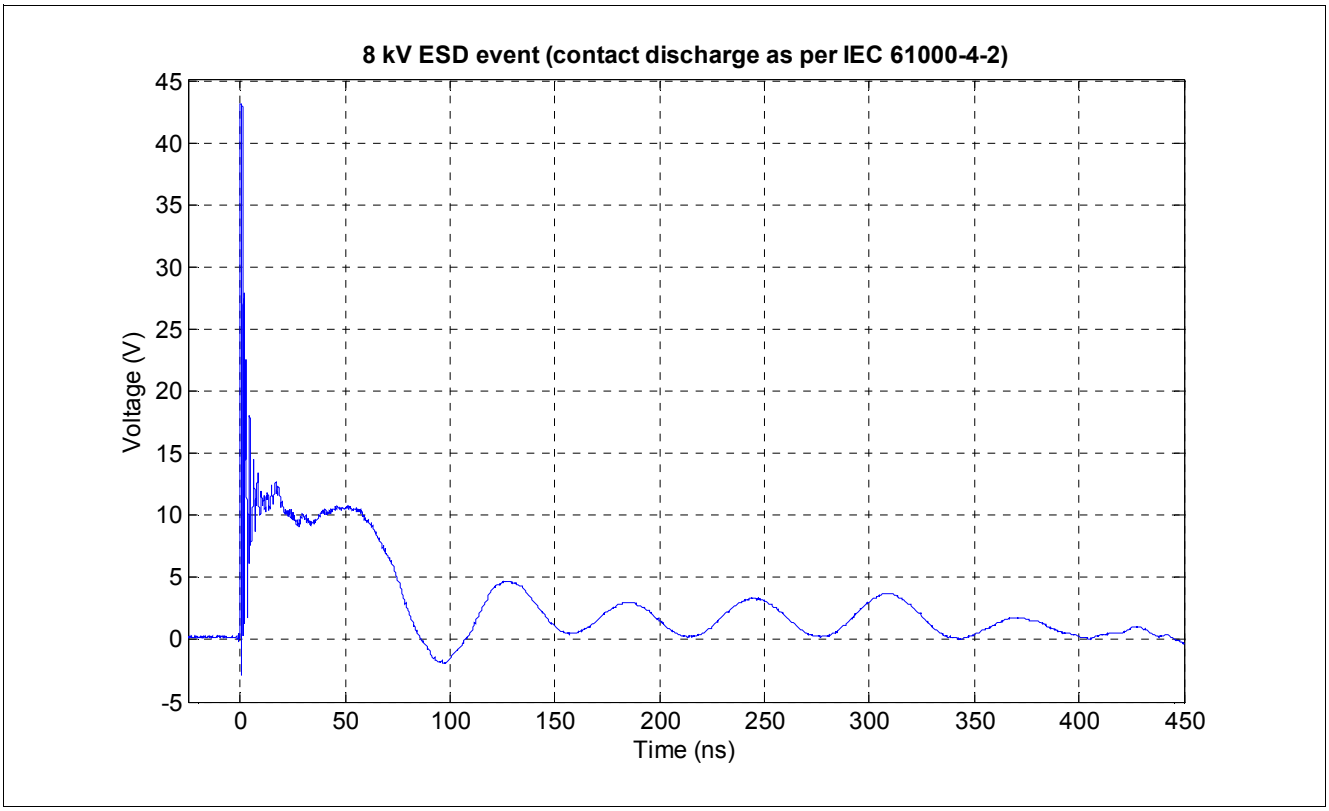

Figure 7 8 kV contact discharge ESD event applied to ESD0P8RFL diode and 50 Ω

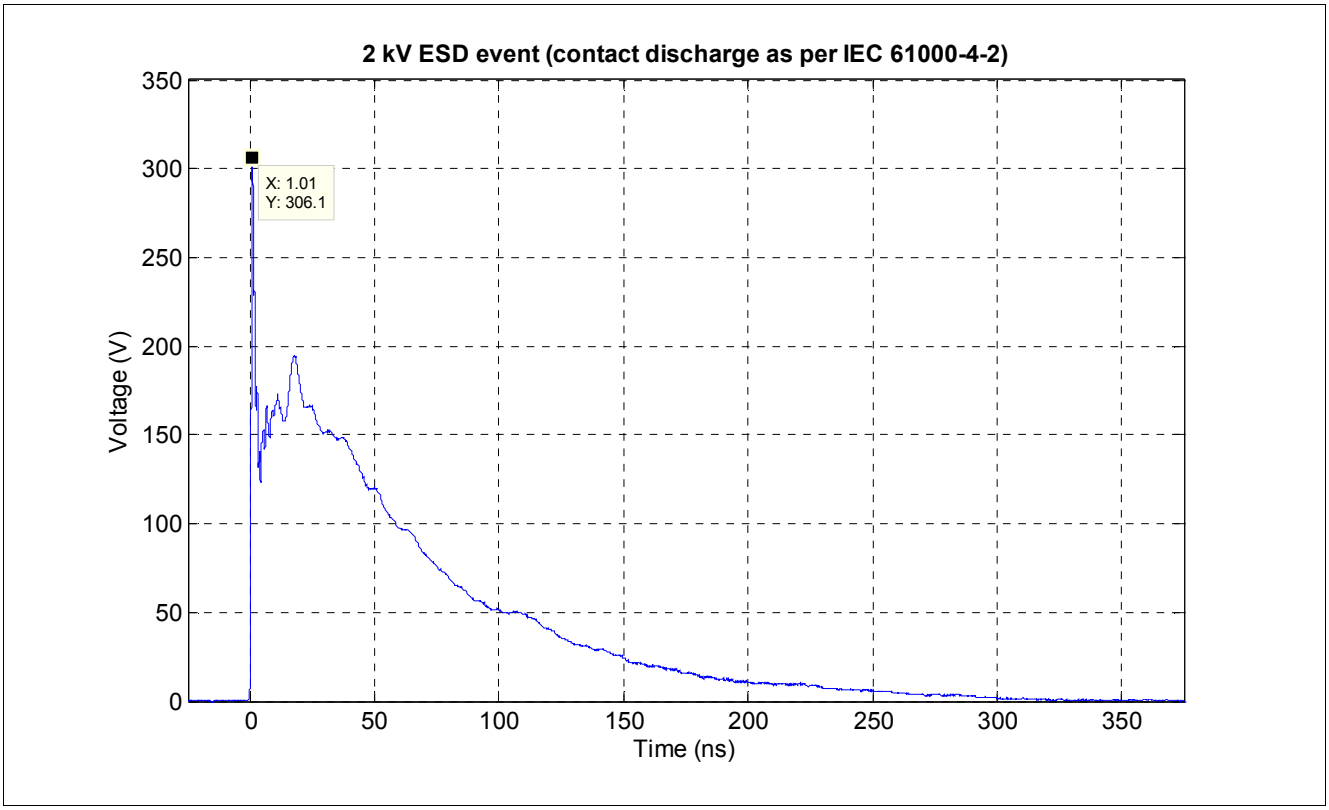

Figure 8 2 kV contact discharge ESD event applied to polymer-based ESD protection device and 50 Ω

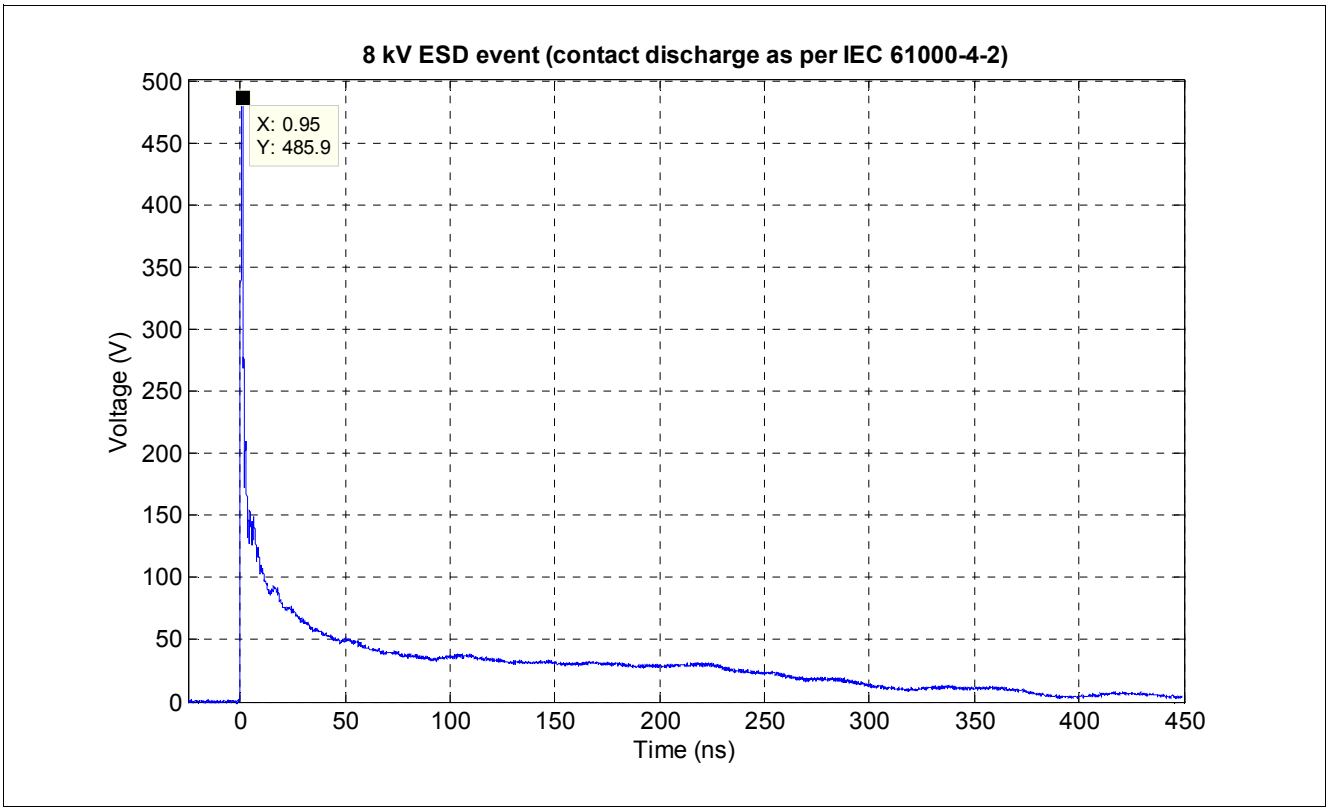

Figure 9 8 kV contact discharge ESD event applied to polymer-based ESD protection device and 50 Ω

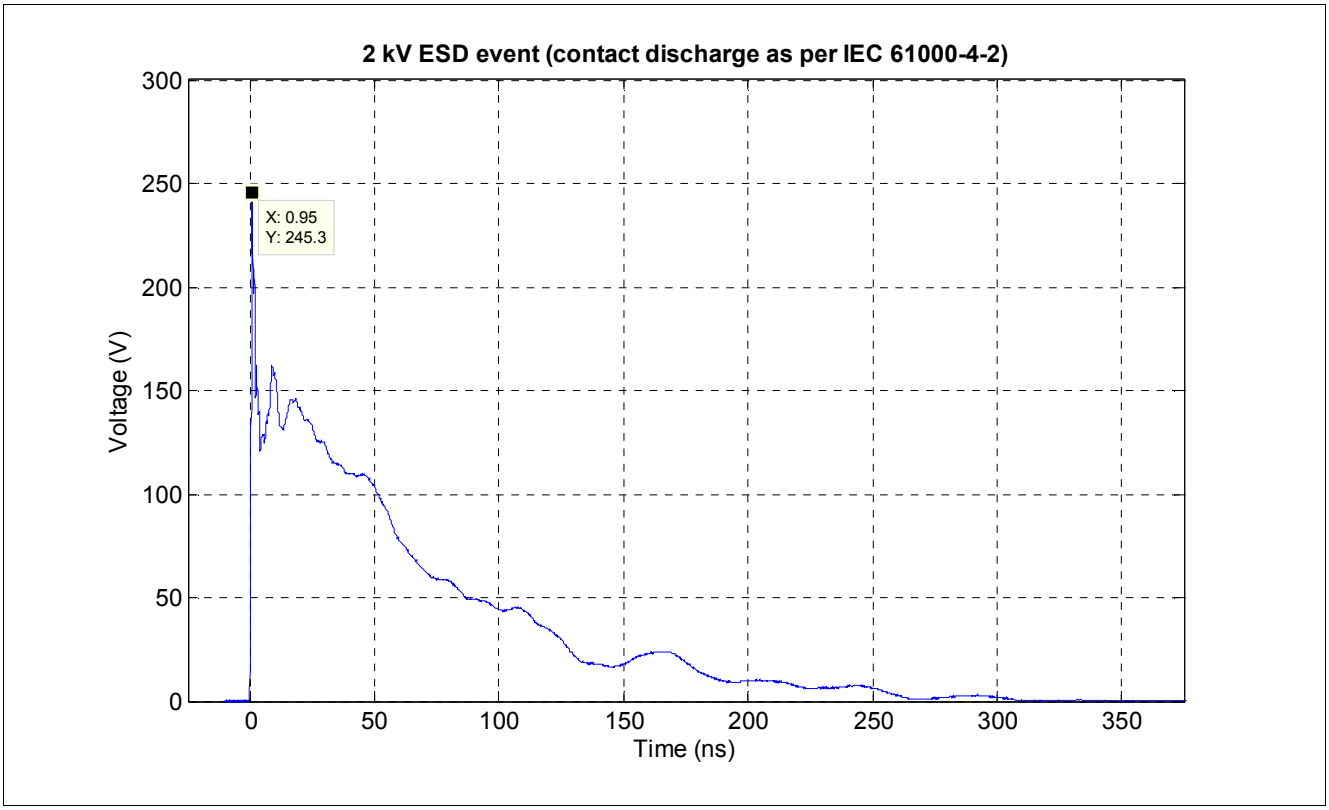

Figure 10 2 kV contact discharge ESD event applied to 0.5 pF varistor and 50 Ω

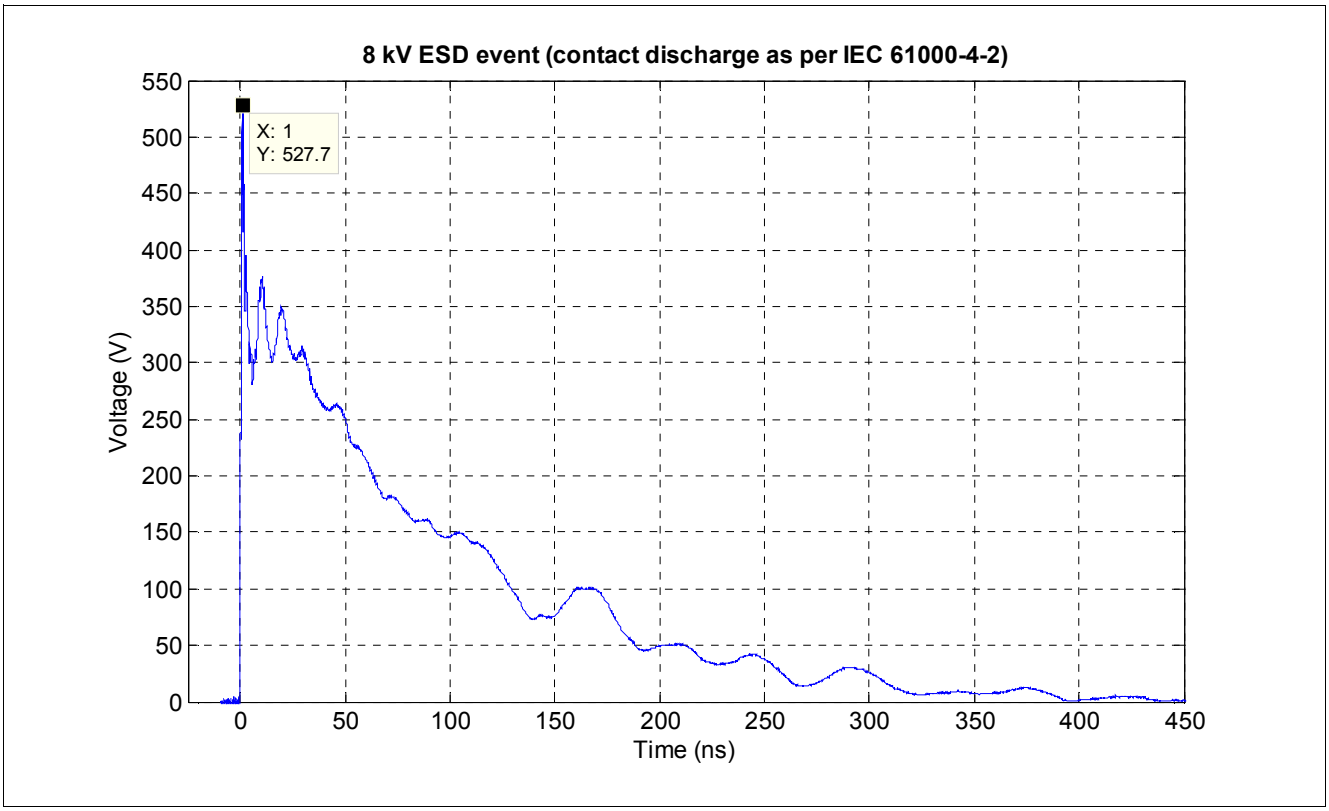

Figure 11 8 kV contact discharge ESD event applied to 0.5 pF varistor and 50 Ω

5 Failure mechanisms from ESD events at the example of BJTs

First we have to clarify the question about the failure mechanisms for RF bipolar junction transistors (BJTs) during an ESD event and how we can check the transistor for damage. Permanent failures are for example the result of junction burnout, shorts or metallization melt due to thermal overload. Metallization melt is also considered a secondary failure mechanism, because it occurs when a secondary breakdown results in a short-circuit, which then draws enough current to melt the metallization or bond wires. Although there are several failure mechanisms caused by ESD events, it has been found that for newer-generation RF transistors the base-emitter junction is the weak point while for older-generation RF transistors the base-collector junction is the weak point.

Failures from ESD events result in increased leakage currents and beta (h_{FE}) degradation of the transistor which can be checked by measuring the supply current. Further stress with increased ESD test voltages finally destroys the transistor due to metallization melt which can of course also be checked by the supply current. Even though measuring the supply current is the easiest method, it is not the most accurate one since leakage currents are much smaller than the collector current. So, it is advisable to take a safety margin for the ESD robustness into account when failures from ESD events are only checked by measuring the supply current.

Now let's have a closer look at the ESD protection capability of the ESD protection diode ESD0P8RFL on the RF transistor BFP540ESD without any filter, that is just the diode before the transistor as it is shown in the schematic in **Figure 12**. BFP540ESD is an ESD hardened RF transistor with a guaranteed ESD robustness of 1 kV as defined by the HBM. As one can see in **Figure 13**, the transistor protected by the ESD protection diode can survive positive ESD events up to +6 kV without degradation in beta and negative ESD events up to -3 kV as per the IEC 61000-4-2 standard. Usually a bipolar transistor is more robust to positive ESD events than to negative ESD events. This is because positive pulses are absorbed by the transistor's base-emitter diode which is operated in forward direction. By this means a bipolar transistor protects itself to positive ESD events and thus for the transistor's ESD robustness negative ESD events are the crucial factor.

This example is intended to illustrate failures from ESD events and is not applicable to any real world application. As we will see in the next chapter, an additional inductor in parallel to the diode is needed for frequencies above 1 GHz. Furthermore, narrow-band LNAs make use of an input network for noise matching. With the right choice of matching network together with Infineon's ESD0P8RFL the ESD robustness of the system increases by leaps and bounds.

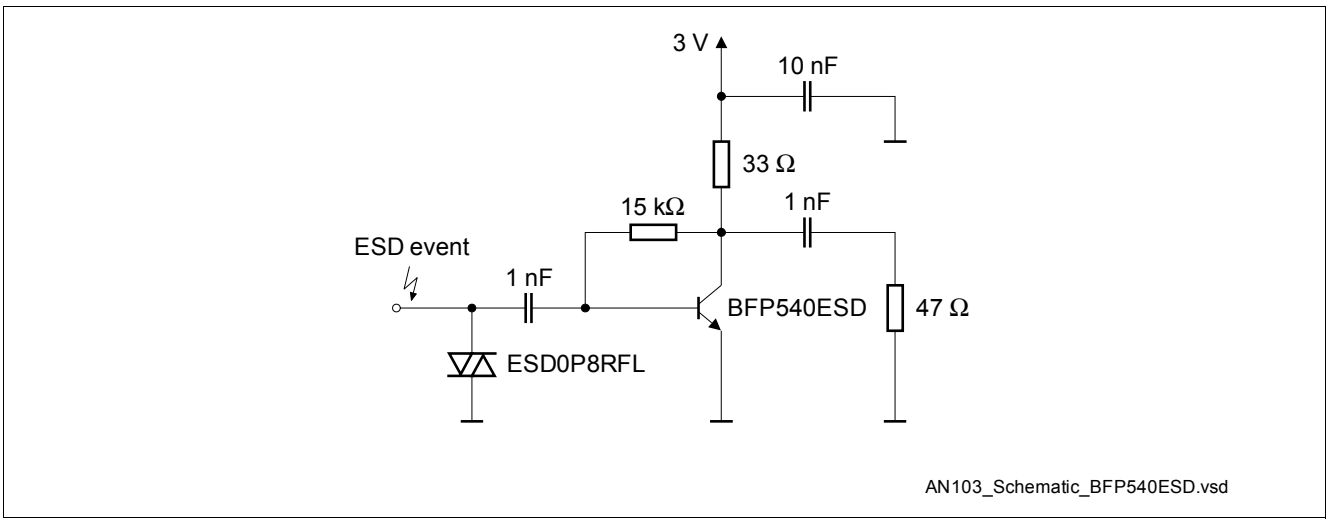

Figure 12 Schematic of ESD test board with BFP540ESD

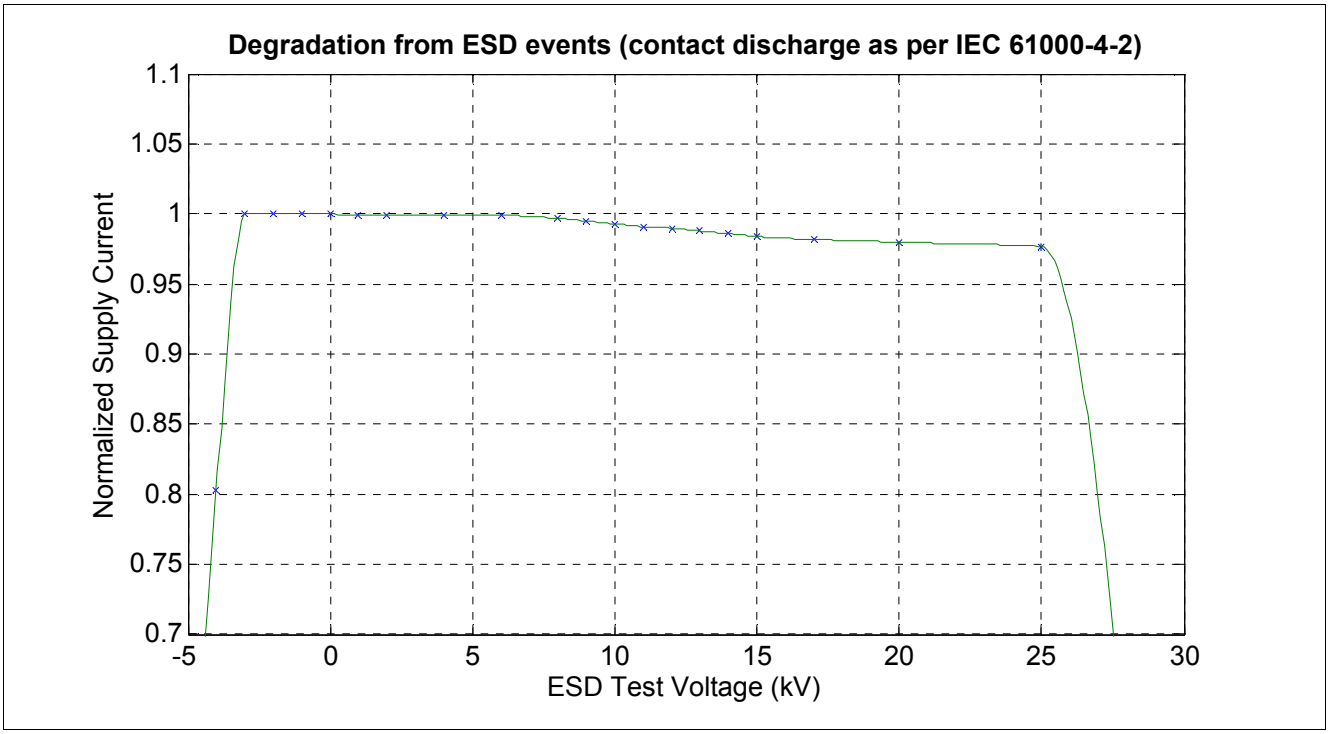

Figure 13 Supply current of ESD hardened transistor BFP540ESD after applying ESD events

6 Application examples

Two different applications are shown here in order to show how Infineon's ESD protection diode ESD0P8RFL can be used to protect LNAs from ESD events injected into the antenna. The first application is a LNA for GPS receivers using Infineon's BGA615L7. The second application is a LNA for receivers for digital media broadcasting services via satellite (S-DMB) using BGA622L7.

6.1 Antenna protection for GPS using BGA615L7

Infineon's BGA615L7 is a dedicated LNA for civilian GPS applications with a minimum noise figure of 0.9 dB (with all losses before BGA615L7 subtracted). As already mentioned earlier in this application note we have to compensate for the capacitance of the ESD protection diode. This is done with an inductor in parallel to the diode and the necessary inductance is calculated as follows:

$$L = \frac{1}{(2\pi f)^2 \cdot C}, \tag{4}$$

where C is the capacitance of the diode and f is the operating frequency. With C = 0.8 pF and f = 1575.42 MHz (the L1 frequency used by civilian GPS) the inductance is calculated to be L = 12.8nH and we have chosen a 12 nH inductor. **Figure 14** shows the schematic of BGA615L7 with its default circuit as used on Infineon's application board together with the ESD0P8RFL protection diode and the 12 nH inductor in parallel. **Table 3** summarizes the electrical characteristics of one sample on Infineon's application board (see **Figure 16**) according to the schematic in **Figure 14**. Neither input 1 dB compression point (IP_{1dB}) nor input third order intercept point (IIP_3) degrade in the presence of the ESD protection diode. Noise figure is only slightly increased, because of the additional 12 nH inductance.

BGA615L7 has integrated ESD protection diodes on-chip and its guaranteed ESD robustness at all pins is ±1 kV as defined by the HBM. However, in the system we have to achieve at least ±8 kV contact protection (level 4) as per the IEC 61000-4-2 standard, which makes higher demands on the ESD robustness than the HBM as we have already seen in **Chapter 2**. Because bipolar transistors are typically damaged by negative ESD events first, the ESD test voltage was increased step-by-step from -1 kV to -30 kV (or until the device was damaged). In order to minimize variance, 10 ESD events at a rate of 10 Hz were applied per ESD test voltage. As we have seen in **Chapter 5**, current consumption is an easy to measure indicator for failures from ESD events and therefore after every test cycle the overall current consumption (I_{CC} plus I_{ON}) of BGA615L7 was measured. The result is shown in **Figure 15** and one can see that BGA615L7 passed ESD events of -30 kV. Therefore, +30 kV ESD events were applied to BGA615L7 and it passed again as expected.

It was demonstrated that the ESD protection diode ESD0P8RFL is able to protect BGA615L7 up to ±30 kV (or even more). When we take a 30% safety margin into account, we can claim that BGA615L7 is effectively protected from at least ±20 kV ESD events and satisfies therefore easily level 4 of IEC 61000-4-2. However, as we will see next, ESD protection capability also strongly depends on the input matching network. For BGA615L7 a high-pass filter with a corner-frequency of above 1 GHz is used for input matching and therefore most of the energy of an ESD event, which is located mostly at the lower frequencies, is blocked by the input matching network.

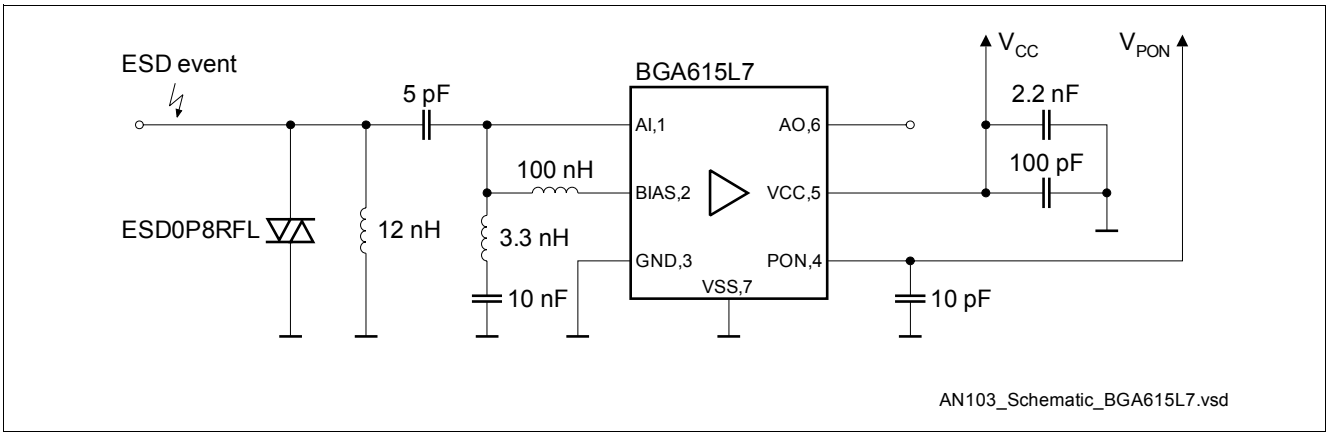

Figure 14 Schematic for GPS LNA with BGA615L7 and ESD protection

Table 3 Electrical characteristics of BGA615L7 with ESD protection.
T_A = 25°C, V_{CC} = 2.8V, V_{PON} = 2.8V, f = 1575MHz (unless noted otherwise)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply current	I_{CC}		5.9		mA	
Gain	$\|S_{21}\|^2$		17.6		dB	
Input return loss	RL_{IN}		12.1		dB	
Output return loss	RL_{OUT}		33		dB	
Reverse isolation	I_{REV}		35		dB	
Noise figure	F		1.15		dB	Including SMA connector and PCB losses of evaluation board
Input 1dB compression point	IP_{1dB}		-8		dBm	
Input 3rd order intercept point	IIP_3		1		dBm	f_1 = 1575 MHz, f_2 = 1576 MHz P_{IN} = -30 dBm

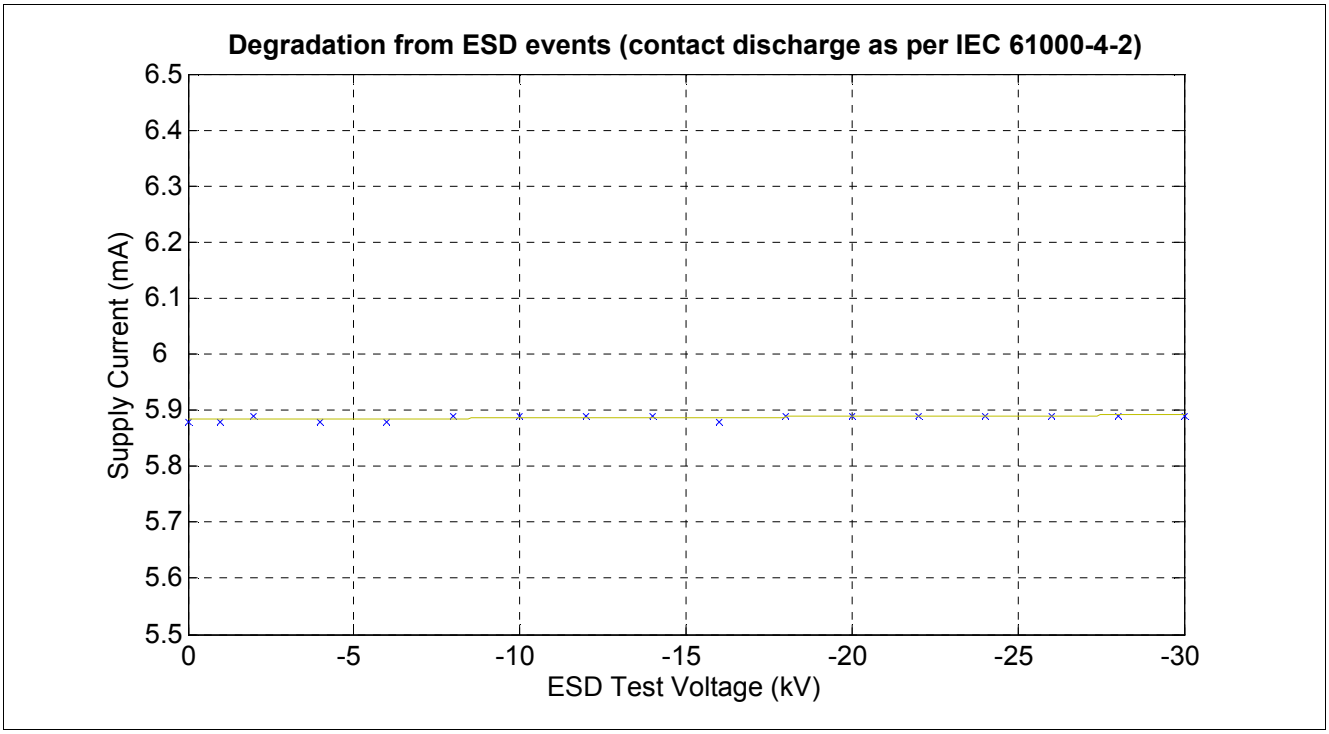

Figure 15 Supply current of BGA615L7 after applying ESD events in contact discharge mode

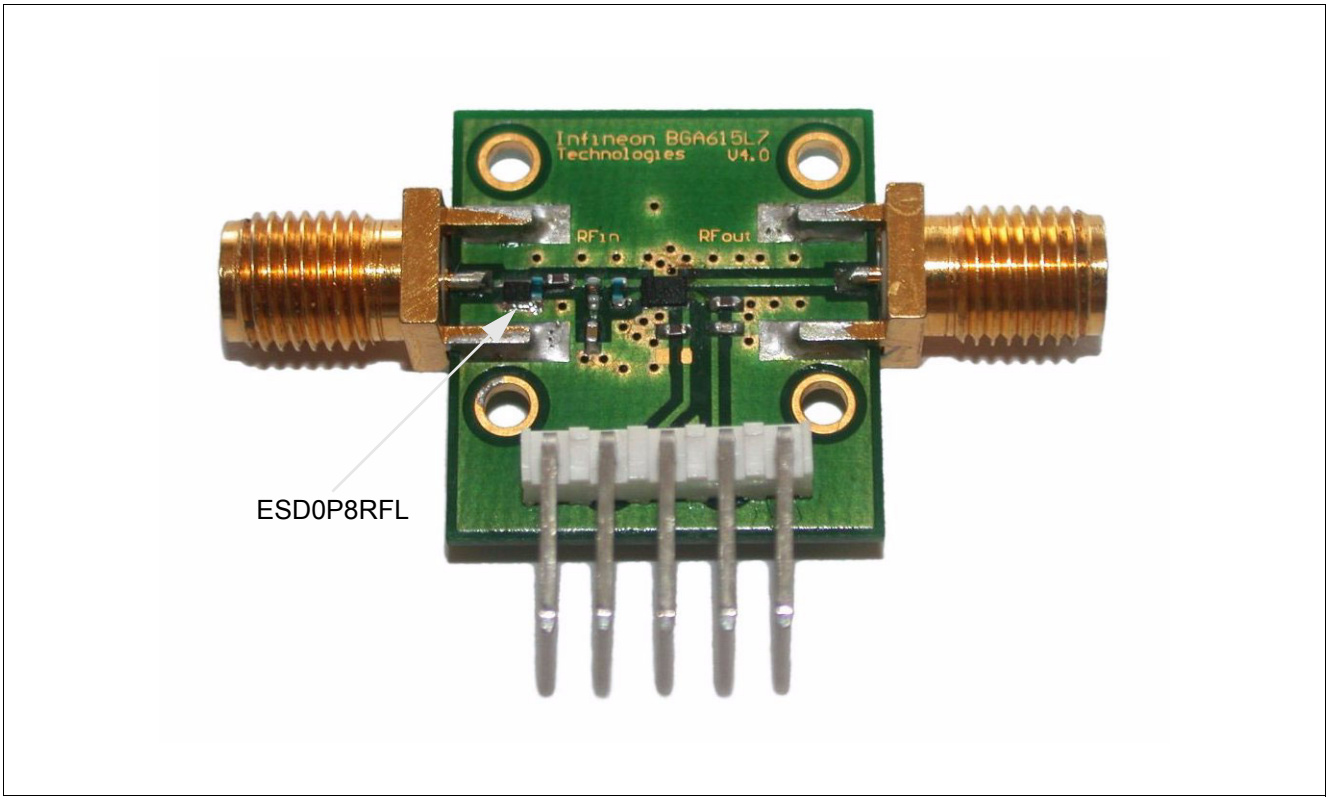

Figure 16 Photo of BGA615L7 application board with ESD0P8RFL protection diode

For BGA615L7 it is possible to use a modified input matching network (see **Figure 17**) with reduced part count but the same electrical characteristics (see **Table 4**) than the default input matching network features. This matching network offers also a low-frequency trap (10 nF capacitor plus 3.9 nH inductor) at the input of BGA615L7 for IIP_3 improvement. Please also note that now the inductance in parallel to the ESD protection diode is not only used to compensate for the diode's capacitance but also for noise matching of BGA615L7 and therefore a 3.9 nH inductor is used instead of a 12 nH inductor. Without the ESD protection diode a 5.6 nH inductor would be needed:

$$\frac{1}{\frac{1}{3.9\,\mathrm{nH}} - \frac{1}{12.8\,\mathrm{nH}}} = 5.6\,\mathrm{nH}\,. \tag{5}$$

The corner-frequency of this high-pass matching network is only 25 MHz and therefore it does not block as much energy arising from ESD events as the original matching network. The same procedure as for the original application board was applied to the modified one. The results are shown in **Figure 18** and one can see that now BGA615L7 could only survive ESD events up to -7 kV. Taking into account a safety margin of 30%, we can claim that BGA615L7 can withstand ±5 kV with the modified matching network. This means that now only level 2 of IEC 61000-4-2 can be satisfied.

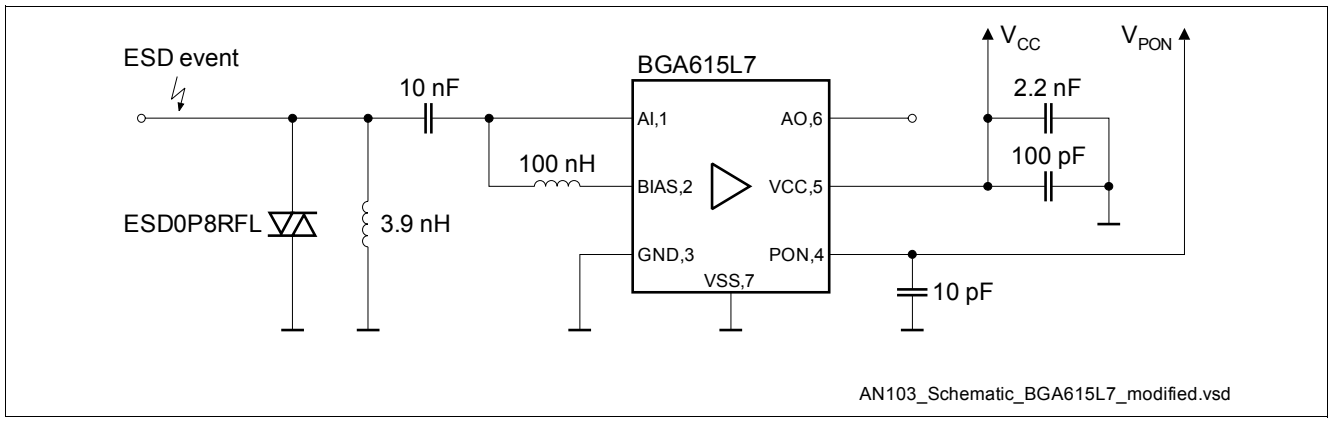

Figure 17 Schematic with modified matching and reduced part count for GPS LNA with BGA615L7 and ESD protection

Table 4 Electrical characteristics of BGA615L7 with modified matching and ESD protection. T_A = 25 °C, V_{CC} = 2.8 V, V_{PON} = 2.8 V, f = 1575 MHz (unless noted otherwise)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply current	I_{CC}		5.5		mA	
Gain	$\|S_{21}\|^2$		17.8		dB	
Input return loss	RL_{IN}		12.3		dB	
Output return loss	RL_{OUT}		33		dB	
Reverse isolation	I_{REV}		34		dB	
Noise figure	F		1.1		dB	Including SMA connector and PCB losses of evaluation board
Input 1dB compression point	IP_{1dB}		-8		dBm	
Input 3rd order intercept point	IIP_3		2		dBm	f_1 = 1575 MHz, f_2 = 1576 MHz P_{IN} = -30 dBm

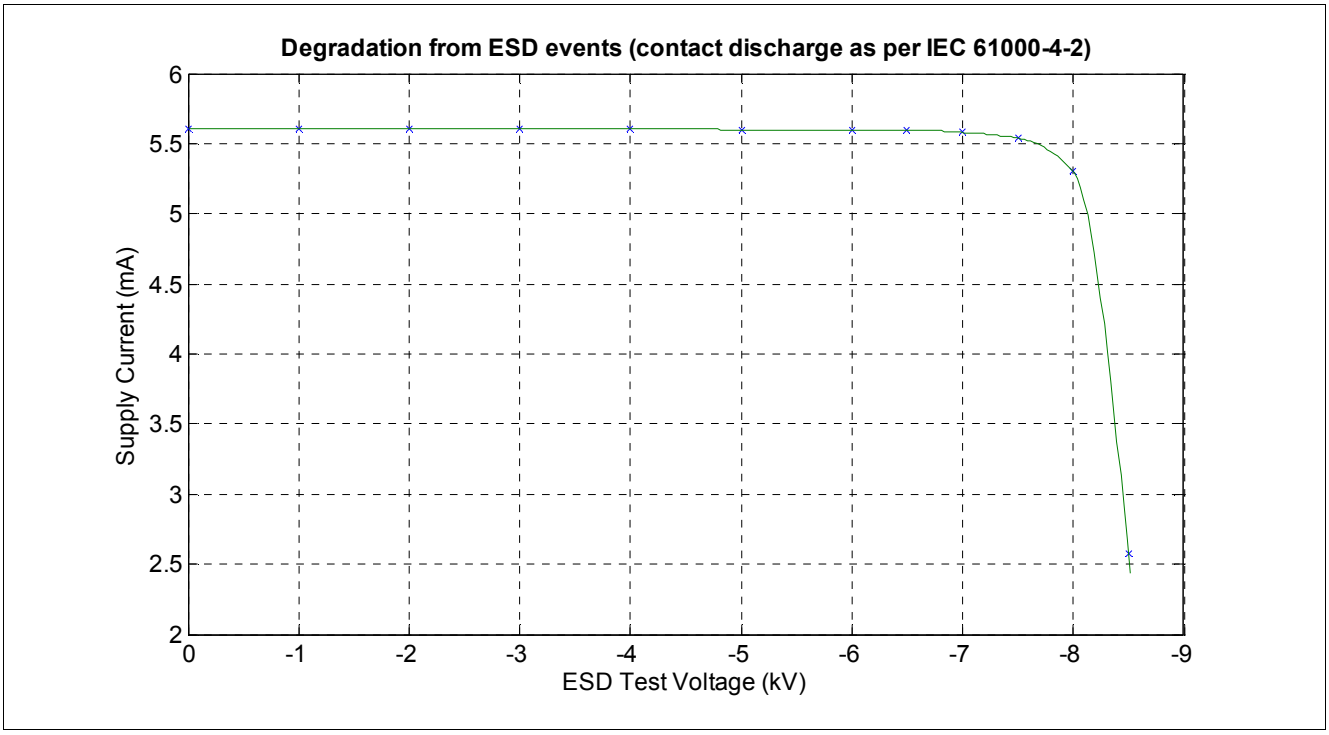

Figure 18 Supply current of BGA615L7 with modified input matching after applying ESD events

For comparison reasons BGA615L7 was also tested with a polymer-based ESD protection device (see **Figure 19**). The advantage of polymers is their very low capacitance of typically less than 0.15 pF, but their ESD protection capability is quite low (see **Figure 20**). While BGA615L7 protected by the ESD0P8RFL diode did not show any degradation in current consumption up to 30 kV, it started already degradation in current consumption for ESD test voltages greater than 10 kV when a polymer was used for ESD protection. Once again, we have to take 30 % safety margin into account. So, we can claim that a polymer-based ESD protection device can protect BGA615L7 up to ±7 kV or, in other words, that level 3 of IEC 61000-4-2 can be satisfied.

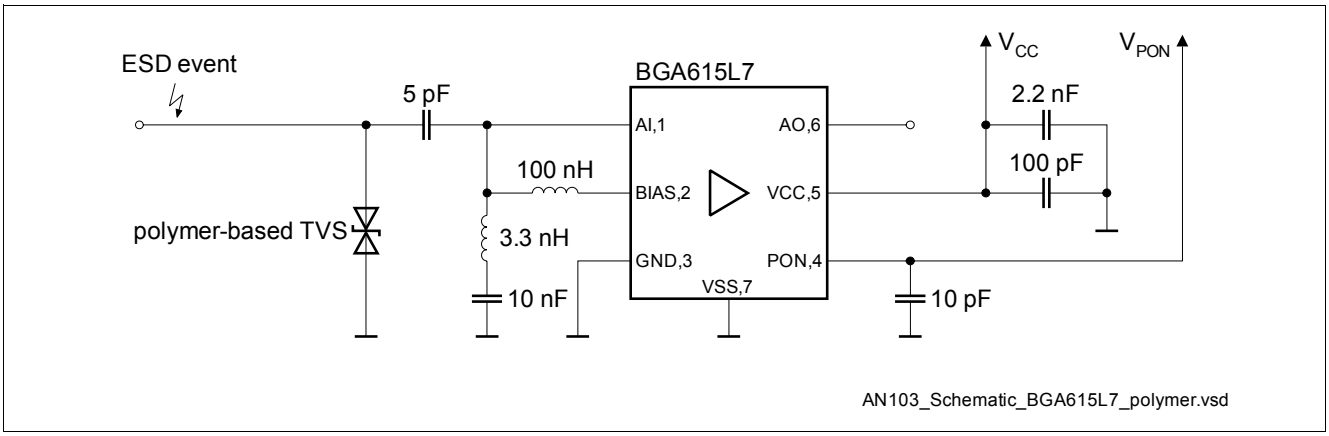

Figure 19 Schematic of GPS LNA with BGA615L7 and a polymer-based ESD protection device

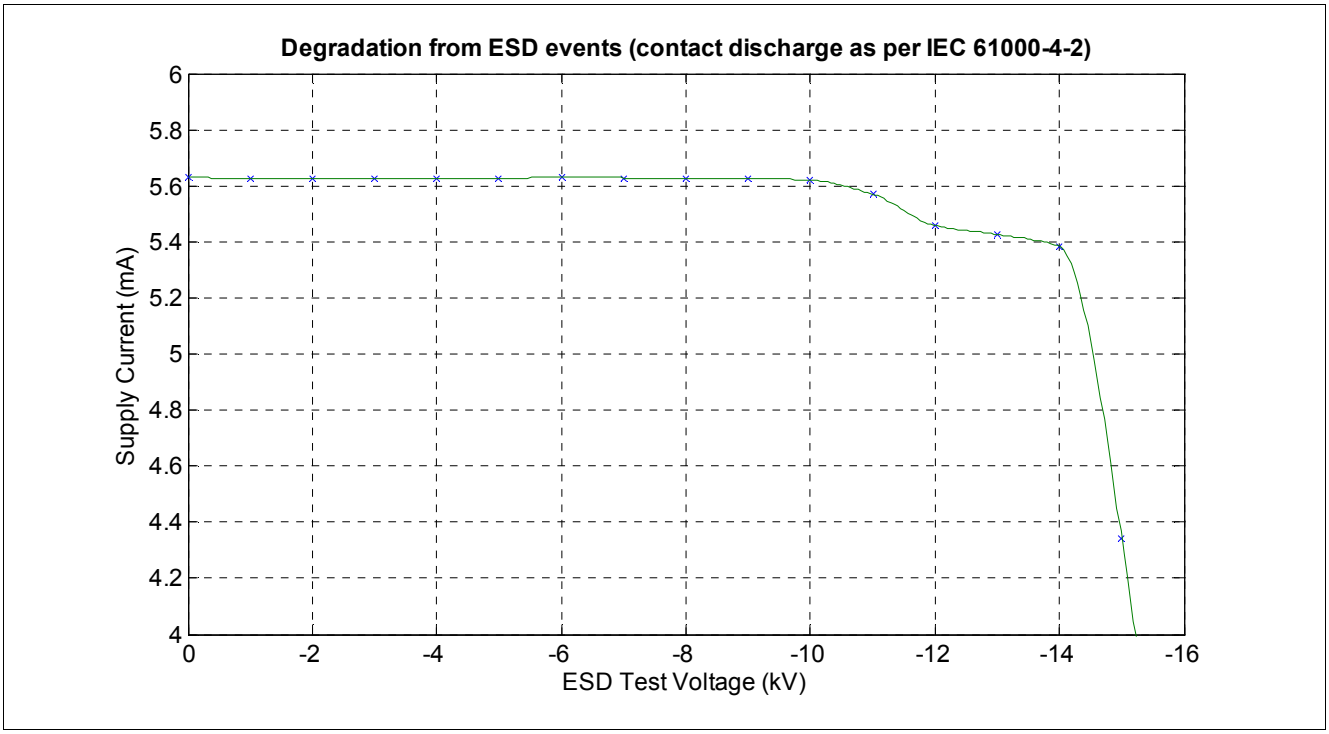

Figure 20 Supply current of BGA615L7 with polymer-based ESD protection device after applying ESD events

6.2 Antenna protection for S-DMB using BGA622L7

The second application example is a LNA for S-DMB receivers (digital media broadcasting services via satellite) using Infineon's BGA622L7. BGA622L7 is used for a wide variety of applications around the 2 GHz frequency band and it can be easily matched for S-DMB which operates from 2630 MHz to 2655 MHz. Only a small series inductance at the output of BGA622L7 is needed in order to have an output return loss of more than 10 dB. The schematic with Infineon's ESD0P8RFL protection diode is shown in **Figure 21** and **Figure 22** shows the photo of the application board. The 0 Ω resistor was only used to fill a gap on the application board and does not have any further function. According to **Equation (4)**, with C = 0.8 pF and f = 2642.5 MHz (mid-band frequency), the inductance in parallel to the protection diode is calculated to be L = 4.5 nH and we have chosen a 4.7 nH inductor, because it gives slightly better results than a 4.3 nH inductor. The electrical characteristics of the application board shown in **Figure 22** can be found in **Table 5**.

Like BGA615L7, also BGA622L7 comes with an integrated on-chip ESD protection and can withstand at least ±2 kV as defined by the HBM. Again, ESD test voltage was increased step-by-step from -1 kV to -30 kV and 10 ESD events at a rate of 10 Hz were applied at each ESD test voltage. The current consumption of BGA622L7 versus the ESD test voltage is shown in **Figure 23** and like BGA615L7 also BGA622L7 does not show any significant degradation in current consumption up to ±30 kV. This is not a surprise, because we are using again a high-pass matching filter with a corner-frequency greater than 500 MHz. Therefore, after taking again a 30% safety margin into account, we can also claim a contact protection of at least ±20 kV for BGA622L7. Again, level 4 of IEC 61000-4-2 is easily satisfied.

Although not always applicable, the capacitance of the protection diode can also be used for matching purposes at high frequencies. However, the inductance in parallel to the protection diode provides a low frequency path to ground and strengthens therefore not only robustness against ESD but also against lightning (IEC 61000-4-5), because the energy of such pulses largely accumulates at lower frequencies.

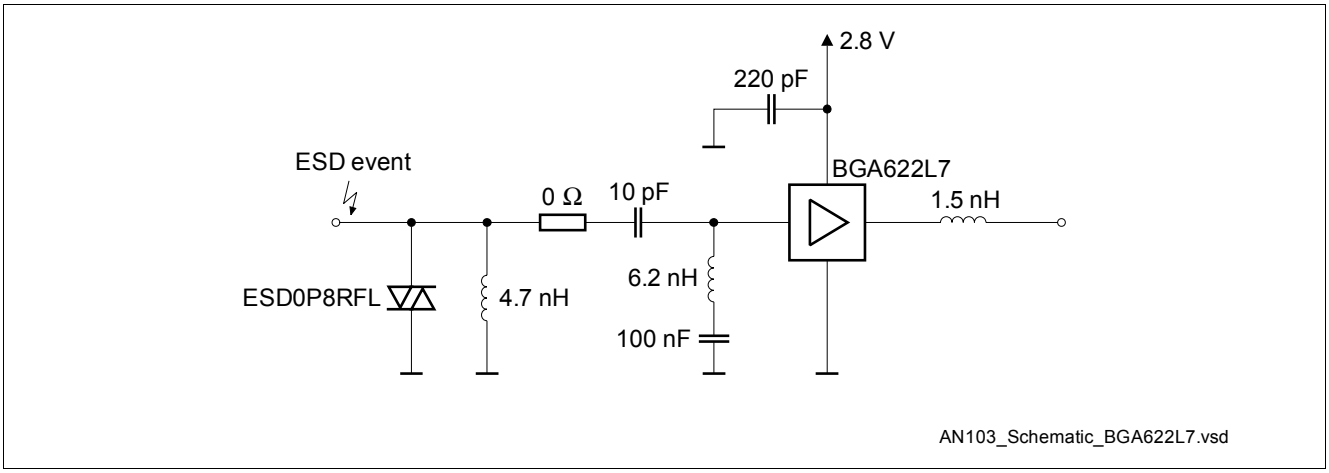

Figure 21 Schematic for S-DMB LNA with BGA622L7 and ESD protection

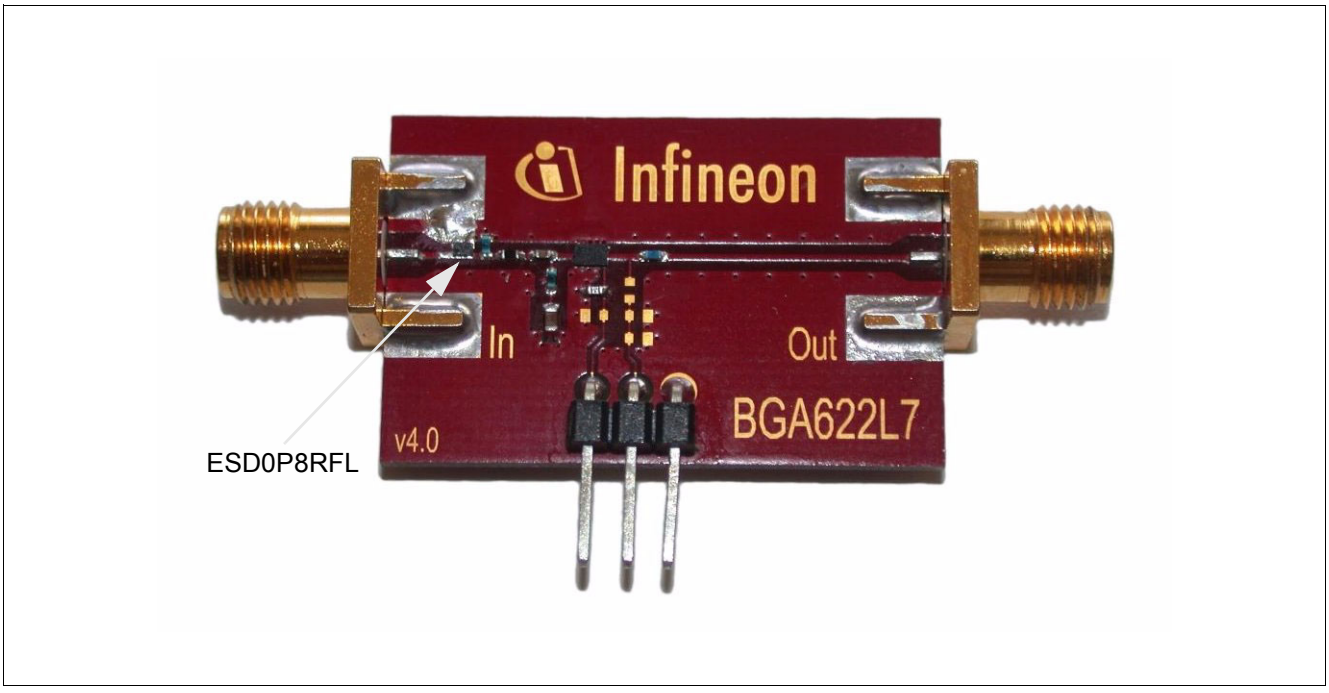

Figure 22 Photo of BGA622L7 application board with ESD0P8RFL protection diode

Table 5 Electrical characteristics of BGA622L7 with ESD protection for S-DMB. T_A = 25°C, V_{CC} = 2.75V, f = 2642.5MHz (unless noted otherwise)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply current	I_{CC}		5.5		mA	
Gain	$\|S_{21}\|^2$		15.9		dB	
Input return loss	RL_{IN}		10.3		dB	
Output return loss	RL_{OUT}		12		dB	
Reverse isolation	I_{REV}		26		dB	
Noise figure	F		1.35		dB	Including SMA connector and PCB losses of evaluation board
Input 1dB compression point	IP_{1dB}		-17		dBm	f = 2630 MHz
Input 3rd order intercept point	IIP_3		3		dBm	f_1 = 2630 MHz, f_2 = 2631 MHz P_{IN} = -30 dBm

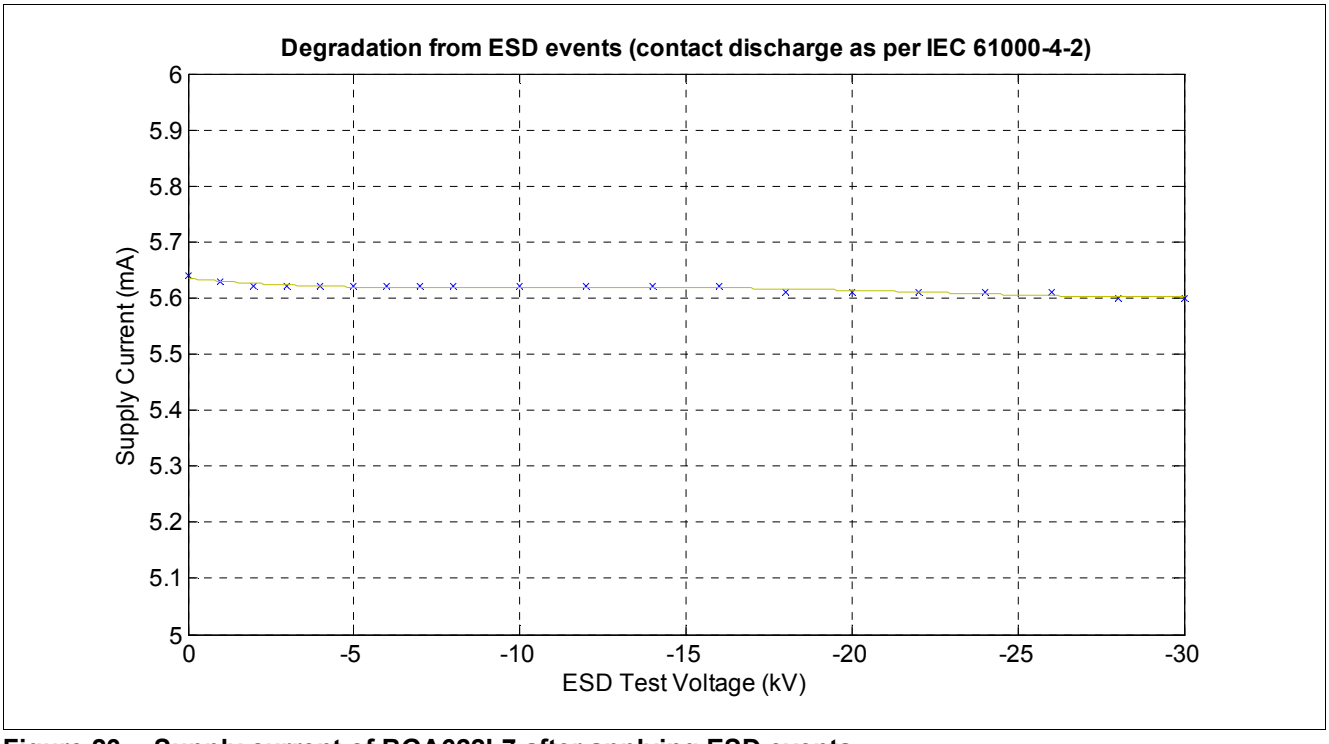

Figure 23 Supply current of BGA622L7 after applying ESD events

7 Conclusion

We have seen that system-level tests as per the IEC 61000-4-2 specification make greater demands on the ESD robustness than device-level tests as per the JESD22-A114D specification (HBM) and that test results from both specifications are not directly comparable. In discussing some basic concepts of ESD protection using either fast switching PIN-diodes or Zener-diodes optimized for high currents, we have shown that both the anti-parallel and the rail-to-rail configuration of fast switching PIN-diodes offers the lowest capacitance and are therefore the preferred configuration when it comes to RF antenna protection. A comparison between Infineon's low-capacitance ESD0P8RFL protection diode, a low-capacitance varistor and a polymer-based ESD protection device has shown considerable differences in ESD protection capabilities with Infineon's ESD0P8RFL to reign supreme. Polymer-based ESD protection devices suffer from high trigger voltages of typically 300 V or more and low-capacitance varistors suffer from high clamping voltages of quite a few 100 V. **Table 6** gives an overview on the ESD protection capabilities of low-capacitive ESD protection devices. Even though the ESD protection diode has the highest capacitance out of the three devices, this does not influence the RF performance as it was shown in **Chapter 6**. Next we have observed that failures from ESD events result in changes in the supply current, which can easily be measured. However, since leakage currents are much smaller than collector currents, we should always take a safety margin of at least 30% into account in order to account for measurement uncertainty. Finally, two application examples, one for GPS using Infineon's BGA615L7 and one for S-DMB using Infineon's BGA622L7, illustrated the ESD protection capability of Infineon's ESD0P8RFL protection diode in anti-parallel configuration. The results have shown that neither LNA shows significant changes in the supply current up to ±30 kV contact discharge as per IEC 61000-4-2 specification. Therefore, we can claim that level 4 (±8 kV contact protection) of IEC 61000-4-2 is satisfied with ESD0P8RFL without the slightest effort. With polymer-based ESD protection devices or even varistors level 4 can not be met.

Table 6 ESD protection capability of low-capacitive ESD protection devices

ESD Protection Device	Capacitance (typ.) (pF)	ESD Protection
Infineon ESD0P8RFL	0.8	++
Polymer-based ESD protection	0.1	-
Varistor	0.5	--

Please, feel free to contact Infineon's ESD application experts for further recommendations and technical support.

References

[1] IEC 61000-4-2, Electromagnetic Compatibility (EMC) Part 4: Testing and measurement techniques – Section 2: "Electrostatic discharge immunity test," International Electrotechnical Commission, 1995.

[2] JESD22-A114D, "Electrostatic Discharge (ESD) sensitivity testing Human Body Model (HBM)," JEDEC Solid State Technology Association, March 2006.