Application Note No. 089

The BGA622L7 Silicon-Germanium Universal Low Noise Amplifier MMIC in UMTS Receiver Application

RF & Protection Devices

Never stop thinking

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Page	Subjects (major changes since last revision)
All	Document layout change

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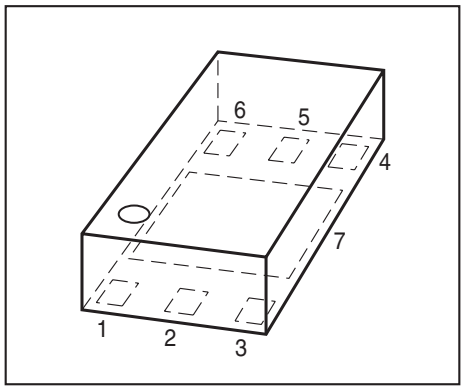
1 The BGA622L7 Silicon-Germanium Universal Low Noise Amplifier MMIC in UMTS Receiver Applications

Features

- Versatile, easy-to-use LNA MMIC in 70 GHz f_T SiGe technology.
- 50 Ohm matched output, pre-matched input
- Integrated output DC blocking capacitor, integrated RF choke on internal bias network
- Low current consumption of 6 mA
- “Shutdown” or “Sleep” mode
- Unconditionally stable
- Low external component count
- Ultra small TSLP-7-1 package
- Exceptional noise figure: 1.1 dB at 2.1 GHz



Applications

- Low Noise Amplifier for 800 / 900 MHz, GSM900, 900 MHz ISM, DCS1800, GPS, 1900 MHz PCS, 2.1 GHz UMTS, Bluethooth and 2.4 GHz Wireless LAN

1.1 Introduction

The BGA622L7 is an easy-to-use, versatile and flexible low-cost Low Noise Amplifier (LNA) MMIC designed for the high linearity and sensitivity requirements of existing and next - generation wireless applications including GSM, 900 MHz ISM, GPS, UMTS and Wireless LANs. The BGA622L7 is housed in the ultra-small TSLP-7-1 package consuming less PCB space while providing more gain compared to BGA622. Based on Infineon’s cost-effective 70 GHz f_T Silicon-Germanium (SiGe) B7HF bipolar process technology, the BGA622L7 offers a 1.1 dB noise figure and 16 dB of gain at 2.1 GHz for high performance, cost-effective mobile communications applications. BGA622L7 offers impressive noise figure performance, particularly for a low-cost, integrated MMIC. In the past, in-circuit noise figure approaching 1.0 dB at 2 GHz were possible only for more expensive GaAs-based, fully discrete solutions utilizing narrowband impedance matching and higher external parts count. The BGA622L7 combines the excellent noise figure advantages of a high-performance discrete solution with the easy-to-use, low parts count, and diminished risk and reduced system development time made possible by a MMIC approach.

The new LNA incorporates a 50 Ω matched output with an integrated output DC blocking capacitor. The broadband output match simplifies integration issues with external image-stripping filters. The input is pre-matched, requiring an external RF choke on the voltage supply pin. The noise figure of BGA622L7 is relatively insensitive to the input impedance matching approach taken by the end user, reducing development time and risk. A low supply current of 6 mA at 2.75 V and an integrated on / off feature provides for low power consumption and increased stand by time for 3 G cellular handsets or other portable, battery-operated wireless applications.

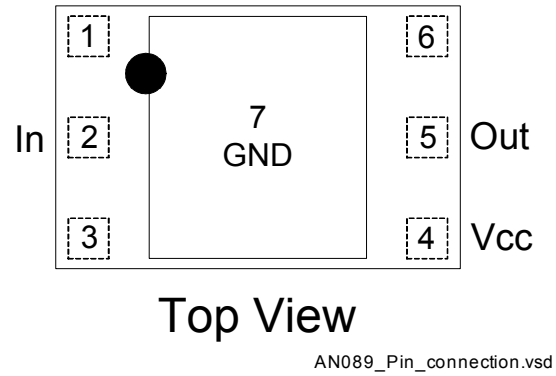


Figure 1 Pin Connection

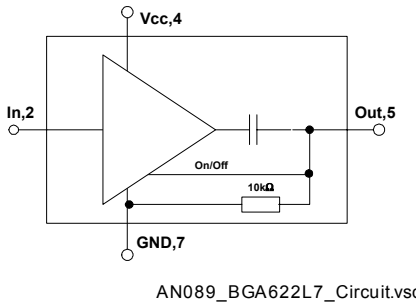


Figure 2 BGA622L7's Equivalent Circuit

1.2 Overview

The BGA622L7 is shown in three different configurations for the UMTS frequency band between 2.11 GHz and 2.17 GHz:

- Configuration A: minimum parts count
- Configuration B: BGA622L7 with increased IIP_3
- Configuration C: BGA622L7 with increased IIP_3 and power down option

Table 1 shows the measured performance of these three circuits. All measurement values presented in this application note include losses of both PCB and connectors - in other words, the reference planes used for measurements are the PCB's RF SMA connectors. Please note that noise figure and gain results shown do not have any PCB loss extracted from them. Removing the effects of the connectors' and the PCB's loss would result in an increase of gain of about 0.4 dB and a decrease of noise figure of about 0.2 dB.

Table 1 Performance Overview

Parameter	Configuration A	Configuration B	Configuration C
Supply voltage	2.75 V	2.75 V	2.75 V
Supply current	5.7 mA	5.7 mA	5.7 mA
Gain	16.2 dB	16.1 dB	16.2 dB
Noise figure	1.35 dB	1.35 dB	1.35 dB
Input return loss	11.1 dB	12.0 dB	12.0 dB
Output return loss	9.4 dB	9.8 dB	9.3 dB

Table 1 Performance Overview (cont'd)

Parameter	Configuration A	Configuration B	Configuration C
Reverse Isolation	26.3 dB	26.4 dB	26.3 dB
Input compression point	-17.5 dB	-17.5 dB	-17.5 dBm
Input 3rd order intercept point, on state[1)]	-10 dB	0 dB	0 dB
Insertion loss, power down	-	-	21.4 dB
Input 3rd order intercept point power down[2)]	-	-	20 dBm

1) -35 dBm per tone, Δf = 1 MHz

2) -10 dBm per tone, Δf = 1 MHz

All values displayed are measured at 2.14 GHz if not otherwise noted.

2 Configuration A

The circuit in **Figure 3** shows the minimum parts count version of a BGA622L7 LNA. There are only three external elements necessary. A DC blocking capacitor at the output and a coil at the power supply are already integrated on chip.

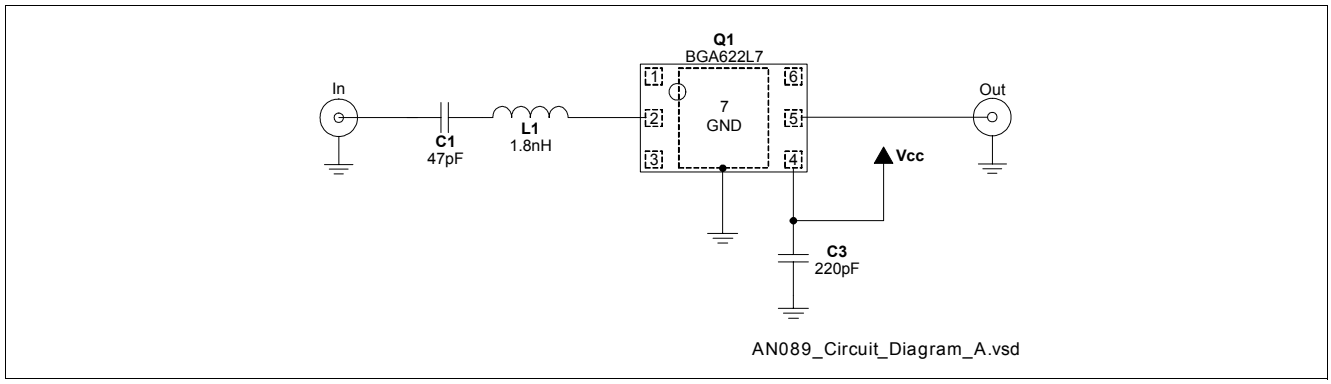


Figure 3 Circuit Diagram of Configuration A

Table 2 Bill of Materials of Configuration A

Name	Value	Unit	Package	Manufacturer	Function
C1	47	pF	0402	Various	DC block, helps noise matching
C3	220	pF	0402	Various	RF bypass
L1	1.8	nH	0402	Toko LL1005-FH	Input matching
Q1	BGA622L7		TSLP-7-1	Infineon Technologies	SiGe MMIC

2.1 Measurements for Configuration A

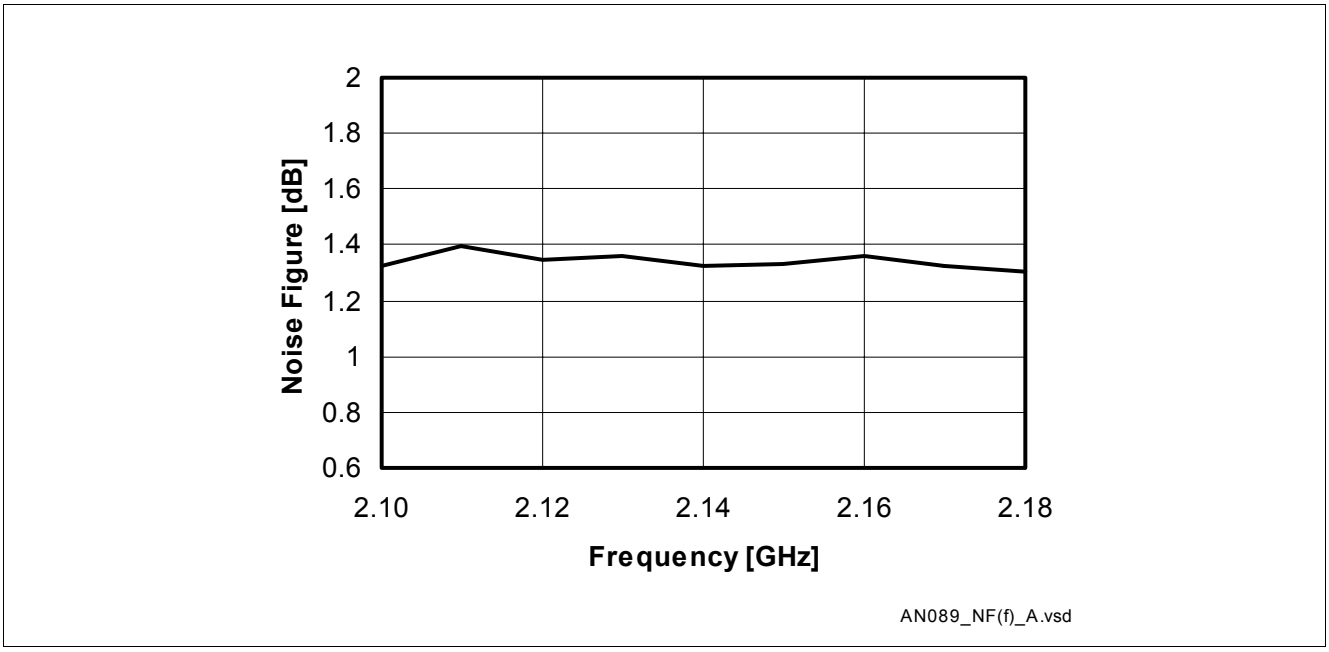


Figure 4 Noise figure Configuration A

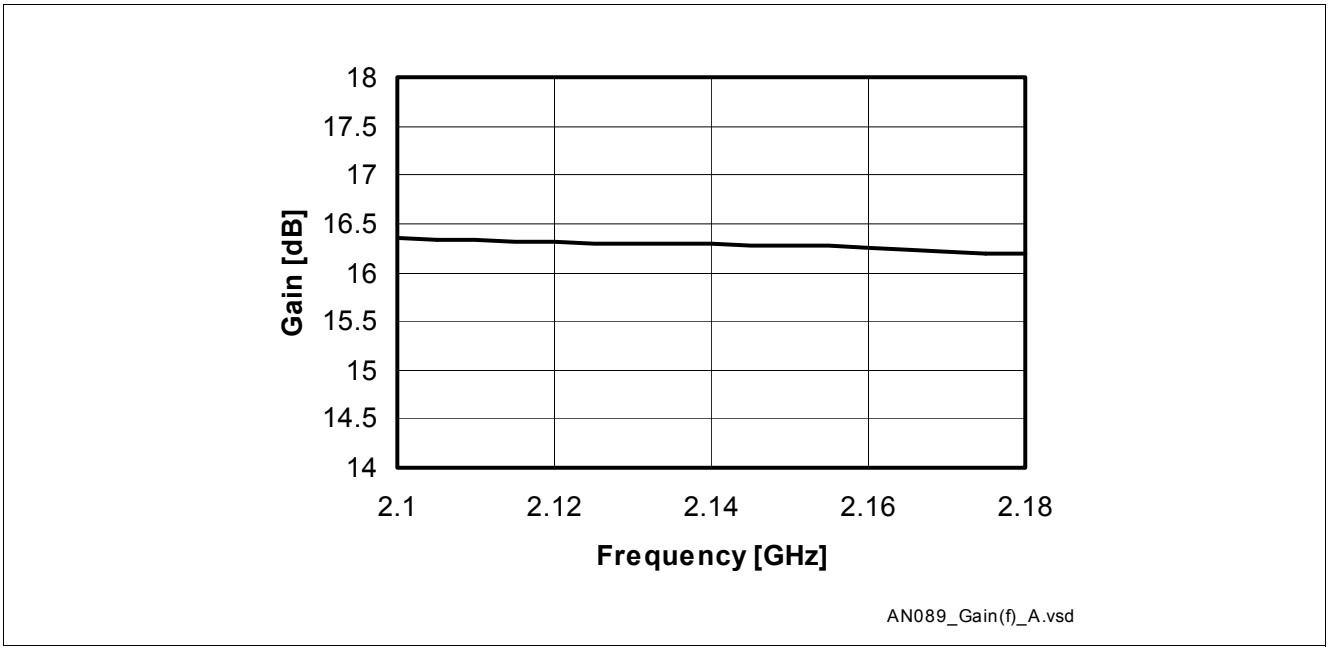


Figure 5 Gain Configuration A

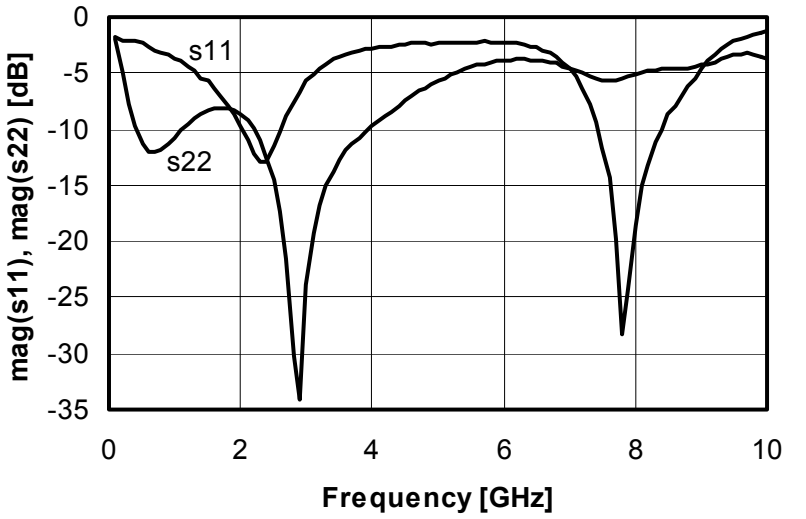


Figure 6 Return Loss Configuration A

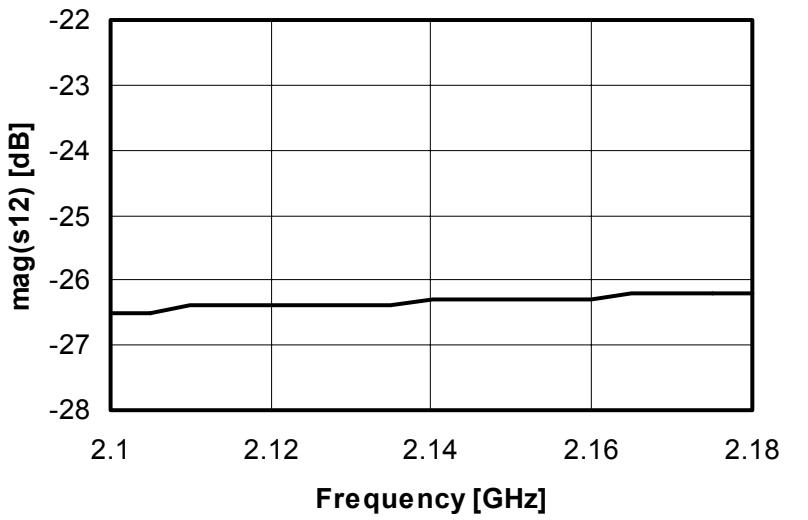


Figure 7 Reverse Isolation Configuration A

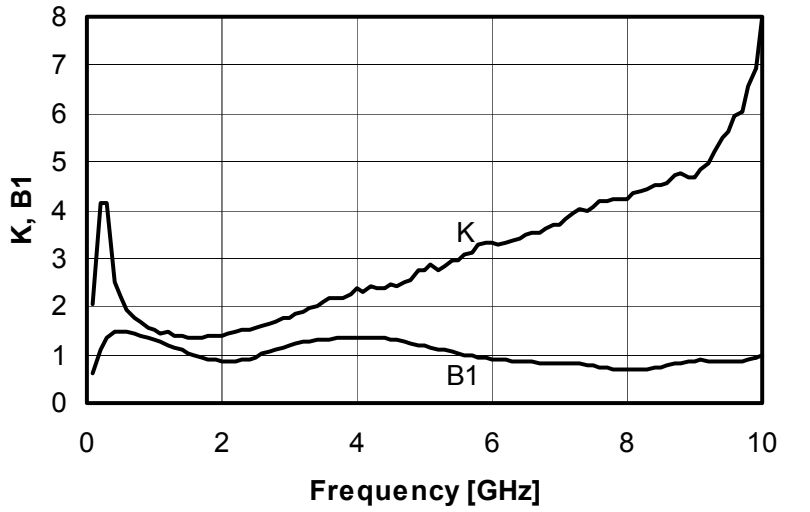


Figure 8 Stability Factor K and Stability Measure B1 of Configuration A

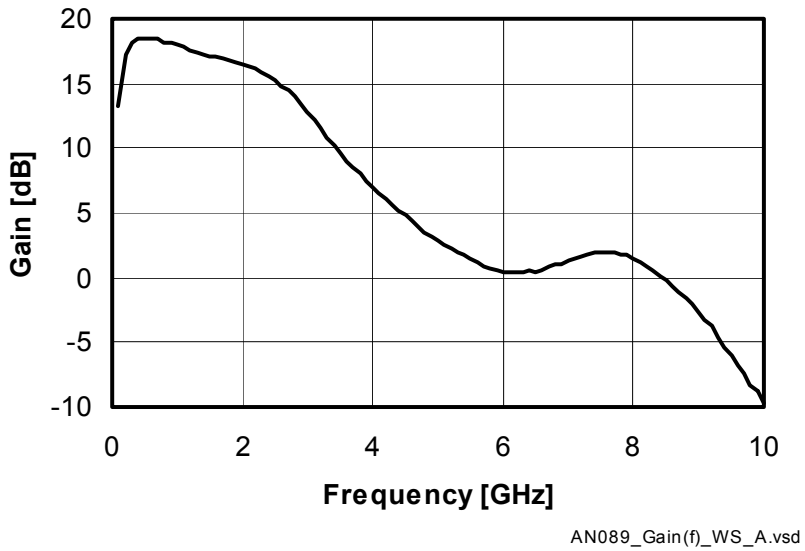


Figure 9 Wide Span Gain Configuration A

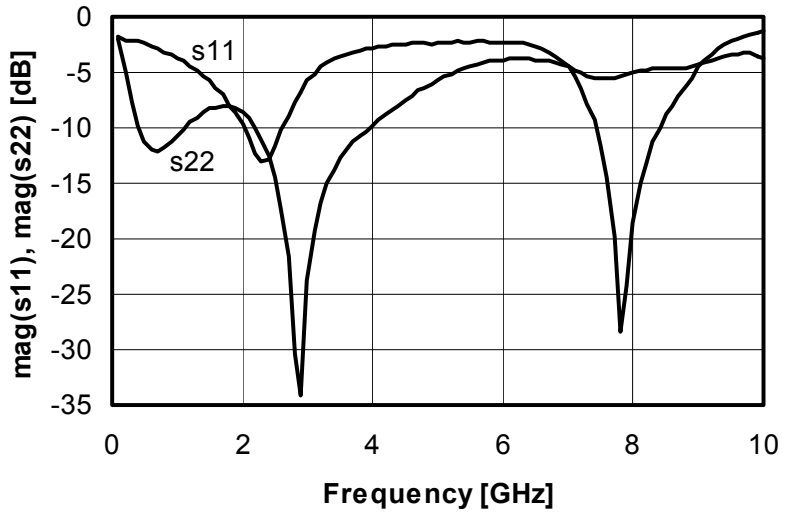


Figure 10 Wide Span Return Loss Configuration A

3 Configuration B

The circuit in **Figure 11** shows a way to increase the input 3rd order intercept point of BGA622L7. L2 and C2 offer low-frequency intermodulation products a low impedance path to ground. This prevents them from modulating the base voltage of the BGA622L7's internal RF transistor and thus linearity is improved. Typically the input 3rd-order intercept point of BGA622L7 can be improved by 6 to 10 dB in this manner.

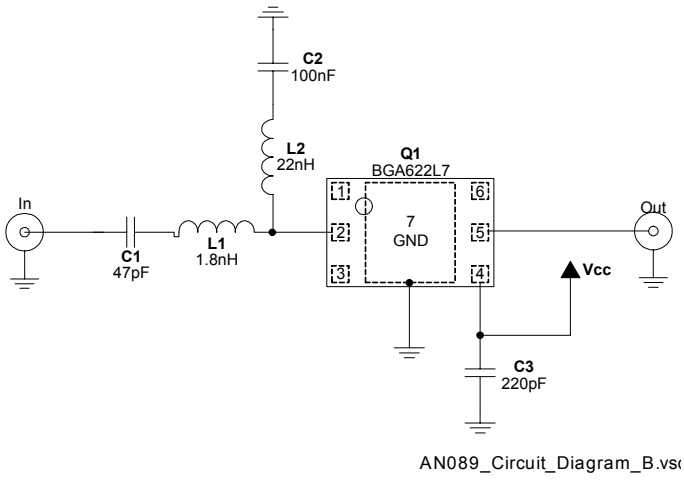


Figure 11 Circuit Diagram Configuration B

Table 3 Bill of Materials of Configuration B

Name	Value	Unit	Package	Manufacturer	Function
C1	47	pF	0402	Various	DC block, helps noise matching
C2	100	nF	0603	Various	IIP_3 improvement
C3	220	pF	0402	Various	RF bypass

Table 3 Bill of Materials of Configuration B (cont'd)

Name	Value	Unit	Package	Manufacturer	Function
L1	1.8	nH	0402	Toko LL1005-FH	Input matching
L2	22	nH	0402	Toko LL1005-FH	RF choke
Q1	BGA622L7		TSLP-7-1	Infineon Technologies	SiGe MMIC

3.1 Measurements of Configuration B

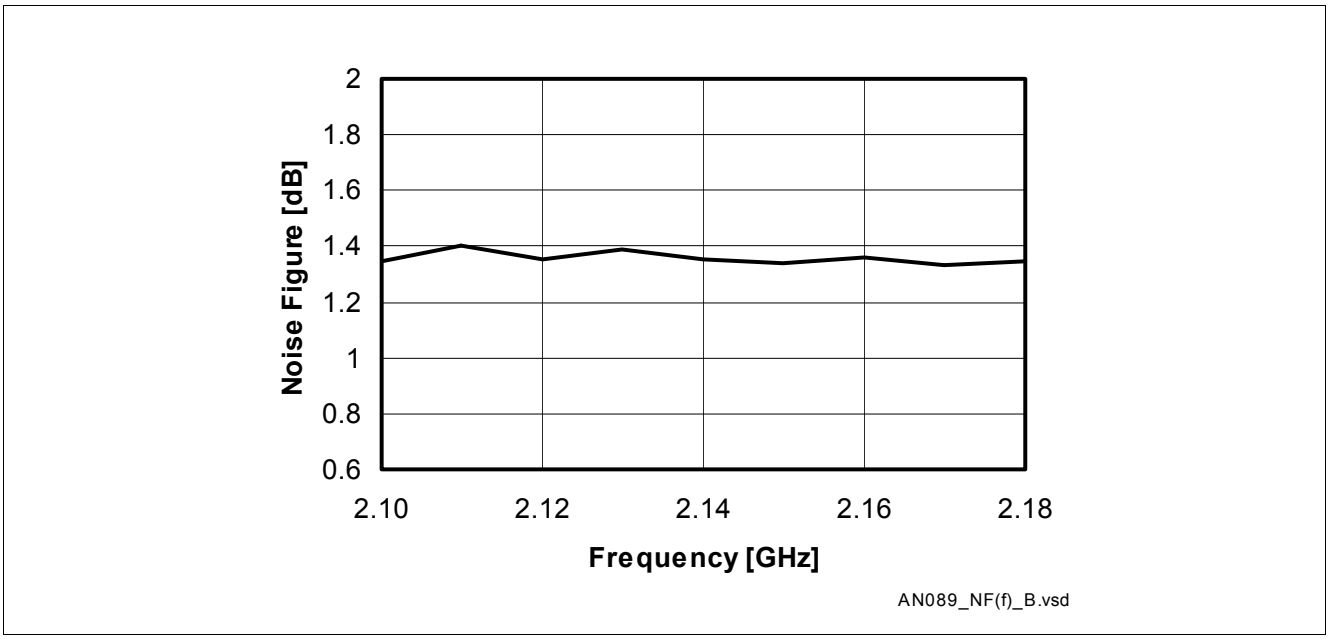


Figure 12 Noise figure Configuration B

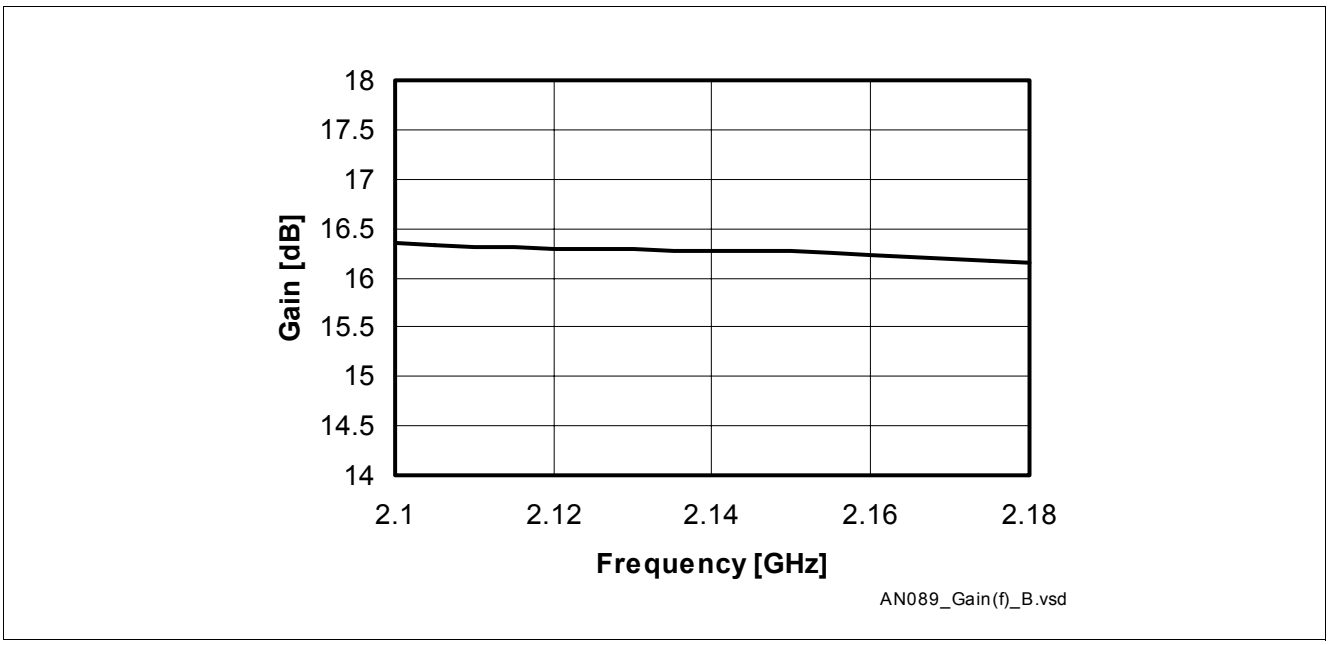


Figure 13 Gain Configuration B

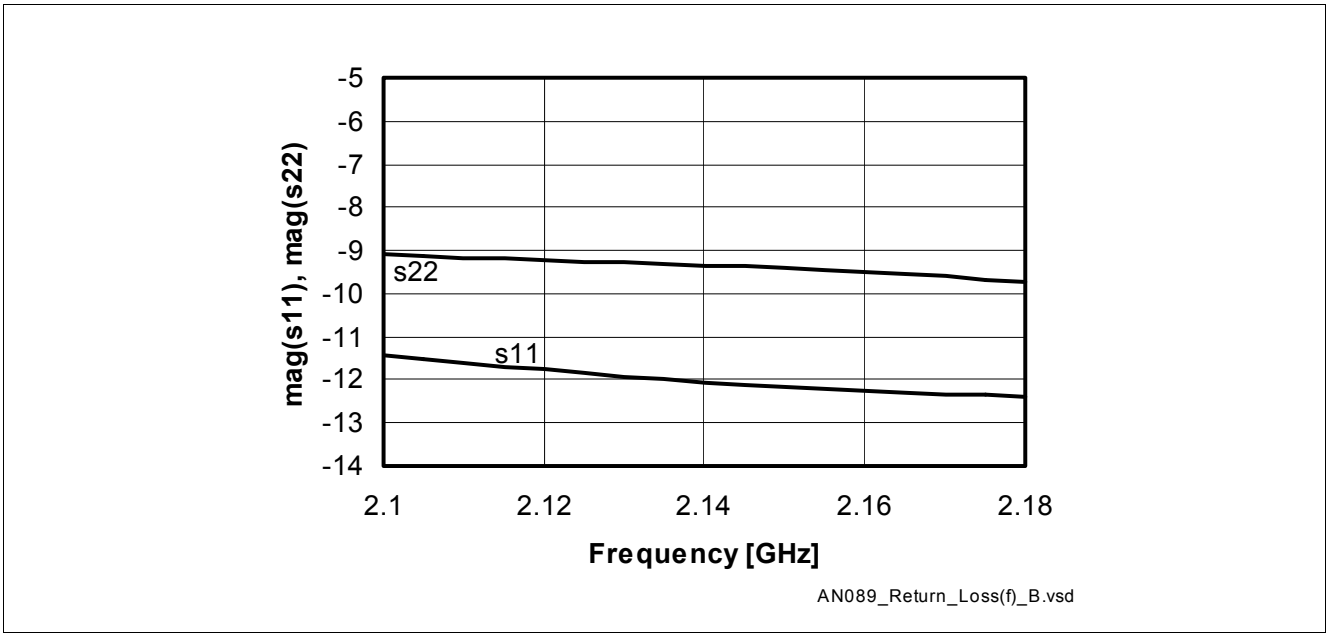


Figure 14 Return Loss Configuration B

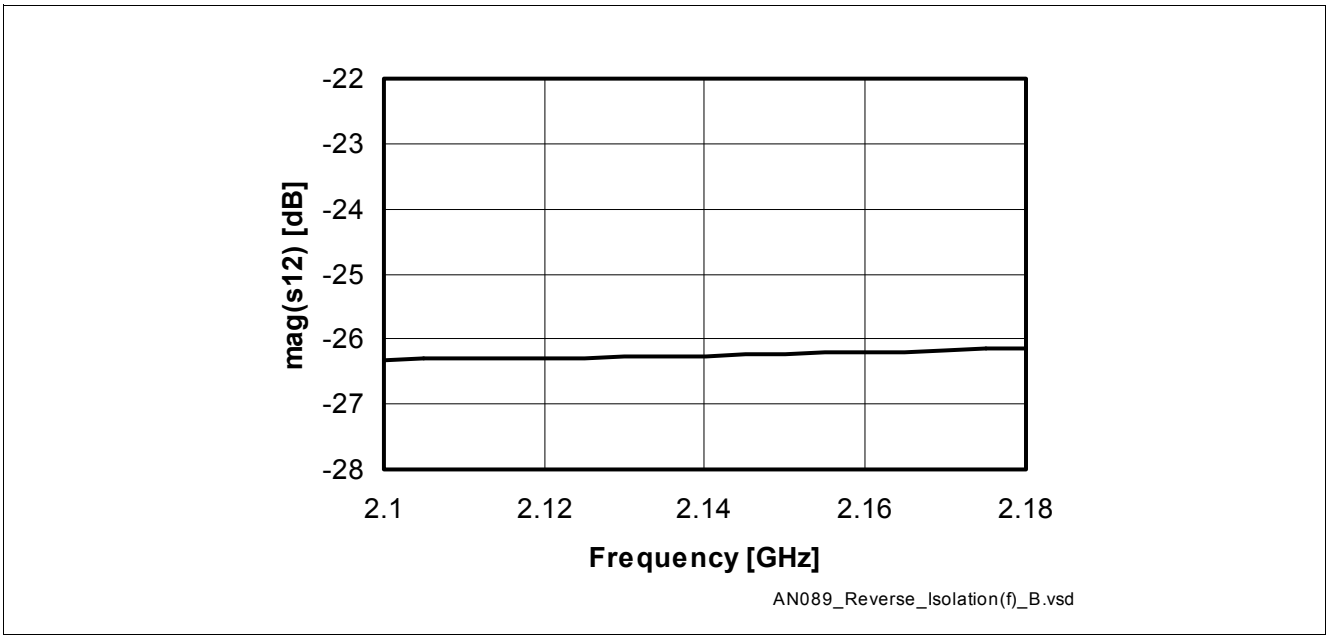


Figure 15 Reverse Isolation Configuration B

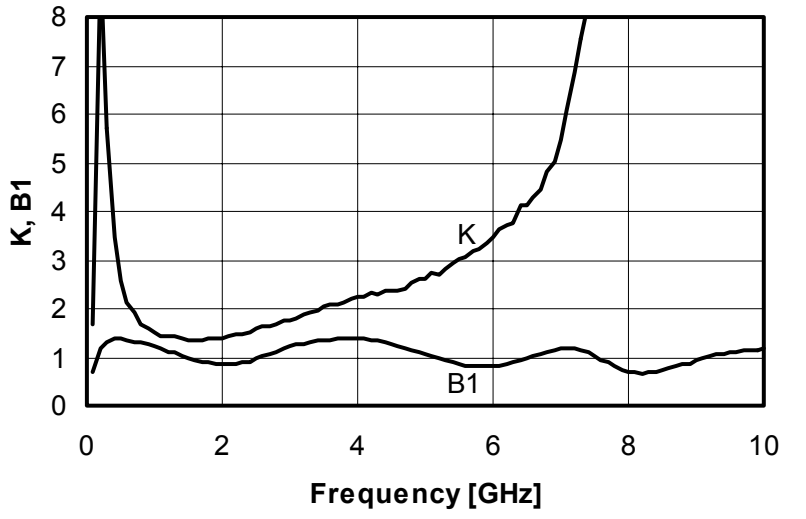


Figure 16 Stability Factor K and Stability Measure B1 of Configuration B

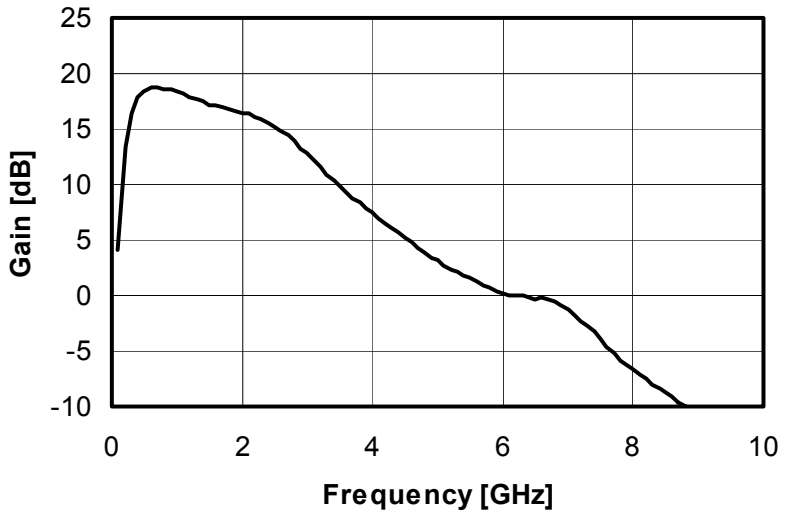


Figure 17 Wide Span Gain Configuration B

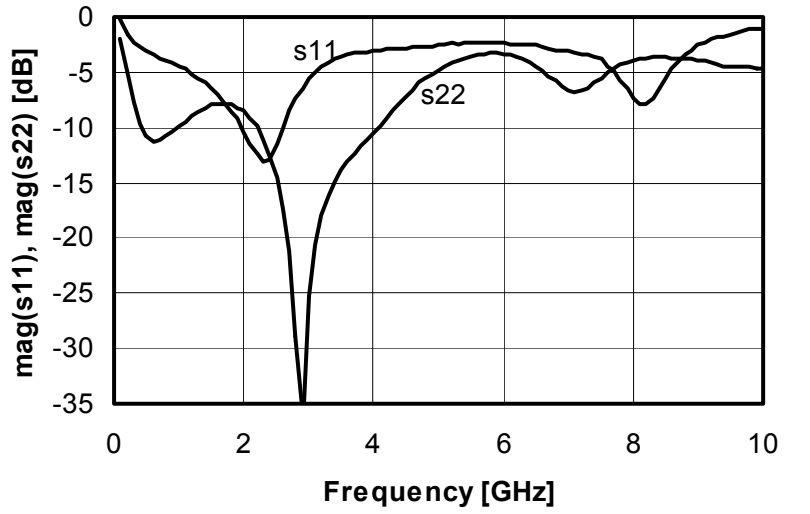


Figure 18 Wide Span Return Loss Configuration B

4 Configuration C

Figure 19 shows a BGA622L7 LNA with available power down mode. In the BGA622L7, an internal high-impedance path exists around the device's internal output DC blocking capacitor, between the output pin and the device's internal shutdown circuitry. Applying VCC at the Output pin (pin 5) will switch off the BGA622L7 and only a small supply current of about 0.26 mA flows into the device in shutdown mode. The schematic shows the "PD" (Power Down) connection where the shutdown signal may by applied. Ground or an open circuit at the PD pin will turn on the device. Note that if the Power Down feature is employed, the internal DC blocking capacitor of the BGA622L7 is bypassed by external circuitry, and therefore some sort of external DC blocking at the output must be employed. This can be either an external output DC blocking capacitor, or the usual image-stripping filter, provided the input of the filter presents a DC open circuit.

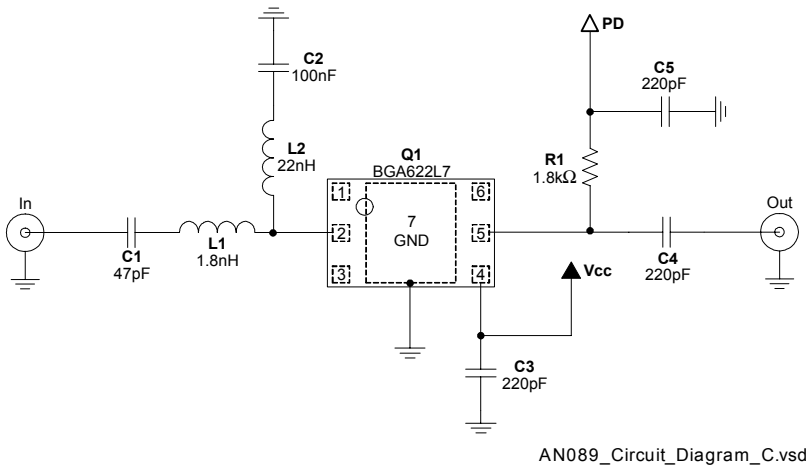


Figure 19 Circuit Diagram Configuration C

Table 4 Bill of Materials of Configuration C

Name	Value	Unit	Package	Manufacturer	Function
C1	47	pF	0402	Various	DC block, helps noise matching
C2	100	nF	0603	Various	IIP_3 improvement
C3	220	pF	0402	Various	RF bypass
C4	220	pF	0402	Various	DC block
C5	220	pF	0402	Various	RF bypass
L1	1.8	nH	0402	Toko LL1005-FH	Input matching
L2	22	nH	0402	Toko LL1005-FH	RF choke
R1	1.8	kΩ	0402	Various	RF choke
Q1	BGA622L7		TSLP-7-1	Infineon Technologies	SiGe MMIC

4.1 Measurements of Configuration C

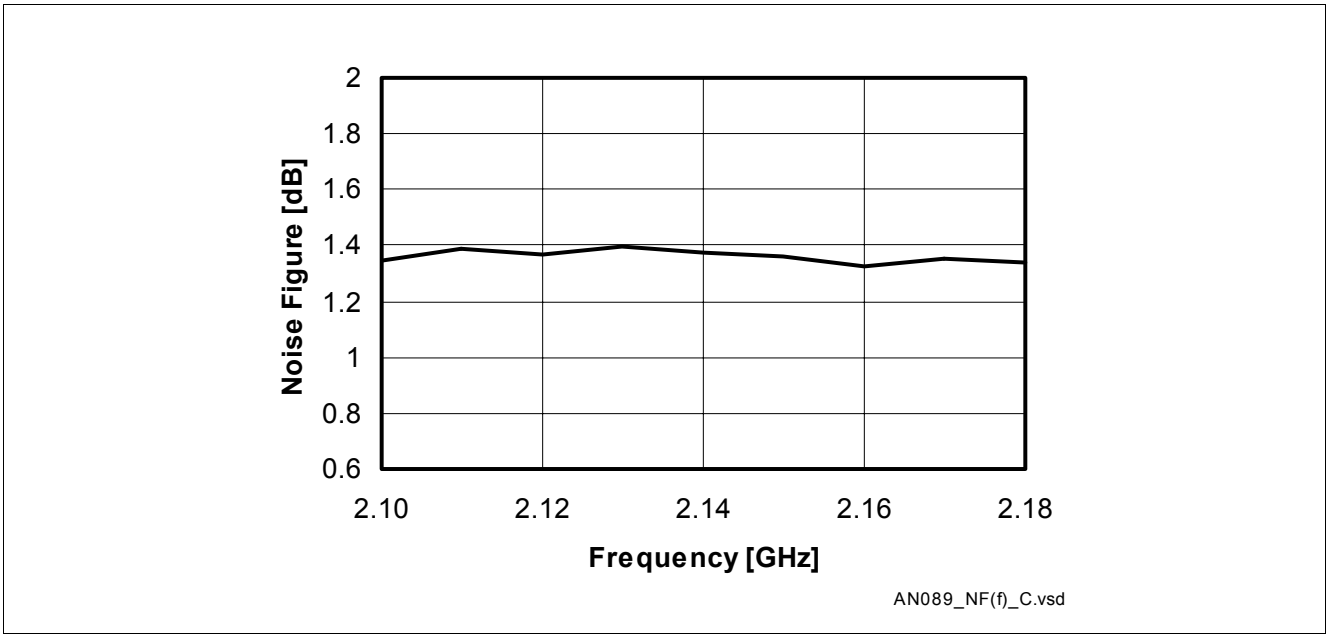


Figure 20 Noise figure Configuration C

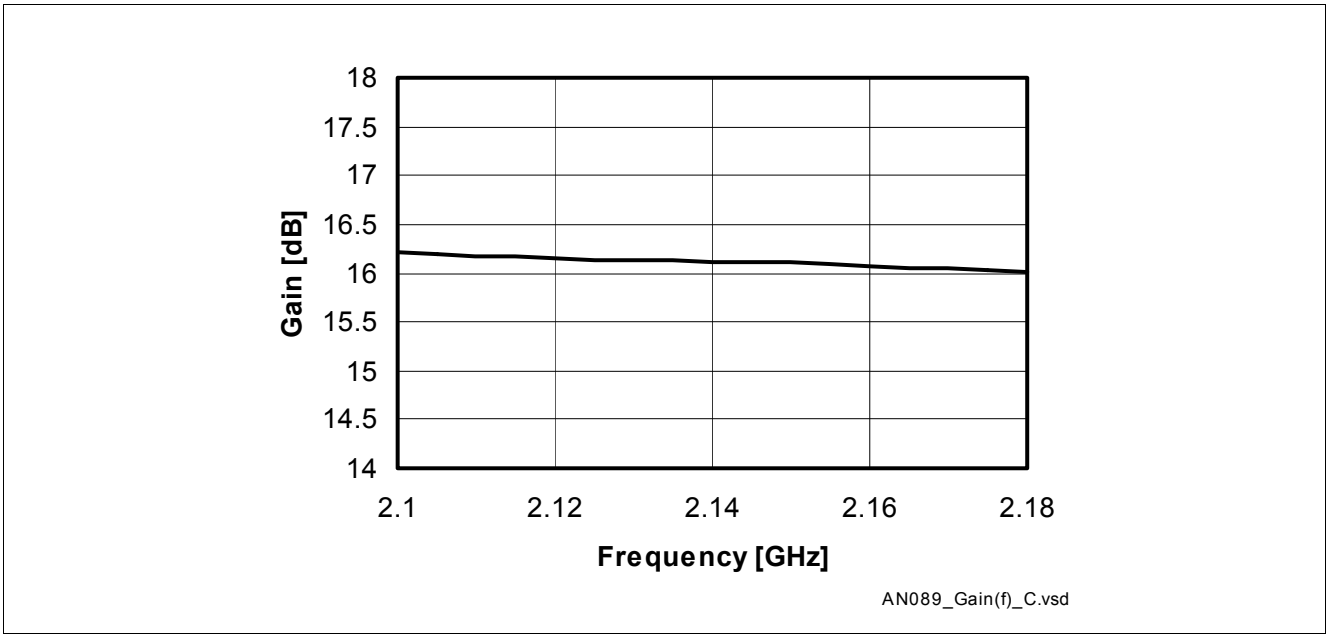


Figure 21 Gain Configuration C

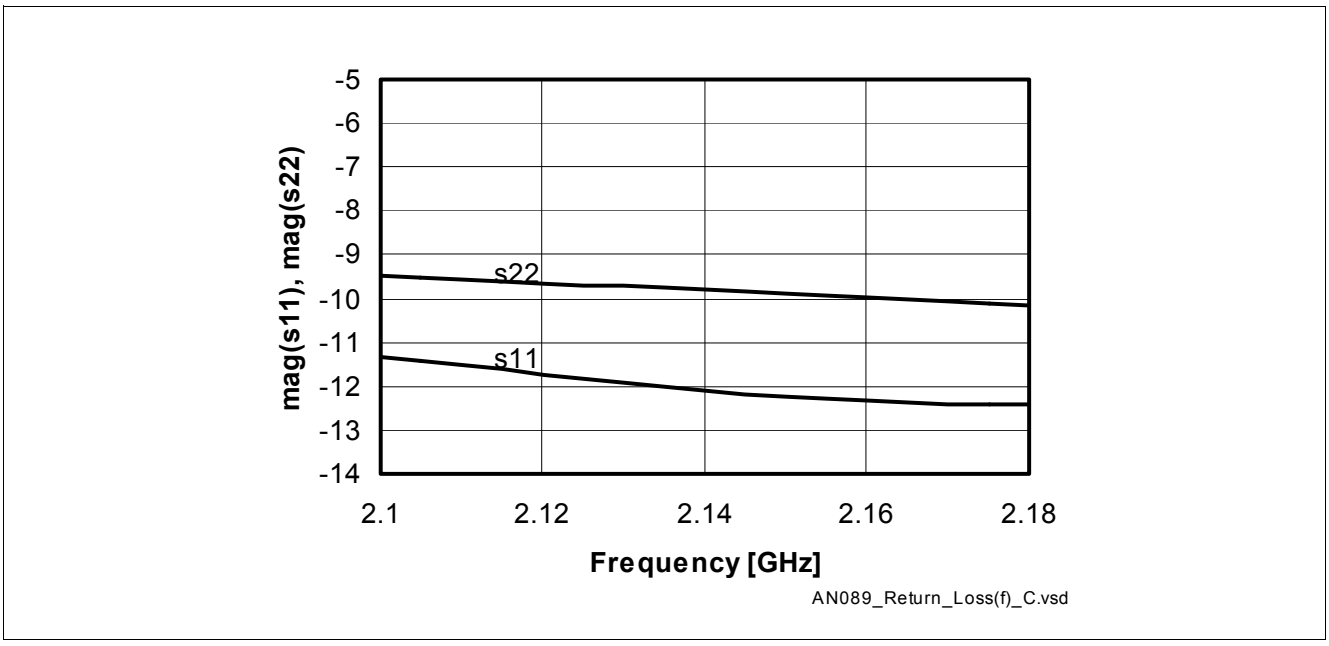


Figure 22 Return Loss Configuration C

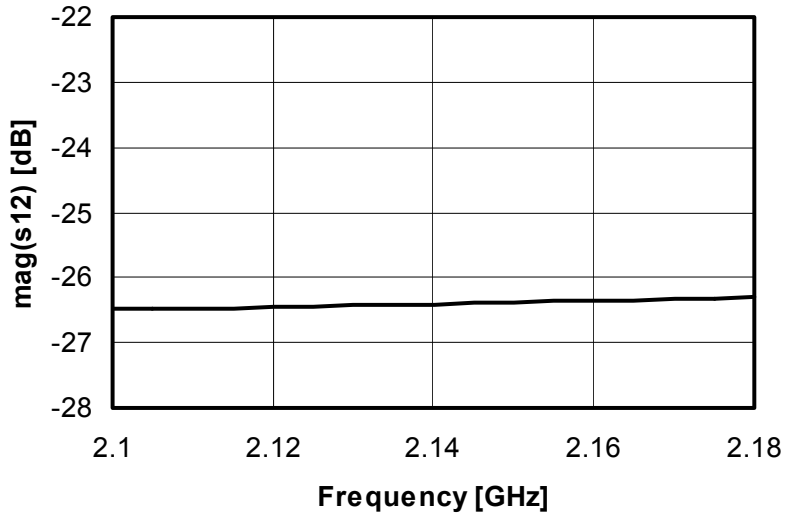


Figure 23 Reverse Isolation Configuration C

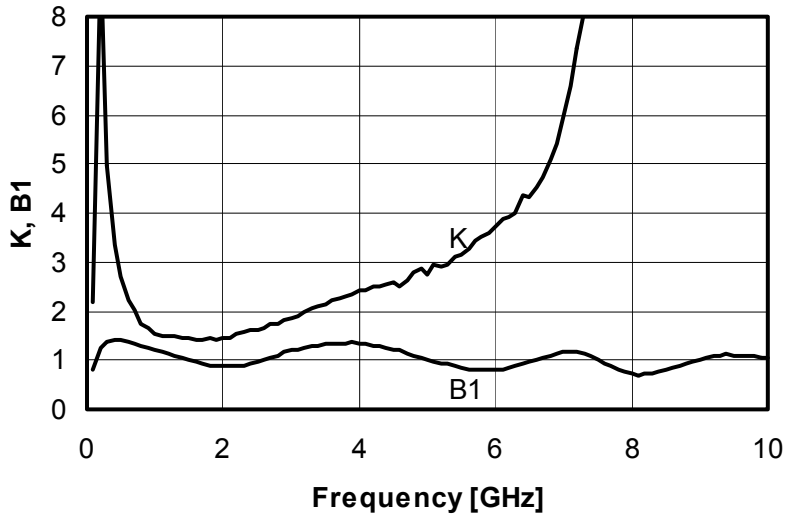


Figure 24 Stability Factor K and Stability Measure B1 of Configuration C

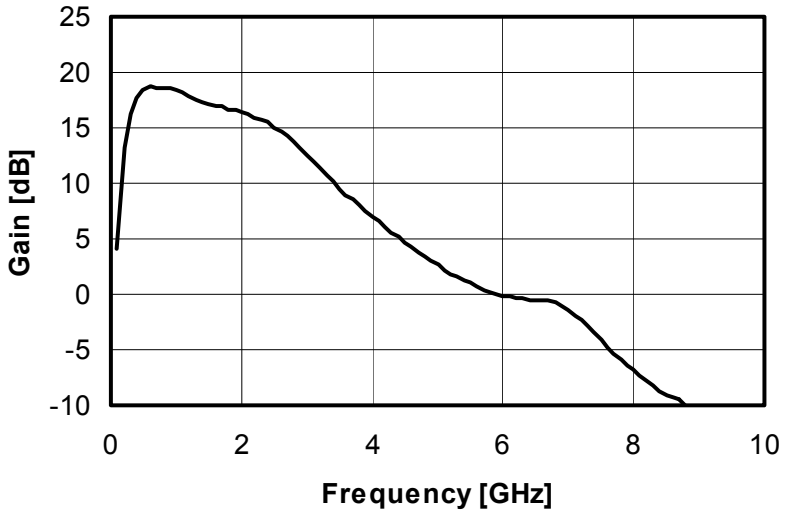


Figure 25 Wide Span Gain Configuration C

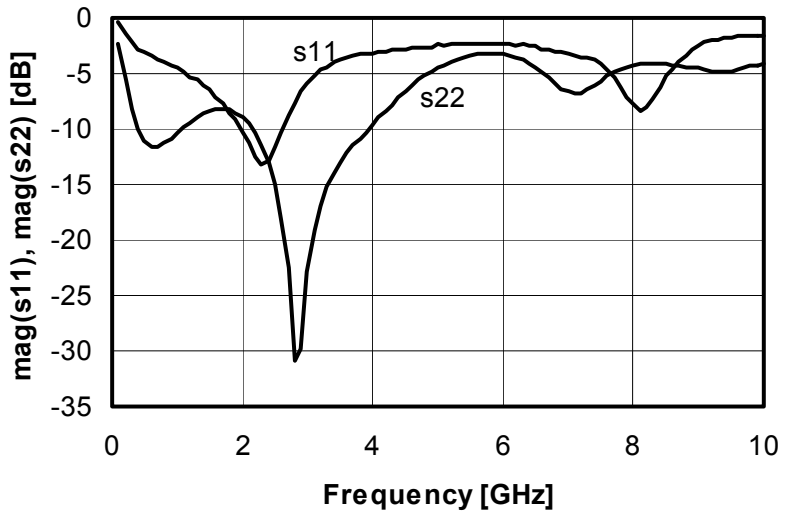


Figure 26 Wide Span Return Loss Configuration C

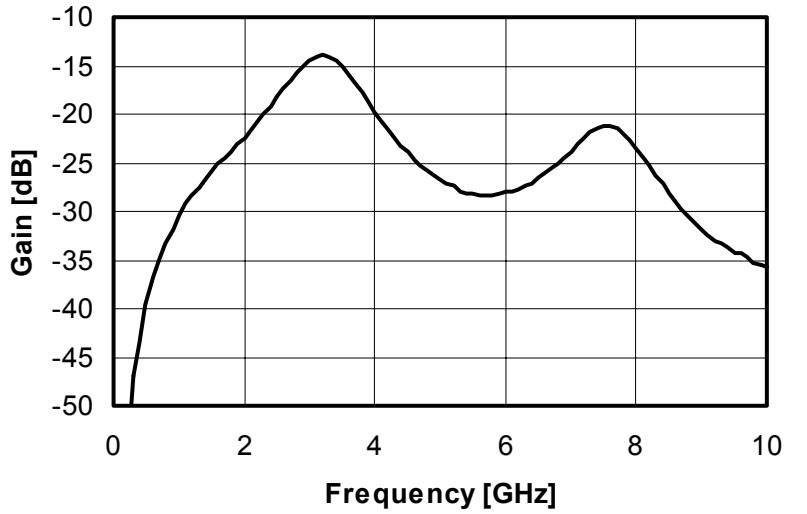


Figure 27 Forward Transmission in Power Down Mode

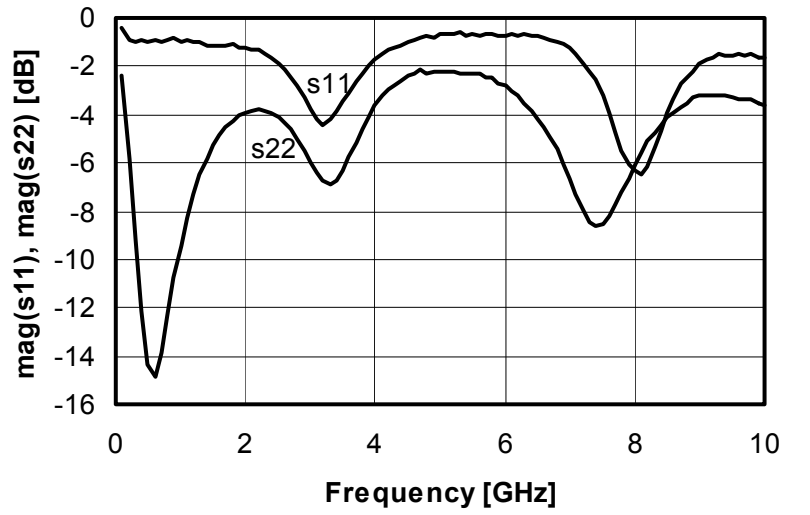


Figure 28 Input and Output Return Loss in Power Down Mode

5 Application PCB

Figure 29 shows the placement of the specific components on the PCB. The Test-pin is not used in this application. It is only provided in case someone wants to access the input of the BGA622L7 for testing purposes.

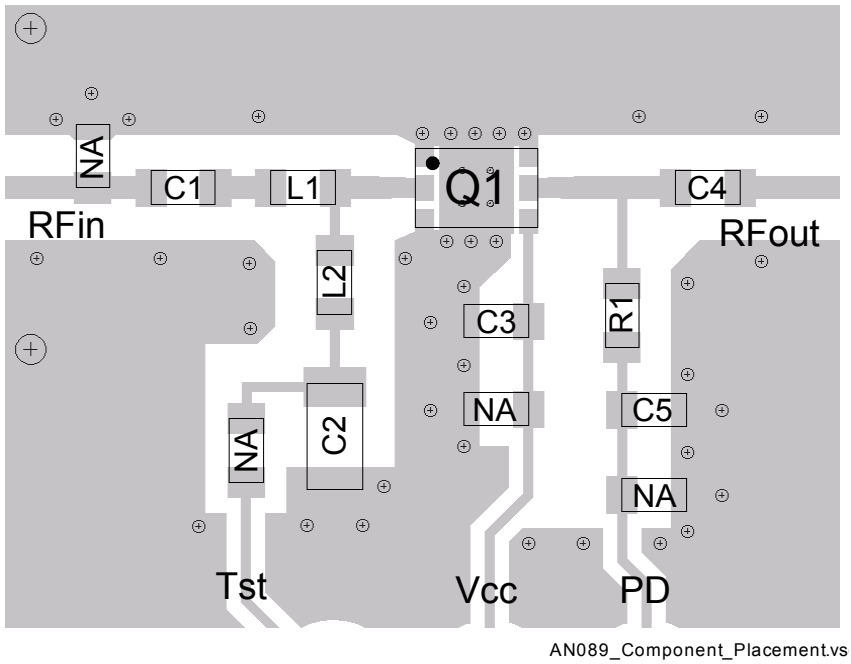


Figure 29 Component Placement on Application PCB

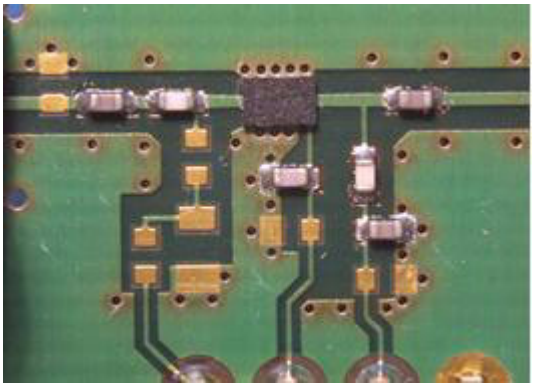


Figure 30 Zoom-in on a PCB with input matching and power down option

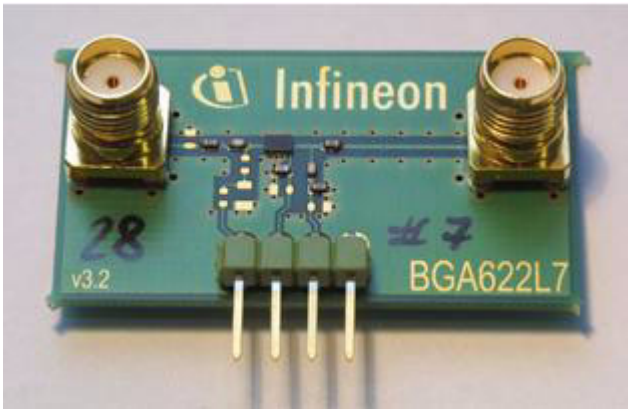


Figure 31 Application PCB

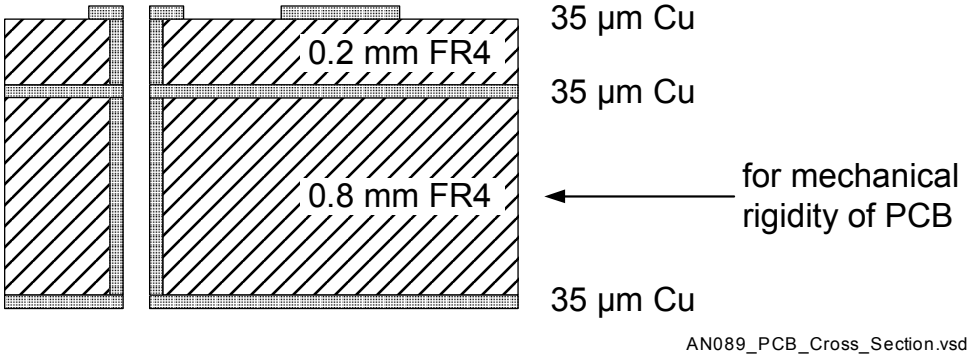


Figure 32 PCB Cross Section

Evaluation boards for the LNA applications described in this application note are available from Infineon Technologies.