

Application Note No. 075

High Third-Order Input Intercept Point CDMA 800
Low Noise Amplifier

RF & Protection Devices



Never stop thinking

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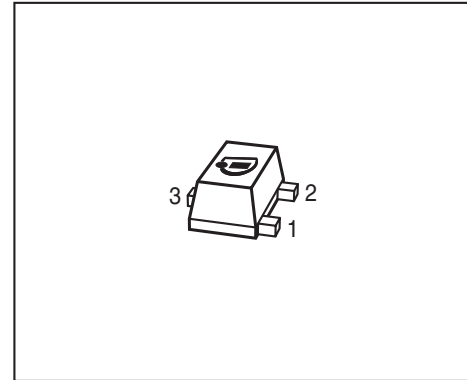
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Page	Subjects (major changes since last revision)
All	Document layout change

High Third-Order Input Intercept Point CDMA 800 Low Noise Amplifier

Features

- Extremely high IIP_3 of 10 dB at 850 MHz associated with a low current consumption
- High overall performance at extraordinarily low cost



Introduction

The BFR380F is a silicon bipolar transistor housed in a small outline TSFP-3 package. The BFR380F is a member of Infineon's new 3+ generation transistor family consisting of three different sizes of transistors: BFR340F, BFR360F and BFR380F. These transistors are 14 GHz transition-frequency devices which take advantage of the latest manufacturing techniques requiring fewer processing steps than other devices in their class, thereby offering excellent performance and device-to-device consistency at extraordinarily low cost. All types of 3+ transistors are also available in Infineon's new TSLP-3 package. The world's smallest chip size leadless plastic package for discrete components like diodes and transistors.

With a noise figure of 1.1 dB at 1800 MHz and a bias point of 3 V / 8 mA, the BFR380F is a good solution for cost-sensitive LNA designs. In addition, the BFR380F is an ideal choice for VCO applications due to its low flicker noise corner frequency of 15 kHz.

This application note describes the BFR380F as a CDMA 800 LNA for the frequency range between 830 MHz and 870 MHz. **Table 1** shows the measured performance of the application circuit. All parameters include losses of PCB and SMA connectors.

Table 1 Measured Performance at 850 MHz

Parameter	Value	Unit
Supply voltage	3	V
Supply current	8.2	mA
Gain	14.8	dB
Noise figure	1.1	dB
Input 3 rd order intercept point ¹⁾	10.5	dBm
Input return loss	14.4	dB
Output return loss	18.1	dB
Reverse isolation	20.2	dB
Input compression point	-9	dB

1) $\Delta f = 1$ MHz, -25 dBm per tone

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Application Circuit

Figure 1 shows the schematic of the application circuit. Input IP_3 is improved by different measures. The first one is inductive emitter degeneration where a microstrip line between emitter and ground enlarges the emitter inductance. This additional emitter feedback decreases gain and increases input IP_3 in about the same magnitude while output IP_3 remains at the same level. As a drawback increased emitter inductance destabilizes the device at higher frequencies so a careful look at the circuit's stability factor is necessary when applying emitter degeneration.

Another possibility to increase IP_3 on the whole is to provide low frequency paths to ground at base and collector to avoid AM modulation effects. At the base L1 and C1 form such a path at the transistor's base, the one at the collector consists of L2-R3-C3. In general the low frequency path at the base is the more efficient way to increase IP_3 . For more detailed information on increasing IP_3 by low frequency grounding please refer to Infineon's application note AN060 (BFP620) and AN057 (BFP540).

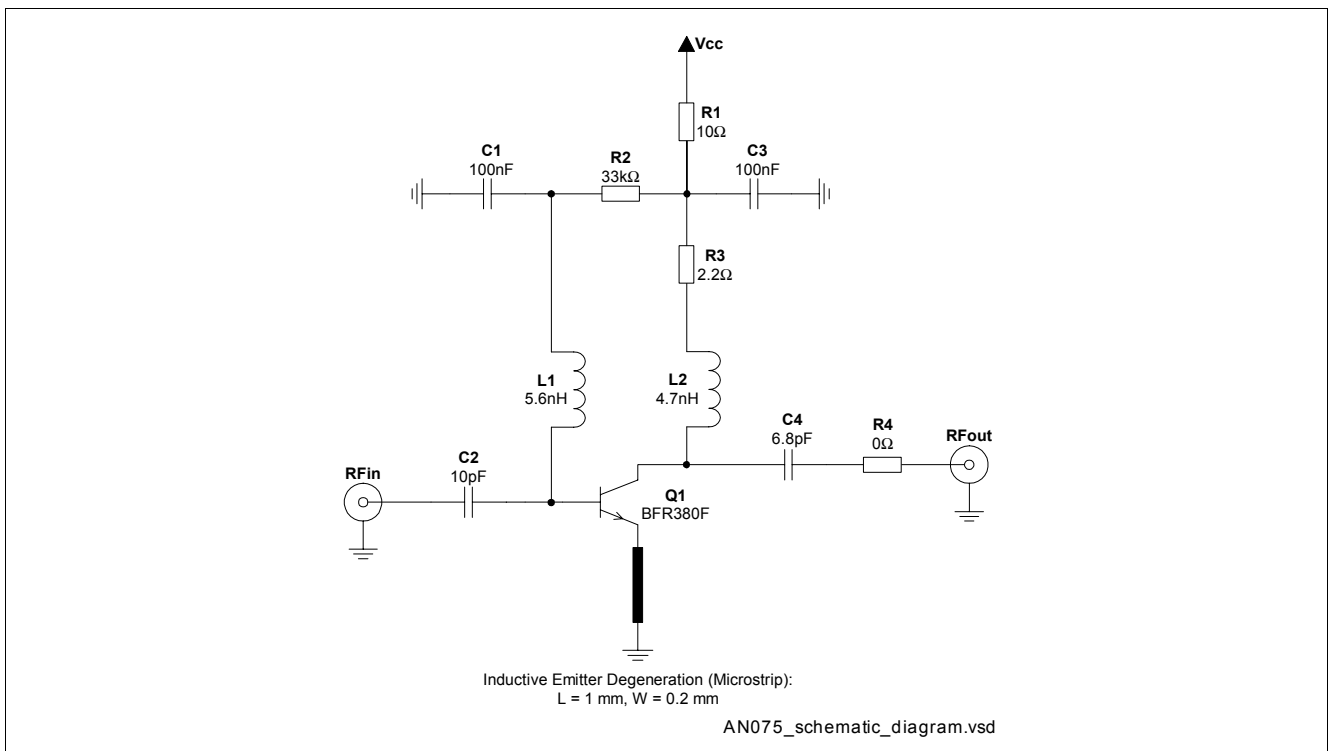


Figure 1 Schematic Diagram

Table 2 Bill of Materials

Name	Value	Package	Manufacturer	Function
C1	100 nF	0603	Various	RF decoupling, IP_3 improvement
C2	10 pF	0402	Various	Input matching, DC block
C3	100 pF	0603	Various	RF decoupling, IP_3 improvement
C4	6.8 pF	0402	Various	Output matching, DC block
L1	5.6 nH	0402	Toko LL 1005-FH	RF Choke, input matching
L2	4.7 nH	0402	Toko LL 1005-FH	RF Choke, output matching
Q1	BFR380F	TSFP-3	Infineon	Si BJT
R1	10 Ω	0402	Various	Biasing
R2	33 Ω	0402	Various	Biasing

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Table 2 Bill of Materials (cont'd)

Name	Value	Package	Manufacturer	Function
R3	2.2 Ω	0402	Various	Stability
R4	0 Ω	0402	Various	Jumper

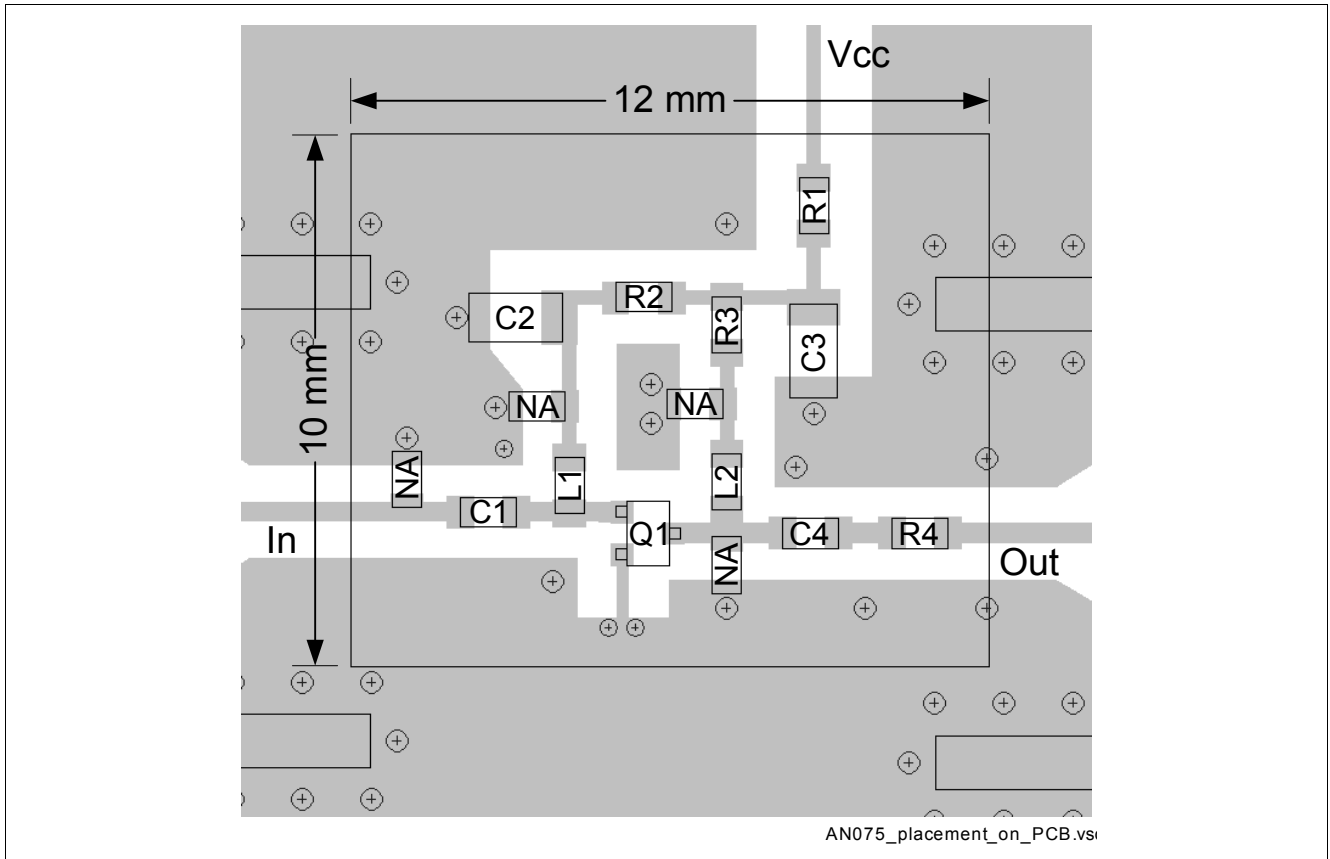


Figure 2 Component placement on PCB

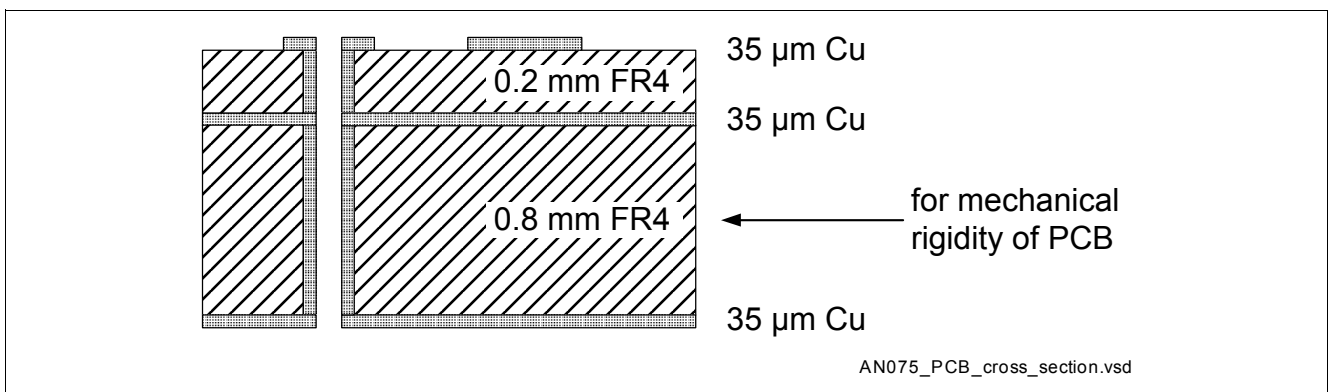


Figure 3 PCB Cross Section

Evaluation boards for the LNA depicted in this application note are available from Infineon Technologies.

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Measured Curves

The following pages show measurement graphs of the BFR380F LNA described in this application note. As mentioned before all measurement results presented here include losses of PCB and connectors, in other words the reference plane is at the SMA connectors.

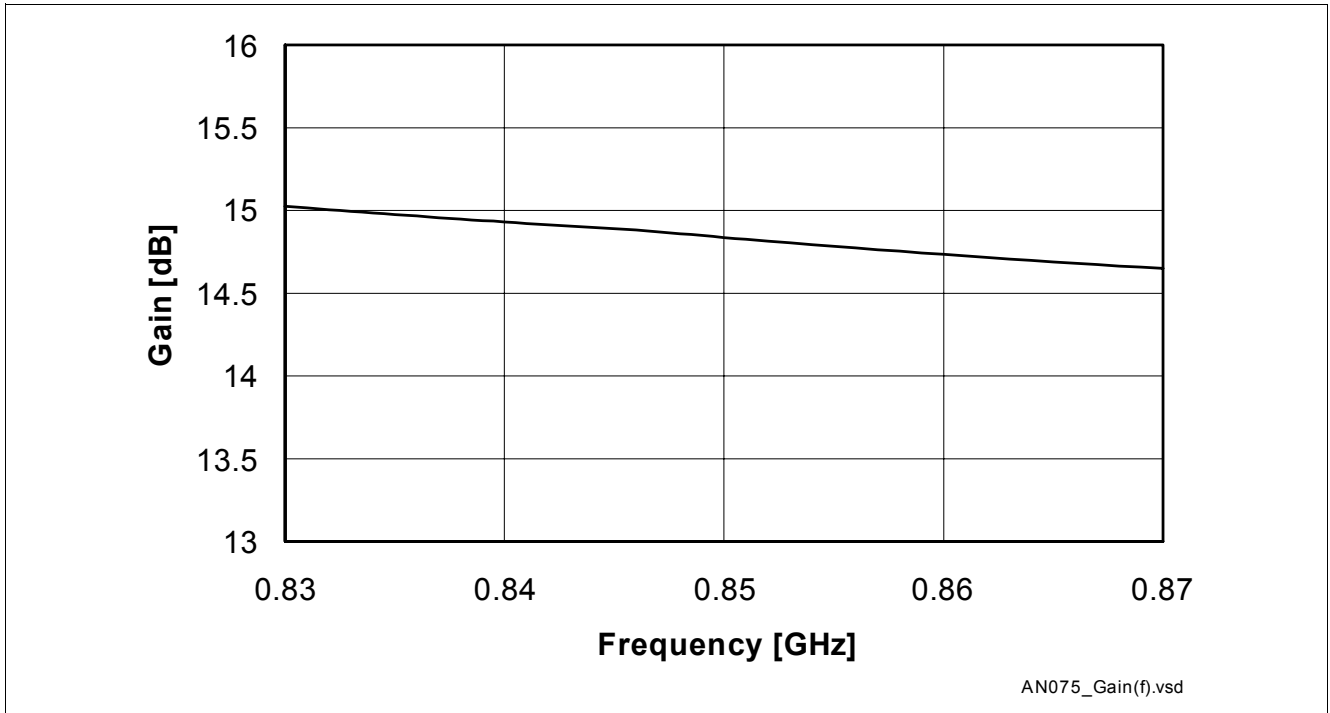


Figure 4 Measured Gain

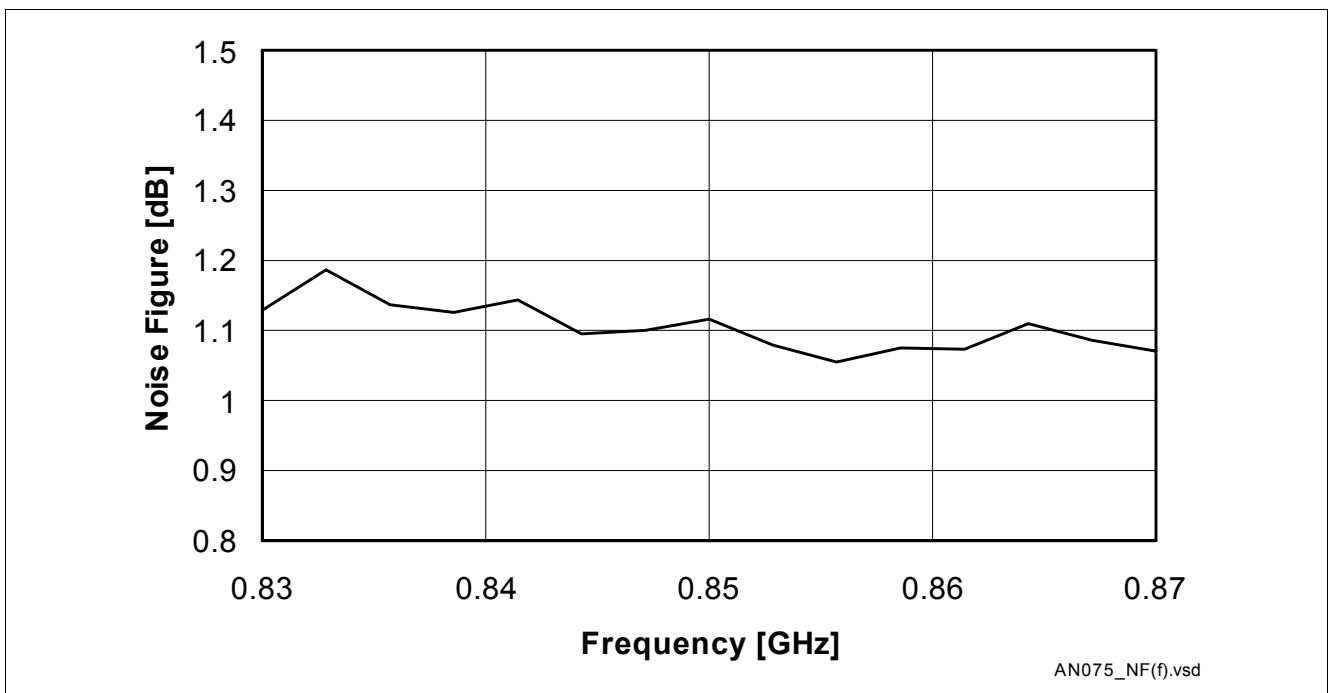


Figure 5 Measured Noise Figure

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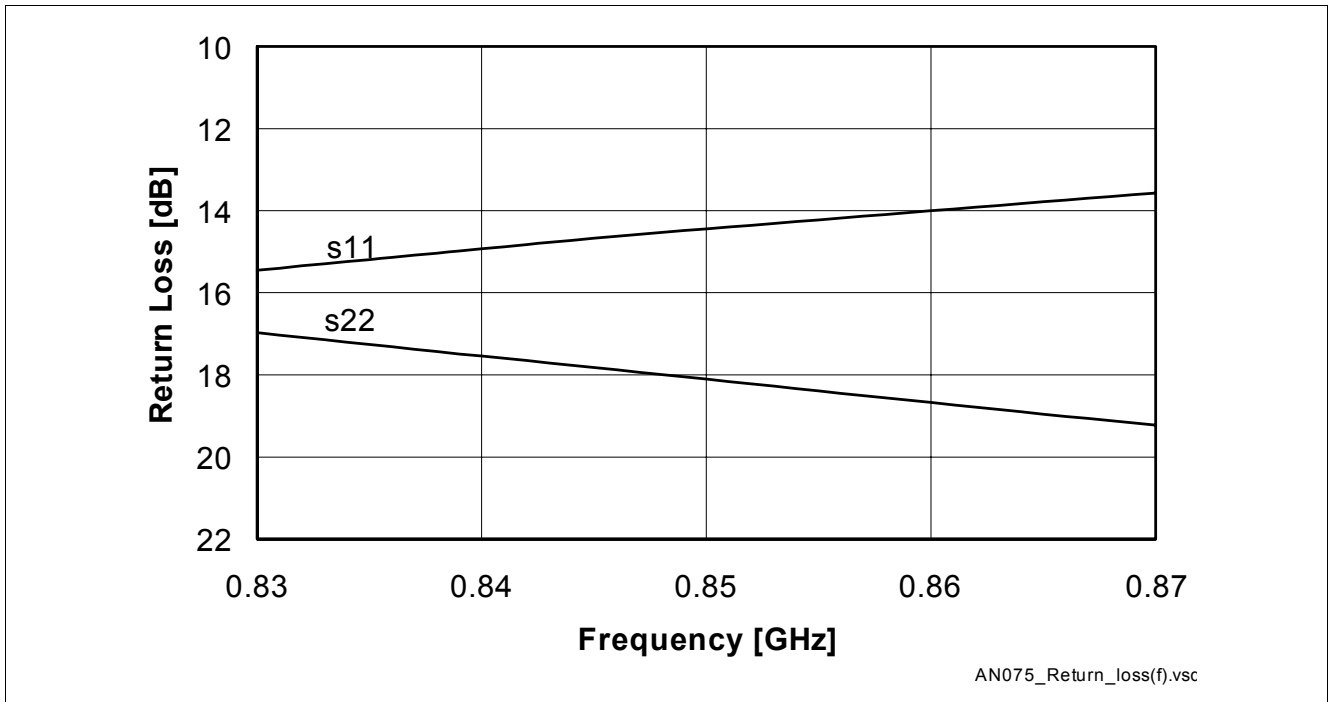


Figure 6 Measured In- and Output Return Loss

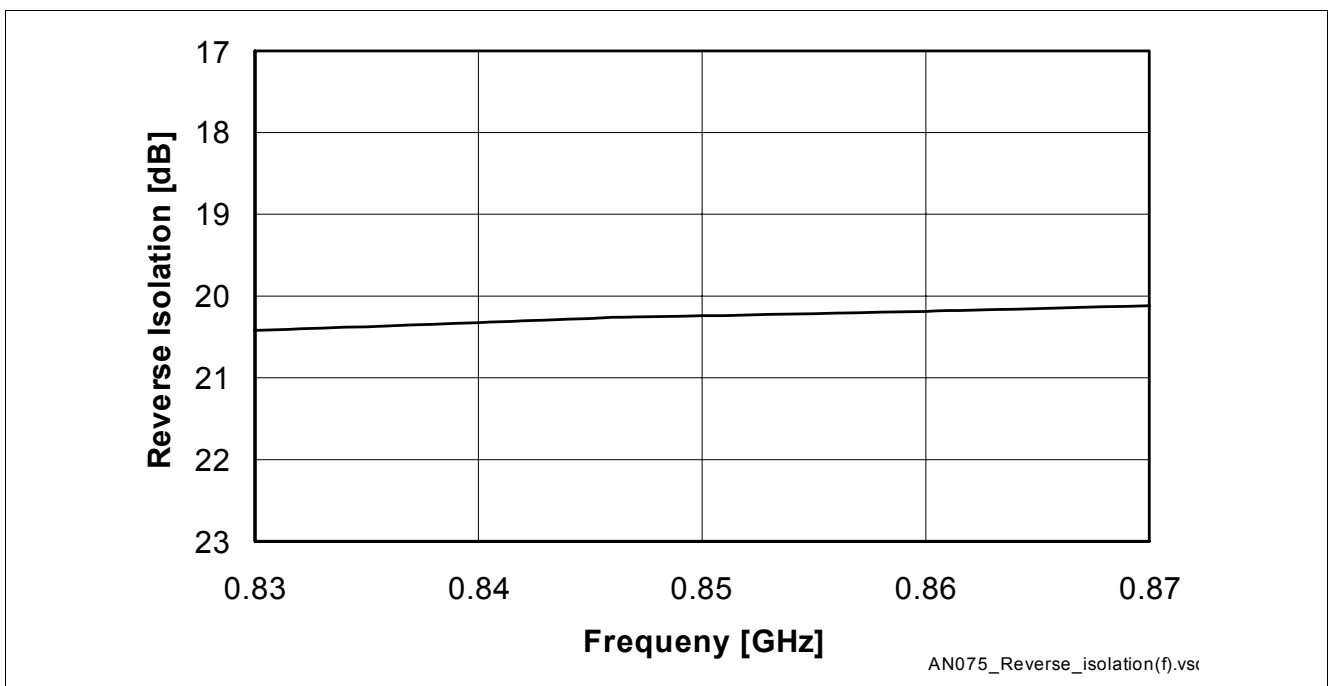


Figure 7 Measured Reverse Isolation

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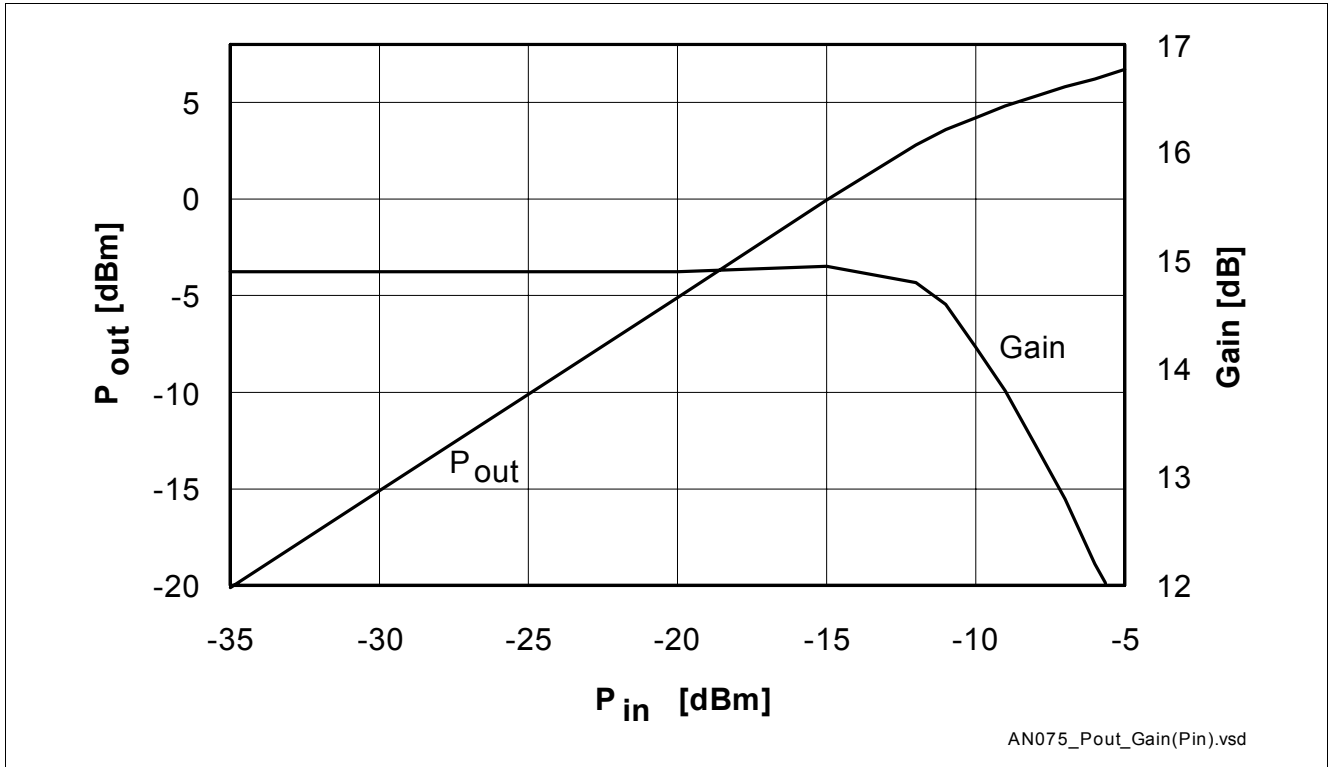


Figure 8 Measured Gain Compression

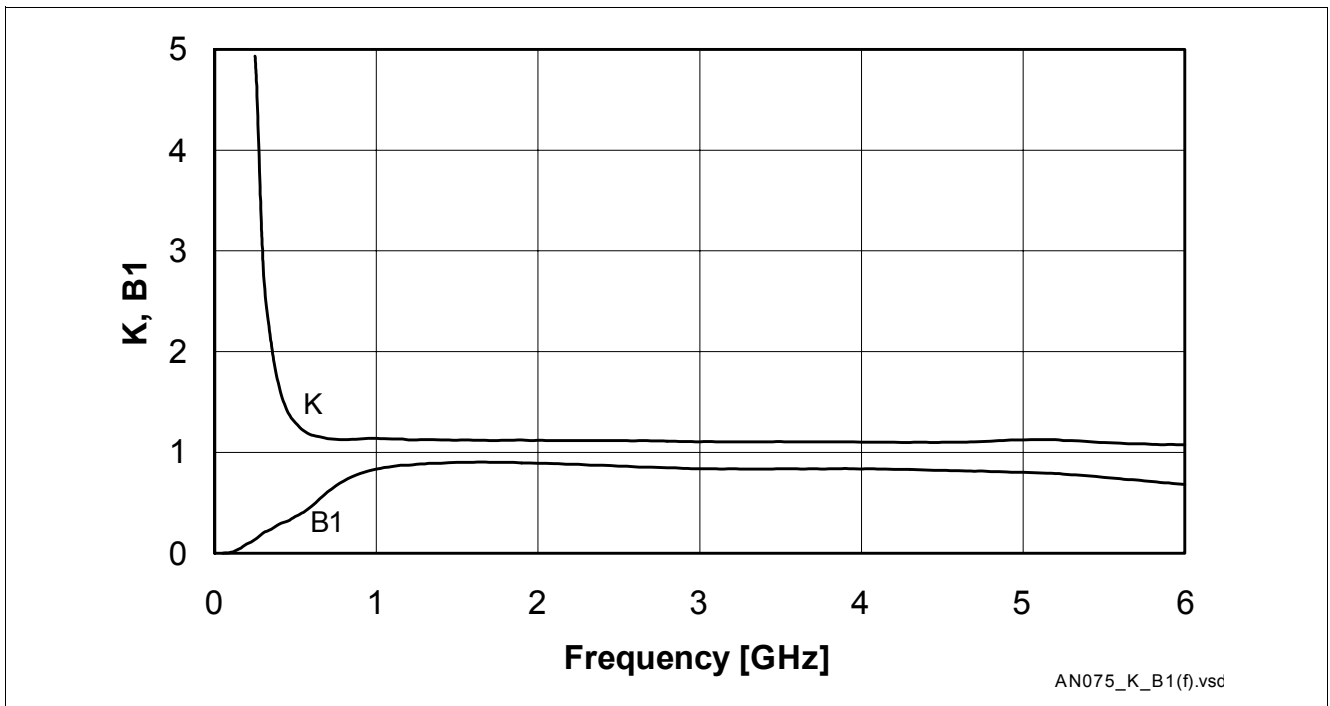


Figure 9 Measured Stability Factor K and Stability Measured B1

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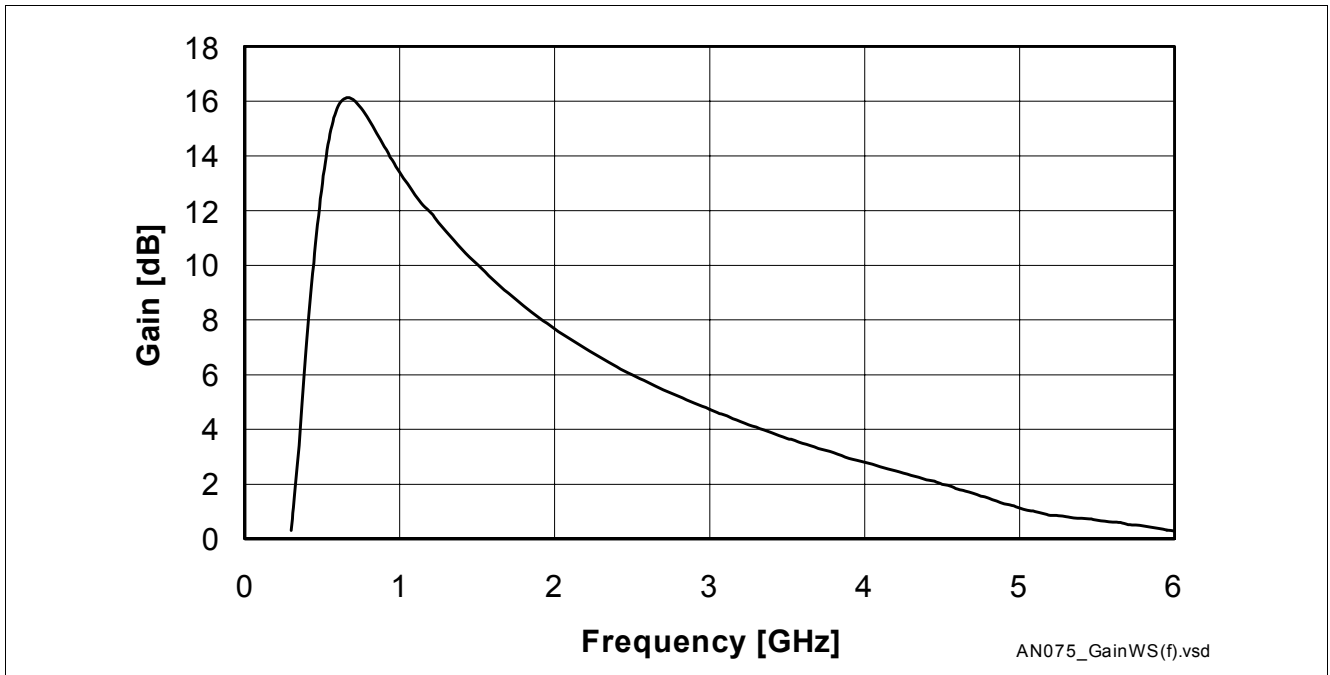


Figure 10 Measured Gain - Wide Span

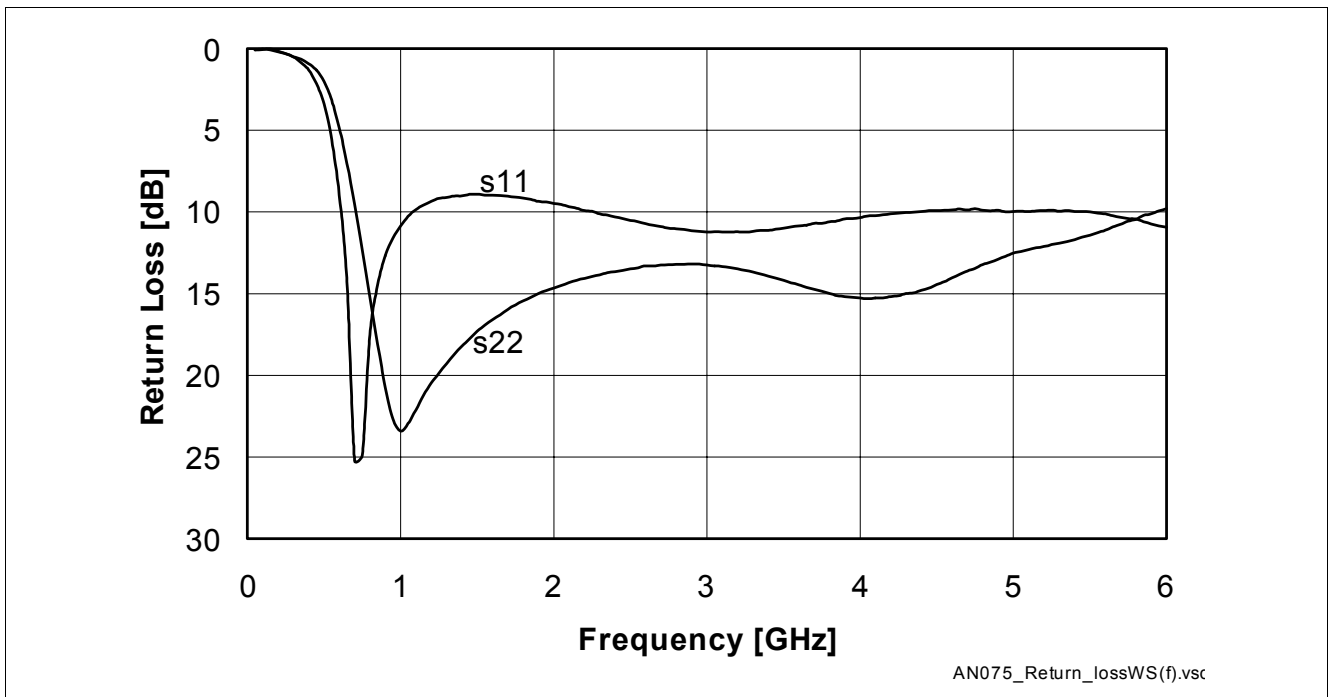


Figure 11 Measured Return Loss - Wide Span