Errata Sheet

V 1.0, 2001-09-03

Device	**SAK 82C900**
Marking/Step	**Step ES-AB**
Package	**P-DSO-28-1**

This Errata Sheet describes the deviations from the current user documentation.

The module oriented classification and numbering system uses an ascending sequence over several derivatives, including already solved deviations. So gaps inside this enumeration can occur.

Current Documentation

- 82C900 User's Manual V1.0 D2 2000-12

Note: Devices marked with EES- or ES are engineering samples which may not be completely tested in all functional and electrical characteristics, therefore they should be used for evaluation only.

The specific test conditions for EES and ES are documented in a separate Status Sheet.

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Table 2 AC/DC Deviations

AC/DC Deviations	Short Description	Fixed in step	Change
PD.SC_1	Power-Down mode supply current (5V, oscillator stopped)	AB	

2 Functional Problems

TwinCAN2.1 Multiple transmissions

Failure description:

It can not be ensured that a message, which is pending for transmission during the transmission of another message is started at the first bit of the following intermission, but after a short delay.

This behavior may lead to the situation, that the transmission of higher priority messages is delayed.

Workaround:

none.

Workaround:

none.

82C900.1 Transmit pin behavior in power-down mode

Failure description:

When the power-down mode is selected (PWD is set in CLKCTR register), the transmit pins of the 82C900 may drive a dominant level. This is dependent on the actual states of the internal state machines.

Workaround:

The problem can be avoided when the corresponding INIT bit is set twice the length of the longest message on the bus (this is at maximum 2x154 CAN bit times) **before** the PWD bit is set.

82C900.3 Write access using the parallel interface

Failure description:

On a write access in parallel mode, the specified time t_{WHLH} (write high to next ALE high) does not fit to the characteristics of the external bus units from the host microcontrollers. If t_{WHLH} is not taken into account, the following ALE signal corrupts the current write access address.

Workaround:

– Tricore Architecture: Configure in EBU_BUSCONx, the RECOVC or the HOLDC bit accompanied by the multiplier CMULT, in such a way, that the delay t_{WHLH} between WR high and ALE high can be hold.
If only one device is using multiplexed bus mode, the problem does not occur as the ALE signal is not used for demultiplexed access. (no ALE generated)
– Otherwise: Transfer the write access into internal code memory.

Application hint:

for Infineon 16-bit microcontrollers see chapter Application hints.

82C900.4 Multiple SSC slaves (including at least one 82C900)

Failure description:

In case of multiple SSC slaves and a disabled Baud-Rate-Error detection, the TwinCAN controller may come to a deadlock situation, which can only be solved by a hardware reset. If glitches occur between two accesses or a non-modulo 8 number of clocks for other slaves is taking place, then the 82C900 gets erratic because all shift clock pulses are counted.

Workaround:

Before the access to the 82C900, the number of shift clock pulses has to be completed to a number of pulses multiple of 8. During this time no other slave should be active.

Another simple possibility is to activate the bit 'Baud-Rate-Error Enable' detection.

82C900.5 Wake up from SLEEP by host

In SSC slave mode, the sleep mode cannot be entered.

In master mode, this is also true for the CANINIT message, configuring the CANCLK for sleepmode. This errata does not apply to SLEEPMSG via CAN.

Workaround:

– SSC mode: Use SLEEPMSG.

82C900.7 Message canceled for transmission

Failure description:

If a message lost arbitration on the CAN bus and this message has been canceled for transmission by clearing TxRQ of the corresponding message object, then this pending transmit request will not be canceled.

In this case the pending transmission can be canceled only if:

– An error frame occurs on the selected CAN bus.
– Resetting the 82C900 device
– The message is transferred successfully without arbitration loss.

Workaround:

– Reset
– Adapted CAN system concept (lower bus load)

82C900.8 Wake up from SLEEP in parallel mode

Failure description:

For parallel mode, the wake up functionality of the 82C900 is specified to take place after an active edge of the $\overline{CS}$ signal (negative edge). In parallel mode, the device wakes up immediately after sleep mode is entered, in case the $\overline{CS}$ signal is still active.

Workaround:

– Parallel mode: Make sure, that the chip select $\overline{CS}$ is inactive as soon as the write access is over. Be aware of the fact, that in case a TriCore architecture is used and more than one device is running in multiplexed bus mode, that the configuration of EBU_BUSCONx is only allowed to be changed during the activation of sleep mode.

3 Deviations from Electrical- and Timing Specification

none

4 Application Hints

82C900.3: Example to avoid problem 82C900.3 on a 16-bit Infineon architecture

If the following assembly sequence is executed from internal memory, a correct write access to the 82C900 can be performed.

If the write sequence is in the internal memory protected by an ATOMIC instruction, neither a PEC transfer nor an external bus access can interrupt the write sequence.

The example shown below allows a correct write access to the 82C900:

The data and the addresses are put into two separate arrays (each array has to be at consecutive addresses in memory) of equal length containing the addresses and data respectively.

unsigned int address_array[length]={address$_1$, .., address$_{length}$}
unsigned char data_array[length]={data$_1$, .., data$_{length}$}

The (unsigned int) address array is handled by R12, the (unsigned char) data array is handled by R13, the length of the array is stored in R14.

```
MOV    _length2,R14
start_sequence: MOV    R8,[R12]
                ATOMIC #4
                MOVB   [R8],[R13]
                ADD    R12,#02h
                CMPI1  R13,_length2
                JMP    cc_ULT,start_sequence
RETN
```

By using this sequence, the timing t_{WHLH} can be reached for microcontroller frequencies up to 20MHz.

5 Documentation Update

none

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