Next Generation Automotive

Compact and efficient power electronics enablers

With the recent upsurge in hybrid vehicle adoption and almost all major car OEMs now working on full electric vehicle projects, people often point out that this is old news. In many respects they are correct; the origins of the electric car can be traced back to the 1830s and by the late 1890s fleets of electric taxi cabs were running around the streets of several US cities. So what's different this time round?

By Benjamin Jackson, Product Manager, Automotive MOSFETs, International Rectifier

There have been two major barriers to the electrification of the car to date. The first is the dominance of the existing technology. In short the internal combustion engine is just too good. Modern engines are mass produced, cost effective, well understood, highly refined & reliable and supported by a universally established refueling and repair infrastructure. Now as governments scrutinize CO_2 emissions, the internal combustion engine is coming under pressure from both ends with heavy taxes on the gasoline put into the tank and on the emissions flowing out of the exhaust. The second major obstacle to the electrification of the car is energy density. The main enablers here will be new battery technology and novel battery management schemes. But at the same time the systems which use the limited onboard supply of electrical energy will have to do so in a more intelligent way. An increasing awareness of efficiency is fueling a rapid change in the application landscape across all vehicle types. High power DC-DC converts, HID lighting, class D audio, electric power steering, 3 phase inverters and synchronous rectification will appear in increasing numbers on next generation cars, offering efficiency and good power density. Power MOSFETs will be a key enabling technology in both controlling the battery and its loads.

By their nature power MOSFETs are not 'ideal' switches. MOSFETs have a finite on-resistance, add parasitic parameters to the electrical path and, the more power needed the more space is required for switches and cooling assemblies. These all affect the power density and efficiency of a given power electronics system. How can this be improved?

The power dissipation in the steady state of a semiconductor can be expressed as:

$$Pd = \frac{T_j - T_A}{R_{thJA}}$$

(1) Where Pd is the power dissipated in the semiconductor switch, T_j is the junction temperature, T_A the ambient temperature of the surroundings and R_{thJA} is the total thermal resistance from junction to ambient.

Also considering the relationship between power, current and $R_{DS(on)}$

$$P_d = I_D{}^2 R_{DS(on)}$$

(2) Combining 1 and 2 together we can link the current to the thermal resistances and the $R_{DS(on)}$:

$$I_D = \sqrt{\left(\frac{T_j - T_A}{R_{thJA}}\right) / R_{DS(on)}}$$

(3) This equation is important as it shows how the thermal management aspects of the design have a direct impact on the electrical performance of the system.

Finally dividing by the area of the MOSFET's PCB footprint, A_{FP}, we can arrive at the current density of the device:

$$CurrentDensity = \frac{\sqrt{\left(\frac{T_j - T_A}{R_{thJA}}\right) / R_{DS(on)}}}{A_{FP}}$$

(4) On closer inspection of equation 4 the main obstacles to greater current density can seen.

Minimize thermal resistance → Maximize heat extraction

The first step to increasing power density is to ensure that for a given $R_{DS(on)}$ the silicon in housed in a package which enables the heat generated to be easily extracted; R_{thJA} must be as low as possible.

To keep R_{thJA} low semiconductor designers can increase the size of the silicon die, getting more die in contact with the package enables a better heat transfer to the outside world, a larger die archives this and has lower $R_{DS(on)}$, but at greatly increased cost. Alternatively the thermal resistances of the package can be reduced, perhaps with new materials or a new style of package. Most traditional power packages only have a single cooling path; through the bottom of the device to the PCB or heat sink. Great improvements can be made with the addition of a secondary cooling path; this is exactly what the DirectFET package enables via top side cooling.

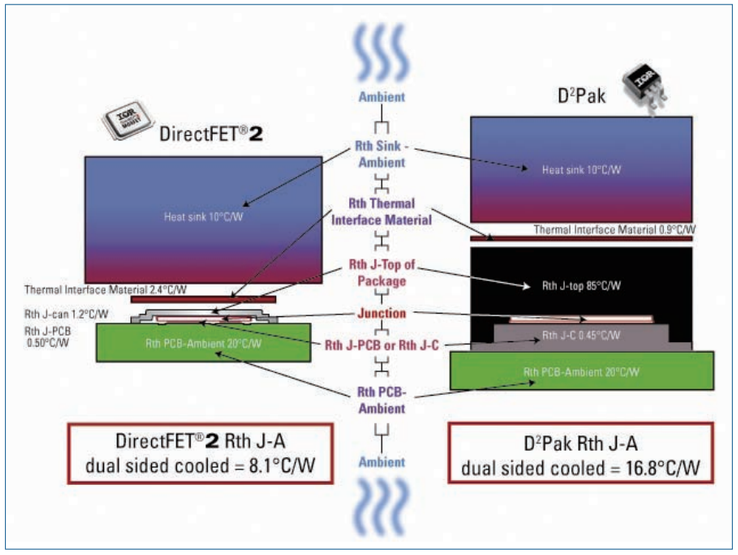

Figure 1: Comparison of cooling routes for a D2Pak and large can DirectFET package

Figure 1 compares and contrasts the thermal routes for getting the heat out of a Large Can DirectFET package and a D2Pak. In both cases the designer has attempted to achieve the lowest possible thermal resistance from junction to ambient by using both the downward thermal path from the junction to the PCB and the upward path through the package to a heat sink on top of the part.

Both packages have good thermal resistance from the junction to the PCB with values of 0.5°C/W and 0.45 °C/W for the $R_{th\ J\text{-}PCB}$ of the DiretcFET and D2Pak respectively. By adding a second upwards thermal path these values can be reduced. The D2pak was not designed to be cooled through the top of its thick plastic package, but if this is attempted an $R_{th\ J\text{-}TOP}$ (junction to top of package thermal resistance) of around 85°C/W will be seen compared to the DirectFET which has an considerably lower value of 1.2°C/W. When the overall thermal resistances of the two routes in parallel are compared the dual sided cooled DirectFET has a thermal resistance which is around half of the D2Pak. Using the second thermal route enables an instant improvement in the current density of the system.

Keep $R_{DS(on)}$ low

Looking at the numerator of equation 4 after having kept R_{thJA} low it's then important to consider the root cause of the heating – the on resistance of the device. A key figure of merit here is the semiconductor material and the design of the MOSFET itself. However silicon based MOSFET technology is maturing forcing manufacturers have to look to further afield to complex silicon solutions or new materials to keep the $R_{DS(on)}$ low. But it is also important to consider the effect of the package on the $R_{DS(on)}$ value or rather the limitations that the package places on delivering ultra low $R_{DS(on)}$ to the system.

MOSFETs with an on resistance in the 1mΩ range at 40V are reasonably common in the market today and increas-

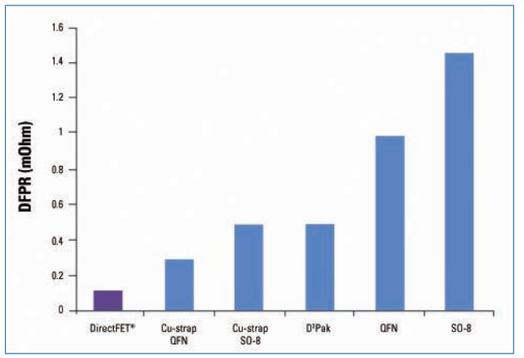

Figure 2: Comparison of die free package resistances for different power packages

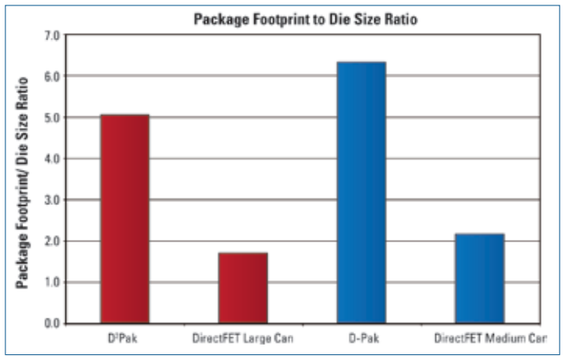

Figure 3: Package footprint to maximum die size area ratio for different power packages

Part	AUIRFS3004-7P	AUIRF7739L2
Package	D2Pak-7P	Large Can DirectFET
PCB Footprint	170 mm²	64 mm²
Single Side Cooled on FR4		
R_{thJA} (Single side cooling)	40 ° C/W	40 ° C/W
$R_{DS(on)}$ @ T_j = 105° C, T_A = 25 ° C	1.24 mΩ	0.9 mΩ
I_D	40.1 A	46.3 A
Current Density	0.24 A/mm²	0.73 A/mm²
Ratio of current density	**1**	**3.1**
Dual Sided Cooled		
R_{thJA} (Dual side cooling DF only)	40 ° C/W	12.5 ° C/W
$R_{DS(on)}$ @ T_j = 105° C, T_A = 25 ° C	1.24 mΩ	0.9 mΩ
I_D	40.1 A	82.8 A
Current Density	0.24 A/mm²	1.30 A/mm²
Ratio of current density	**1**	**5.5**

Table 1: Comparison of current density for a D2Pak-7P and a large can DirectFET with different cooling arrangements

ingly on such devices around half of the $R_{DS(on)}$ stated on the datasheet is attributed to the package. The resistance that the package adds to the silicon is know as the Die Free Package Resistance (DFPR) and figure 2 shows the DFPR values for various power packages.

There is a large range in DFPR values between the existing plastic packages (shaded in green). Different wire bonding and lead frame options enable the DFPR to be greatly reduced to around 0.3mΩ in the case of the copper clip PQFN. However the lead frame and wire bonds on the traditional plastic packages still leave a relatively long electrical path between PCB and die. As the market continues to demand more efficient systems, at higher power levels, $R_{DS(on)}$ values will hit a fundamental limit at the resistivity of the conductors in the packaging. When the wire bonds and leadframe removed (in the case of DirectFET) the DFPR is reduced to a value of less than half of best performing equivalent plastic power package at a mere 150μΩ. This enables very low $R_{DS(on)}$ and the best possible current density for a given semiconductor technology. Furthermore the dramatic reduction of the DFPR barrier ultimately means that a lower area of silicon is needed to deliver a given $R_{DS(on)}$ to the system and thereby opening up the possibility of cost savings.

Go small to be effective

Finally turning to the denominator of equation 4 it's clear and logical that ultimately the smaller the footprint of the MOSFET greater the current density. But such a reduction in package footprint area must not be done at the expense of $R_{DS(on)}$ or current rating. Ideally the designer wants to get the lowest $R_{DS(on)}$ possible in a given space. As die size and $R_{DS(on)}$ are inversely proportional, calculating the ratio of package footprint area to maximum die size area for the given package is an indication of the $R_{DS(on)}$ performance that a given package can offer in a given space. Figure 3 plots the ratio of package footprint to maximum die size area.

In figure 3, the ideal ratio would tend towards 1, giving the least mm2 of PCB footprint to achieve a given $R_{DS(on)}$. However figure 3 clearly shows the area overhead that the more traditional packages such as the DPak and D2Pak place on the die size area, and ultimately the reduction in current density. The D2Pak has a package footprint to maximum die size area ratio of 5; the package area is five times the size of the largest die size. The Large Can DirectFET however offers a ratio of around 1.7 – so ultimately on the PCB you can achieve a given $R_{DS(on)}$ in a smaller space and therefore at a higher current density as well as saving on PCB and enclosure space.

Drawing the factors of space, $R_{DS(on)}$ and R_{thJA} together, table 1 (using equation 4) makes a side by side comparison of a low $R_{DS(on)}$ D2pak product with a counterpart Automotive DirectFET product. The table summarizes the improvement in current density.

By taking two high performance 40V power MOSFETs which are typically used in automotive applications table 1 shows how current density can be improved by over 3 times due to the low package resistance and small PCB footprint of the DirectFET package. When dual sided cooling is employed the DirectFET can further improve its margin to over 5 times the current density of the D2Pak.

The adoption of new fuel efficient vehicles has been kick-started by financial, environmental and political forces of the last few years. But the electrification of the car will only be a long term success if new electrical solutions prove they can overcome the technical and practical dominance of the existing internal combustion engine and its drive train. This has proven to be too greater hurdle over the last 170 years, but today, with highly efficient, cost effective & compact power semiconductors and battery technology the links to the successful electrification of the car are beginning to connect. The humble package which holds the small and delicate semiconductor it important to protect the device from its environment but it also serves an important role as the performance gatekeeper between the die and the PCB. As tougher performance goals are set bringing the packaging technology of power semiconductors up to date will be key to unlock the maximum performance from existing silicon MOSFETs and the next generation compound semiconductors.

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Essential Multicell Monitoring

Maximizing the cycle life of rechargeable battery packs

Rechargeable battery packs prematurely deteriorate in performance if any cells are allowed to over-discharge, for example, in hybrid automobiles or lower-cost products like portable tools and backup power sources. As a pack becomes fully discharged, the ILOAD • RINTERNAL voltage drop of the weakest cell(s) can overtake the internal VCELL chemical potential and the cell terminal voltage becomes negative with respect to the normal voltage

By Jon Munson, Senior Applications Engineer, Linear Technology Corporation

In such a condition, irreversible chemical processes begin altering the internal material characteristics that originally provided the charge storage capability of the cell, so subsequent charge cycles of the cell do not retain the original energy content. Furthermore, once a cell is impaired, it is more likely to suffer reversals in subsequent usage, exacerbating the problem and rapidly shortening the useful cycle life of the pack.

With nickel-based chemistries, an over-discharge of a set of series-connected cells does not necessarily lead to a safety hazard, but it is not uncommon for one or more cells to suffer a reversal well before the user is aware of any significant degradation in performance. By then, it is too late to rehabilitate the pack. In the case of the more energetic lithium-based cell chemistries, reversals must be prevented as a safety measure against overheating or fire. Monitoring the individual cell voltages is therefore essential to ensure a long pack life (and safety with lithium cells).

Enter the LTC6801, developed to provide integrated solutions for these specific problems. The LTC6801 can detect individual cell overvoltage (OV) and undervoltage (UV) conditions of up to twelve series connected cells, with cascadable interconnections to handle extended chains of devices, all independent of any microprocessor support.

Features of the LTC6801

The operating modes and programmable threshold levels are set by pin-strap connections. Nine UV settings (from 0.77V to 2.88V) and nine OV settings (from 3.7V to 4.5V) are available. The number of monitored cells can be set from 4 to 12 and the sampling rate can be set to one of three different speeds to optimize the power consumption versus detection time. Three different hysteresis settings are also available to tailor behavior of the alarm recovery.

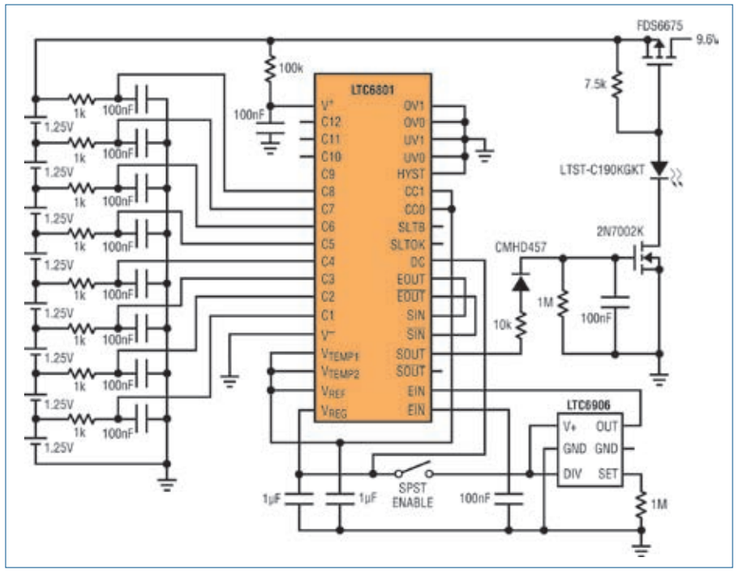

Figure 1: An 8-cell nickel pack can be easily monitored and protected from the abuse of over-discharge