GaN - A New Era Begins

Commercial introduction of GaN based power electronics

The initial commercial introduction of GaN based power conversion solutions by International Rectifier repre-sents the culmination of significant engineering efforts to resolve several fundamental barriers to achieving practical cost effective high performance packaged power devices.

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Introduction

As has been previously discussed [1], significant advances in the performance/cost figures of merit (FOMs) for power devices (e.g. Rdson*cost or Ron*Qsw*cost) are required in order to improve the power delivery system FOM of efficiency*density/cost. The reduction of total system costs can be substantially enabled by intelligent power electronics which optimize performance/cost, in turn promoting the wide spread adoption of more efficient working loads, leading to a potential reduction in worldwide energy consumption by some 25%.

Over the last 3 decades significant engineering efforts have driven the improvement in the performance figure of merit of silicon based power devices by more than an order of magnitude. However, as this technology approaches maturity, it becomes increasingly expensive to achieve even modest improvements in the device FOM. It is estimated that less than a factor of two improvement will be economically feasible to achieve for 30 V FETs [3], with perhaps a factor of five possible for 600 – 1200V silicon IGBTs [4]. Necessary further advances in power device performance must be achieved through the use of alternative materials. One of the most promising alternatives to silicon is gal-lium nitride based power devices.

Even though the basic GaN HEMT transistor was first invented over 15 years ago by M. Asif Khan [5], significant development efforts on practical power devices using GaN-on-Si technology have been fairly recent, predominantly in the past 5-7 years. GaN based power devices are expected to improve rapidly over the next 10 to 20 years. In fact, it is expected that an order of magnitude in improvement in the key device performance FOMs will be achieved over the next 5 years.

Barriers to Commercialization

There have been however, several significant barriers to the commercialization of GaN based power devices. Chief amongst these is the cost of production. The production of power devices includes the costs of substrate, epitaxy, device fabrication, packaging, support electronics and development.

The viable economic based limit of about \$3/cm^2 for substrate and epitaxy cost set by the power device marketplace is exceeded by all substrate choices except silicon wafers. Multi-wafer MOCVD tools provide the required through-put and cost of ownership.

Next to the cost of substrate and epitaxial layers, device fabrication costs are the most critical. In fact, currently, sub-strate diameters of at least 150mm are required to achieve widespread commercial viability for power device fabrica-tion. In addition, the device fabrication costs are only acceptable if high volume, high yielding standard (silicon compatible) semiconductor fabrication lines are used. Similarly, the volume necessary to support the broad power device market (10 million 150mm wafer equivalents per year) requires scalability in device manufacture provided most readily by existing silicon device fabrication facilities.

It is for these reasons that International Rectifier has developed its GaNpowIR technology platform using GaN-on Si hetero-epitaxy and device fabrication processing that can be performed in a standard modern silicon CMOS manufacturing line with little modification to equipment or process discipline. It is this approach that allows this technol-ogy platform to provide power devices with compellingly superior performance/cost FOMs compared to silicon which will promote widespread adoption.

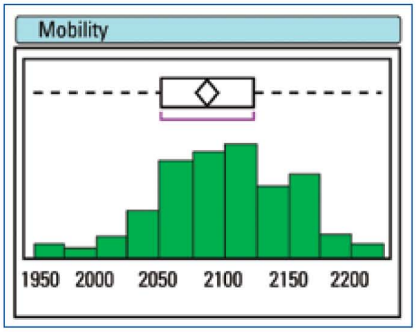

Figure 1: Measured Hall Mobility (cm^2/Vs) for GaNpowIR III-Nitride HEMT epitaxy.

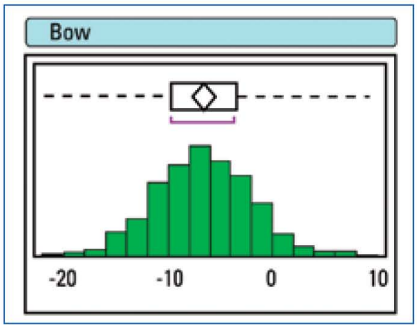

Figure 2: Measured wafer bow in microns after III-Nitride HEMT epitaxial deposition on 150mm silicon.

Initial GaNpowIR Device Focus

As has been previously reported [2], the initial GaNpowIR products from International Rectifier will be low voltage (30V) dc-dc power stage modules. This approach is different from many commercial efforts which focus on the obvious advantages of GaN based power devices at higher voltage ratings above 600V [3,6,7]. Though the distinct ad-vantage of low voltage GaN based HEMTs is not as obvious in terms of specific-on-resistance, it is important to note the it is the R(on)*Qsw FOM which is critical to many of the low voltage applications. In this regard, the GaN HEMTs are expected to achieve more than an order of magnitude improvement over state of the art silicon devices within the next 5 years [2]. Quantitatively, this means a R(on)*Qg device performance of less than 4 mohm*nC compared to next generation silicon FOM of 45 mohm*nC.

Barriers Overcome

One of the most fundamental challenges to the commercialization of GaN based power devices is the development of cost effective, high yielding, high throughput III-Nitride epitaxial processes on large diameter silicon wafers. It is well established that silicon is the substrate of choice for commercial GaN based power devices. The intrinsic mis-match in both lattice constant and thermal coefficient of expansion with the requisite III-Nitride epitaxial films causes threading dislocations, as well as significant macroscopic film stresses, which result in excessive wafer bow and plastic deformation (cracks) in the films. These issues have been addressed by engineering the proprietary epi-taxial film growth on standard thickness 150mm <111> silicon wafers to both eliminate most of the threading dislo-cations, resulting in $10^9 cm^{-2}$, predominately edge dislocations for 2µm thick films (comparable to similar thickness films grown on SiC), as well as compensating for the stresses due to thermal coefficient mismatches. These result in a high quality device layer, as demonstrated by the excellent electron Hall mobility of >2000cm^2/Vs achieved in the 2 dimensional electron gas formed at the interface between the thick GaN buffer layer and the overlying AlGaN bar-rier layer, as shown in Figure 1.

In addition, the resulting wafer bow is well within the required limit for device fabrication of < 60µm, as shown in Figure 2 (bow in µm).

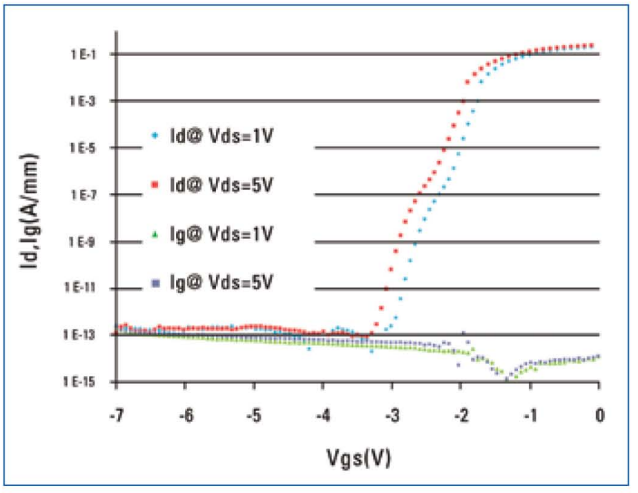

Figure 3: Measured Id normalized to gate width (850mm) as a function of Vgs for Vd= 1 and 5V, Lg=0.3µm.

It should be noted that truly crack free material to within 0.5mm of the wafer edge are consistently produced by this process in manufacturing volume. Further, the occasional crack that is found

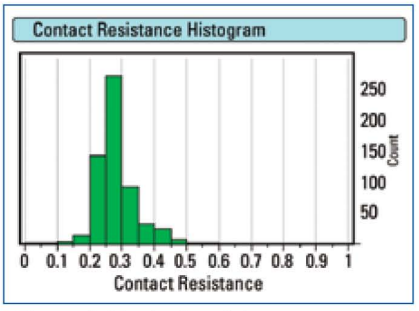

Figure 4: Contact resistance measured using standard transmission line technique in ohm-mm for initial GaNpowIR platform.

within 0.5mm of the wafer edge has been shown not to propagate during subsequent device fabrication.

Much of the reported constructions for GaN devices to date utilize Schottky gates and subsequently exhibit device leakage in operation of mA/mm of gate width. For a power device, which often has an effective gate width on the or-der of 1 meter, such gate leakage would result in an unacceptable power loss/heating. Similarly, the maximum oper-ating voltage has often been specified at reverse bias source-drain current densities of mA/mm of gate width. Another challenge, therefore, is the reduction of these leakage currents to less than 1uA/mm. This has been achieved through the combined use of a proprietary insulated gate construction and improved III-Nitride epitaxial film quality. This has resulted in gate and drain-source leakages of <10pA/mm, as shown in Figure 3. The resulting ratio of Ion/Ioff of 10^{12} is substantially better than reported elsewhere for GaN based devices and even exceeds that of comparable sili-con based power devices.

Figure 5: Topside view of a flip chip GaNpowIR device.

Though the principle challenge to develop high voltage GaN on Si based devices which substantially exceed the per-formance of silicon based devices appears met to a large degree [e.g. 3,6,7], substantial challenges existed to produce low voltage devices to exceed silicon device performance. One such challenge is the reduction and control of source-drain contact resistance. Though this component to the Rdson of a high voltage device (e.g. > 300V) is negligibly small, it can dominate the FOM for low voltage devices (e.g. <100V). In fact, in order to be competitive, the contact resistance for low voltage devices must approach 1micro-ohm cm^2 or <0.35ohm mm. This has been achieved in a cost effective, high volume manner within the IR GaNpowIR technology platform, without the use of gold metallurgy, as shown in Figure 4.

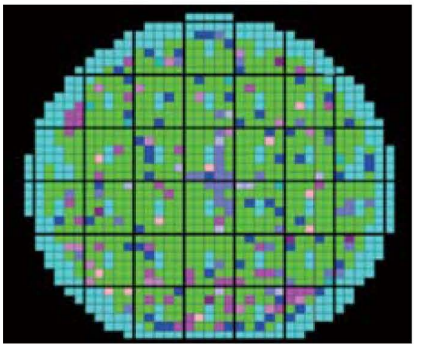

Figure 6: Wafer yield map for production GaNpowIR fabrication process for 15mm^2 die (green = good die).

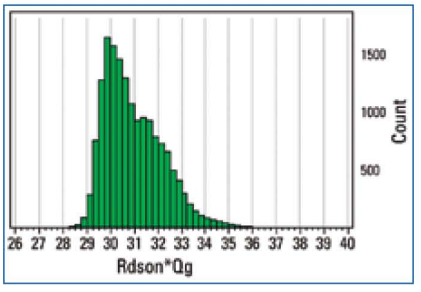

*Figure 7: Measured Ron*Qg product for initial GaNpowIR technology platform.*

Another challenge for the realization of commercially viable low voltage GaN devices is the effective conduction of the source-drain current from the internal to the external device terminals. This has been accomplished through the use of planarized multi-level metallization, common to silicon ULSI device fabrication. In addition, the use of a proprietary solderable front metallurgy (SFM) has been used to produce a flip-chip die, eliminating wire bonding and minimizing other package related parasitics. Figure 5 shows such a flip chip GaN power device.

Device yield is an important challenge for the commercialization of large area power devices. Unlike RF devices, with active areas < 1mm^2, power devices often have active areas >10mm^2. It is economically imperative that yields > 80% are commonly achieved for such large devices. Figure 6 shows a wafer map of device yield for 15mm^2 devices, demonstrating the necessary level of process maturity for

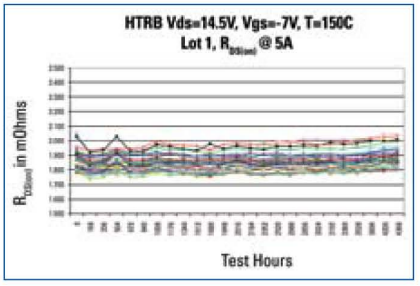

Figure 8: Measured stability of Ron for large (2.5 meter Wg, Lg=0.3µm) power device under constant reverse bias stress for >4000 hrs.

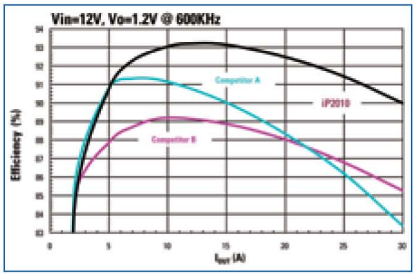

Figure 9: Measured power conversion efficiency for initial GaNpowIR product, iP2010, a 12V$_{in}$ to 1.2V$_{out}$ POL converter power stage operating at 600kHz compared to two silicon based alternatives.

commercialization.

It is interesting to note that much of the remaining yield loss is unrelated to the properties of the III-Nitride epitaxial layers.

Figure 7 shows the distribution for the RQ FOM for a typical wafer batch of low voltage product die, demonstrating that the target of 30mohm*nC for this first generation technology platform has been achieved [2].

Finally, the stability of device in-circuit performance is a prerequisite to commercialization. Figure 8 shows the Rdson stability for a random selection of low voltage GaN power devices.

As can be seen, the stability of this critical FOM is excellent under accelerated conditions for >4000 hrs. In fact, over 1,000,000 device hrs of reliability testing has shown performance in line with silicon based device specifications. Tests have included, gate stress, reverse bias stress, constant current (2x specification), temperature humidity bias, package testing for MSL and temperature cycling, high temperature operating life and intermittent operating life tests.

First Product

In order to realize the potential of the GaN based power devices, it is necessary to develop companion technologies such as high speed drivers, low duty cycle capable PWM controllers and low parasitic packaging [1]. For example, the transition times (and dead time) are on the order of 1ns [1], making it necessary to provide intelligent and fast deadtime control for the drivers in order to realize the optimal performance made possible by the GaN power device.

The first product release to production on the IR GaNpowIR technology platform is a 30A capable 12V buck converter power stage product. It incorporates the control and synchronous rectifying switches together with the intelligent gate driver in a low parasitic LGA package. Figure 9 shows the measured power conversion efficiency for this first generation GaN product compared to competitive silicon based solutions.

Here it can be seen that the GaN based power devices provide more than a 3% improved conversion efficiency over state of the art silicon FETs. In adition, by enabling this high efficiency at 600kHz, this GaN based power solution enables the use of all ceramic capacitors in the power converter, thereby enhancing system reliability.

As has been previously discussed [1] further improvements in LV GaN based power devices (e.g. RQ<5) will allow for truly revolutionary performance of efficient (85 to 90%) single stage power conversion (e.g. 12V to 1.2V) at >50MHz frequencies, eliminating much of the output filter components, significantly reducing costs, and shrinking the converter size by more than a factor of ten. Perhaps more importantly, this higher frequency operation enables the more intimate positioning of the conversion stage with the electronic load. This eliminates a significant amount of parasitic power losses in the output filter and PCB/ package. The resulting simultaneous improvement in power conversion density, efficiency and cost represents the true value of GaN based power device development for LV ap-plications, as it is unknown how to achieve such performance/cost using silicon based devices.

Perhaps even more importantly, the IR GaNpowIR technology platform represents a cost effective platform for true power integrated circuits, incorporating a range of voltage capable devices with best in class performance. This will allow system on a chip integration, such as complete AC-LV DC conversion and high power monolithic inverters for motor drives and power distribution. More than the replacement of silicon discrete devices with GaN based devices, this platform opens a new era for integrated power conversion.

Conclusion

The first commercially viable GaN based power device platform has been introduced, overcoming several significant barriers, particularly cost. First products focus on low voltage applications, resolving technical issues particular to these class of devices. General solutions of high quality, crack free III-Nitride epitaxy in a production environment as well as low contact resistance and low device leakage levels have been achieved. Excellent device stability as well as commercially acceptable device yields have also been achieved.

More than the replacement of silicon discrete devices with GaN based devices, this platform opens a new era for in-tegrated power conversion.

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