Single stage conversion enables small and cool PoL designs

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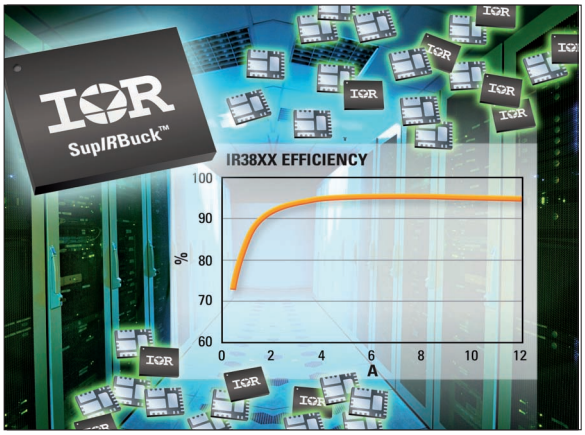
The availability of small, efficient, flexible PoL converters allows the use of single stage conversion, and enables any motherboard rail requiring a supply below 15A to be powered via a common device footprint.



Point of load (PoL) has become the architecture of choice for power systems for several reasons. First, the low supply voltages required by modern devices allow designers to cut on-chip power consumption dramatically, but distributing system power at such low voltages contributes to losses. It therefore makes sense to distribute the power via a high-voltage bus, and convert close to the point of use. At the same time, the majority of systems – as well as many chips – now require multiple supply voltages. Implementing multiple system-wide power buses is typically a less attractive option than local conversion. The need to satisfy high peak current demands also drives the move towards PoL techniques. Moreover, chips and systems increasingly require power-up and power-down to be performed in a controlled sequence: local conversion makes it easier to inject intelligence where it is needed.

Although PoL architectures are well established, they nevertheless remain challenging to implement in many situations. One of the main difficulties is that conventional PoL solutions accommodate only a narrow range of input and output voltages. This means that a typical system requires two-stage conversion. First a 12V input is stepped down to the rail voltage (typically 3.3V or 5V). This is then used by the PoL converter to produce the required output voltage. The two stage technique, however, is wasteful of both board space and power, since it entails two sets of losses. To overcome these restrictions, International Rectifier has developed the SupIRBuck family of PoL voltage regulators. The devices operate from any input voltage, from 2.5V to 21V. As a result, more efficient single stage power conversion becomes a possibility. To quantify the improvement that might be expected from the single-stage approach, figure 1 compares the efficiency of the two types of system. In the two-stage architecture, stage one would convert from 12V to 3.3V and might be expected to achieve an efficiency of 93%. Three PoL converters, each 80% efficient, would be used to deliver 6A at 1.2V, 1.5V, and 1.8V. The two stage power losses for such a system are about 9.2W and the efficiency about 74.4%. In contrast, the single stage equivalent, figure 2, converts directly from 12V to the target output levels, at an efficiency of 85%. Power losses are reduced by nearly half, to 4.76W. In addition, the elimination of one power stage frees board space and reduces cost. The final solution is more reliable, due to a reduced component count and lower thermal stress.

It is worth noting that the simple ability to accommodate a wide input range is not sufficient to satisfy the needs of such a system. The real requirement is for high efficiency across the entire range. In the case of the SupIRBuck series, as figure 3 illustrates, the devices attain efficiencies of around 90%, even at an input voltage of 19V. Another historic shortcoming of PoL converters has been their inability to retain their efficiency across a range of loads. This is equally true at high and low levels of output current. For instance, in traditional converters it is not uncommon to find a drop-off in efficiency at both high and low loads in the region of 10%. SupIRBuck converters address this problem, remaining highly efficient across the range of current requirements.

Whatever architecture is chosen, the designer of a PoL system faces some important design choices. The most fundamental is balancing the benefits of solutions based on discrete components against the use of monolithic converters. The use of discrete ICs and MOSFETs retains some benefits over the monolithic alternative. In particular, solutions can be built for flexibility in terms of current handling, by appropriate choice of MOSFETs. The engineer has more or less total control over the design parameters. However, the discrete approach requires relatively large board area. Its high part count also means that high reliability is harder to achieve, and that inventory management is more complex. Just as importantly, the job of the designer is substantially more difficult, so that design cycles and time to market are longer, and engineering costs are higher. Final-

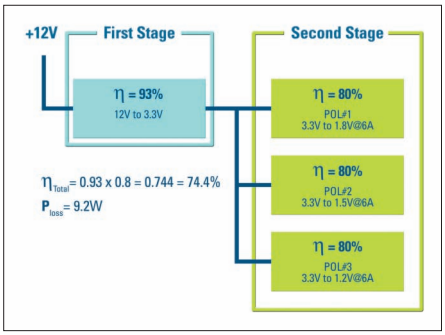


Figure 1. Architecture for two stage power conversion

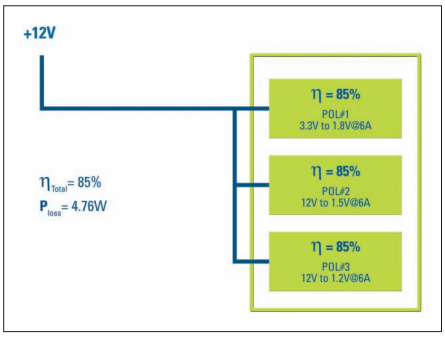


Figure 2. Architecture for single stage power conversion

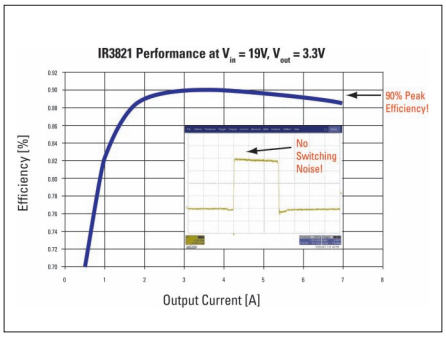


Figure 3. Diagram of peak efficiency of the IR3821 POL converter

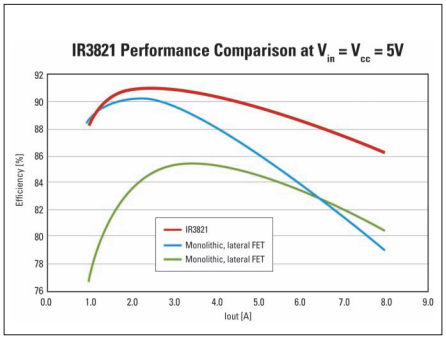


Figure 4. Performance comparison between IR3821 and monolithic, lateral FETs

ly, if the system does not perform as expected or fails in-service, it may be difficult to establish the causes and apportion responsibility. Monolithic solutions, in contrast, provide high density, design simplicity and give the user a single supplier with responsibility to solve any problems. Traditional designs, however, have had their weaknesses. Firstly, they can be inflexible and offer no easy upgrade options, for instance by increasing current delivery. Moreover, they can be significantly less robust than discretes: in particular, the lateral FETs deployed in most monolithic devices are not avalanche tested or rated. The SupIRBuck range addresses all of these issues by combining a high-performance synchronous PWM buck converter IC with benchmark trench MOSFET technology. Supplied in 5mm by 6mm QFN packages, the devices produce a 70% space saving over discrete alternatives, and a 35% space saving when compared with traditional monolithic solutions. Design flexibility is maintained by the ability to accommodate wide input voltage ranges, and by the availability of 4A, 6A, 7A, 9A, 12A and 14A versions in a common packaging footprint. Full load efficiency is 8% to 10% higher than existing monolithic solutions. The availability of multiple current versions is particularly useful in designs for which the current requirements are not known at the outset of the project – or, as is common, in systems in which they change during the design process. A common footprint enables system designers to migrate from one current rating to another without changing the PCB layout, whereas traditional monolithic or co-pack solutions feature different footprints for each current level. Increasing the current (to achieve higher performance or more functionality) or decreasing the current (to reduce cost) requires changing the layout, thereby increasing risk. Discrete solutions do allow the flexibility to change the MOSFET current rating – although not the PWM specifications. But perhaps more importantly, the discrete solution can also introduce EMI issues due to parasitic components such as board trace inductance. SupIRBuck reduces the board space, minimises the EMI problem and ensures first pass success while providing the same design flexibility as the discrete solution.

Enhanced features of the SupIRBuck series extend to its thermally enhanced package, which has a slim 0.9mm profile. This allows mounting on the backside of the motherboard for additional space savings: when combined with the ability to use single stage power conversion, this lower profile make the devices ideally suited for space constrained, high density applications. Devices across the range include pre-bias start up, fixed 600kHz switching frequency, hiccup current limit, thermal shutdown, and precise output voltage regulation. The designer can optionally choose variants with DDR tracking, programmable power good, and a lower 300kHz switching frequency to provide an additional 2A of output current capability. ■