It takes **two**...

... to tango. Or how to choose control and sync mosfets for point of load converters.

By **Carl Blake**.

As processors and fpgas lead the trend to sub 1V supply voltages, designers must optimise efficiency and increase power density in point of load (POL) converters. One way to achieve this is to ensure the sync mosfets in the POL synchronous buck converter are optimised to minimise losses.

To understand the demands for synchronous buck regulator mosfet optimisation in a POL application, consider the regulator in Figure 1, which we assume is supplying 1.2V to a cmos processor core from a 12V dc input.

The duty cycle for this arrangement is around 10 to 15%, which is also the period during which the control fet (Q1) is conducting. As a result, conduction losses in Q1 are relatively low. But Q1 operates under hard switching conditions, making switching loss the dominant mechanism in this part of the circuit. The sync fet (Q2) conducts for up to 90% of the cycle, hence conduction losses dominate. Meanwhile, zero voltage soft switching makes for negligible switching losses.

Broadly speaking, the control fet should be optimised for low switching losses, whilst sync fet conduction losses can be mitigated by designing for low $R_{ds(on)}$. In practice, synchronous buck operation demands additional properties from both the control fet and sync fet in order to minimise the losses arising from parasitic effects. These include $C_{dv/dt}$ induced turn on of the sync fet caused by Miller capacitance and inductive effects at the control fet's gate. Protection against these loss mechanisms is becoming more important as typical switching frequencies continue to increase.

Before the sync fet's gate voltage reaches its threshold, the body diode carries the load current and the drain voltage sits at -0.7V. Beyond the gate voltage threshold, the drain current gradually transitions into the fet channel and the drain sits at -100mV or less.

The reverse recovery loss of the body diode and the output capacitance losses are mostly dissipated in the control fet when it turns on, pulling the switch node up close to the supply voltage, reverse biasing the diode to turn it off and charging the output capacitance of the sync fet.

As conduction loss normally dominates, the natural response would be to choose a mosfet having a large silicon area to minimise $R_{ds(on)}$. However, a large silicon area results in a high charge, implying substantial gate driver losses. A trench mosfet delivers a favourable combination of low $R_{ds(on)}$ without storing excessive charge, but selecting a trench mosfet with the lowest possible on resistance will not necessarily ensure the lowest losses in practice. A suitable sync fet must also have high immunity to $C_{dv/dt}$ induced turn on, and this is closely linked to the gate charge.

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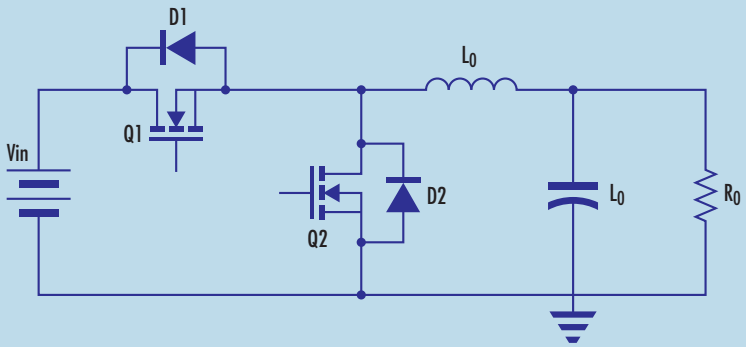
Figure 1: Basic regulator circuit

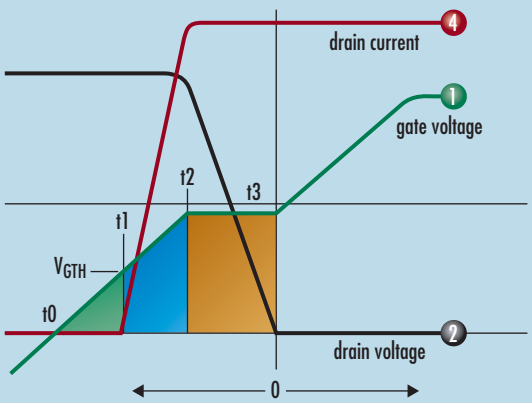


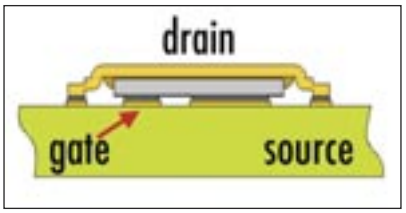
Losses incurred during $C_{dv/dt}$ induced turn on are appreciable in relation to the low $R_{ds(on)}$ performance of modern trench mosfets, even for a few nanoseconds. The key to avoiding $C_{dv/dt}$ loss is to ensure a low gate-to-drain charge (Q_{gd}) and a low charge ratio (Q_{gd}/Q_{gs1}). Q_{gs1} determines the amount of charge required for the gate to move from ground to its turn on threshold. Q_{gd} is defined as the C_{gd} charge when the drain voltage rises to 15V. As a rule of thumb, a charge ratio of less than 1.4 is considered sufficiently low to eliminate $C_{dv/dt}$ turn on.

Optimising the control fet

The turn off transition is a mirror image of the turn on process (see figure 2) and switching losses are incurred during the overlap between drain current and drain voltage. When the gate voltage rises past the threshold level, the drain current will increase from zero to the inductor current, whilst the drain voltage stays at V_{in}.

Figure 2: Control fet operation





Once drain current is equal to the inductor current, the drain voltage will start to collapse as the switch node voltage rises toward the supply voltage and its dv/dt will draw gate current through the mosfet gate-to-drain capacitance. During this period, the gate voltage remains at the Miller plateau. The switching transition is complete when the drain voltage falls to near zero due to the product of I and $R_{ds(on)}$.

In figure 2, Q_{gs2} is the gate charge accumulated as the drive voltage continues to increase beyond threshold and Q_{gd} is the gate charge accumulated on the Miller capacitor. The total switching charge is the sum of these two.

$$Q_{switch} = Q_{gs2} + Q_{gd}$$

The equation expresses all the losses incurred in the control fet throughout the cycle. It includes losses at turn on and turn off and confirms that overall switching loss is a function of switching frequency, input voltage and driver speed. In practice, however, a trade off is required between conduction loss and switching loss.

Packaging considerations

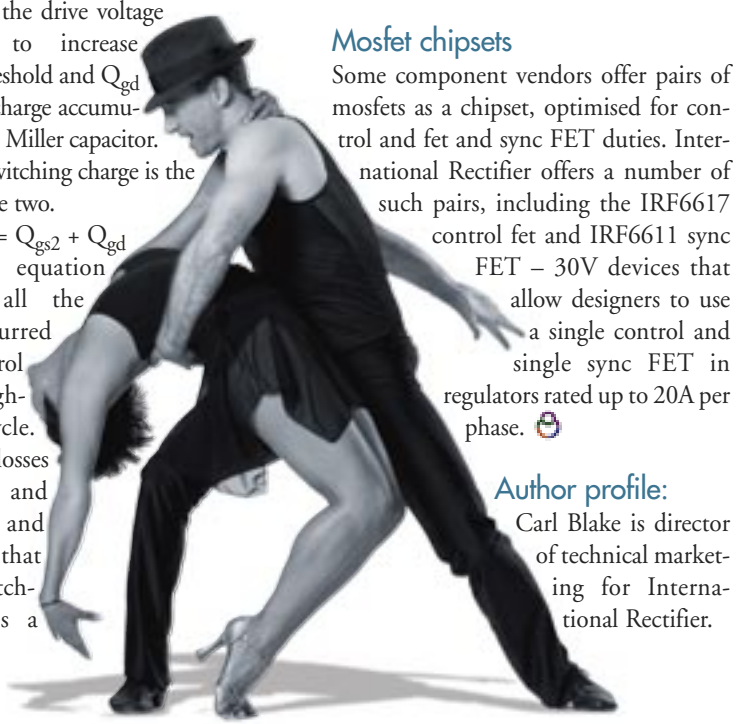
Mosfet packaging has a key role to play in optimising efficiency and increasing power density in POL converters. The PowerPak package, for example, which exposes the drain terminal to allow direct soldering to the board, delivers a 20% reduction in package resistance. This reduces junction-to-pcb thermal impedance compared to so8 packages and takes advantage of the pcb's heatsinking properties.

The DirectFET package (see left) goes further by flipping the die and exposing both gate and source to enable direct soldering to the board. The exposed drain terminal is connected directly to a metal can that extends down to the board and can be soldered to a heat spreader pad on the pcb. The DirectFET package reduces die free package resistance to 0.15mΩ, inductance to less than 0.1mH and junction-to-case thermal resistance to less than 1°C/W for the gate and source connections and 1.4°C/W for the drain.

The package also enables a convenient technique to minimise common source inductance – a system level phenomenon that depends on how the driver is connected to the control fet.

Mosfet chipsets

Some component vendors offer pairs of mosfets as a chipset, optimised for control and fet and sync FET duties. International Rectifier offers a number of such pairs, including the IRF6617 control fet and IRF6611 sync FET – 30V devices that allow designers to use a single control and single sync FET in regulators rated up to 20A per phase.



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