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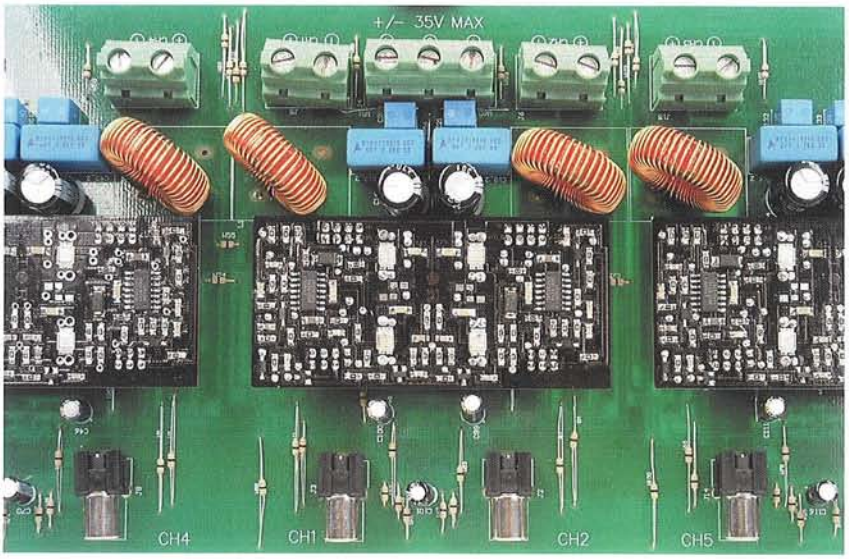

Figure 4: The resulting compact and lightweight 100W+100W amplifier demonstrates the advantages of class-D amplifiers over class-AB.

Eliminating Unwanted Spikes

The amplifier's output current determines its switching mode. In ZVS (zero-voltage switching), the output current is always smaller than the inductor ripple current. In hard switching, the output current is greater than the inductor ripple current.

In ZVS, inductive kick back—not the opposite-side MOSFET—drives commutation. The switching-current waveform looks much cleaner and does not contain shoot-through current during the body diode's reverse-recovery interval.

In hard switching, turning on the MOSFET starts with the reverse recovery interval during which the circuit removes minority carriers that accumulated in the body diode during dead time. There is no large inductance in the reverse-recovery current path to reduce the peak current, resulting in large spikes in the current waveform.

THD+N as diagnostic

The amplifier's THD+N curves are good indicators of circuit performance anomalies. For example, the circuit that Figure 2 characterizes operates with ZVS with outputs to 2 watts. THD degradation evident beyond the 2-watt level indicates a performance anomaly due to hard switching.

Poor THD+N performance at low power suggests a fundamental problem, such as bad grounding or PWM jitter. High THD+N at very low power indicates a high audible noise floor. In this region, operating with ZVS, the problem is likely in the PWM modulator or an earlier stage.

The THD+N bump at the transition between ZVS and hard switching suggests that noise from hard switching is disturbing the PWM signal. In this case, check the power stage's current path, particularly a current loop between the positive and negative busses through the two MOSFETs. Make sure that the current loop is as tight and narrow as possible. Then check if any sensitive blocks share a common impedance with switching elements particularly in the power stage. This type of noise-coupling mechanism is a particular concern in the source path of the low-side MOSFET and in the ground of the high-side gate driver's floating supply.

Clean Gate Drive

A clean switching waveform requires a clean gate drive. Remember that a MOSFET operates in its linear region during switching transitions. Remember also that the MOSFET—a gain element—shares a common impedance with the gate-drive loop and the output-current loop.

The common impedance in the MOSFET's source connection is inductive and provides negative feedback that decreases the switching speed by subtracting from the gate-drive voltage during the drain-source voltage transition. This can induce ringing with capacitive terms such as the MOSFET's gate and output capacitances. Minimize the common impedance in the MOSFET's source path by applying good high-frequency PCB design techniques. In this environment, small surface-mount FET packages are advantageous.

What to Share, What Not to Share

In a stereo amplifier design, common impedances among the audio channels are also problematic. Route the two channels separately to attain good audio performance (Figure 3). In a switching topology, it is always good practice to use separate closed-current paths for each switching leg in order to avoid coupling noise into an adjacent channel.

Unfortunately, simply separating the routings for each channel can weaken the design with respect to EMC due to switching-current waveforms' broad spectral components. This particularly applies to ground design. Those separated ground routes need high-frequency couplings to each other. A 1nF to 10nF ceramic surface-mount capacitor is a good choice for the switching artifacts, but does not couple audio-frequency signals, which would diminish the primary purpose of the separate grounds.

Combining these three fundamental facets of class-D design—device selection, noise reduction, and PCB design—a 100W+100W amplifier can fit in a sleek daughter-board module (Figure 4).

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How Do You Design a 100W + 100W Class-D Amplifier

High quality Class-D comes of age

The traditional Class-AB has been the stalwart for many years now. With power efficiency becoming also of age, there is now the technology to deliver great quality with power efficiency.

By Jun Honda, International Rectifier

The efficiency advantage Class-D amplifiers hold over Class-AB designs is irrefutable and, through this trait, switching-amplifier topologies have earned much of their market share. Less intuitive is that a reasonably well crafted switching amplifier can outperform a Class-AB audio power amplifier by providing both better linearity and lower output impedance.

As with any high high-fidelity amplifier topology, competitive linearity figures result from careful attention to details of the circuit's behavior: A PWM-drive and a couple of MOSFET switches banging between the rails doesn't quite get you there. However, with today's class-D IC controllers, the topology has come of age, and excellent results are attainable without heroic efforts during the design cycle.

Better linearity is, of course, only a part of the class-D amplifier's story. In many applications, such as flat-screen television, the topology's efficiency advantages drive the growing adoption rate: A 100W class-D power amplifier at full power delivers about 95% of its input energy to its load, as compared to 65 to 75% for class AB. At 1/8 output power—an operating point more typical of average use—the efficiency of class-D falls to about 85%. Under the same output conditions, however, class AB delivers load energy with only 25 to 30% efficiency. Flat-screen monitors suffer temperature-induced color shifts and poorly tolerate class-AB-amplifier dissipation.

Class-D's efficiency gains come at the cost of greater signal processing bandwidth: Class AB amplifiers for many applications need only provide a signal bandwidth of 10 to 20 kHz. High-end linear amplifiers may extend their signal-processing spectrum to 100 kHz or so. Class-D stages, on the other hand,

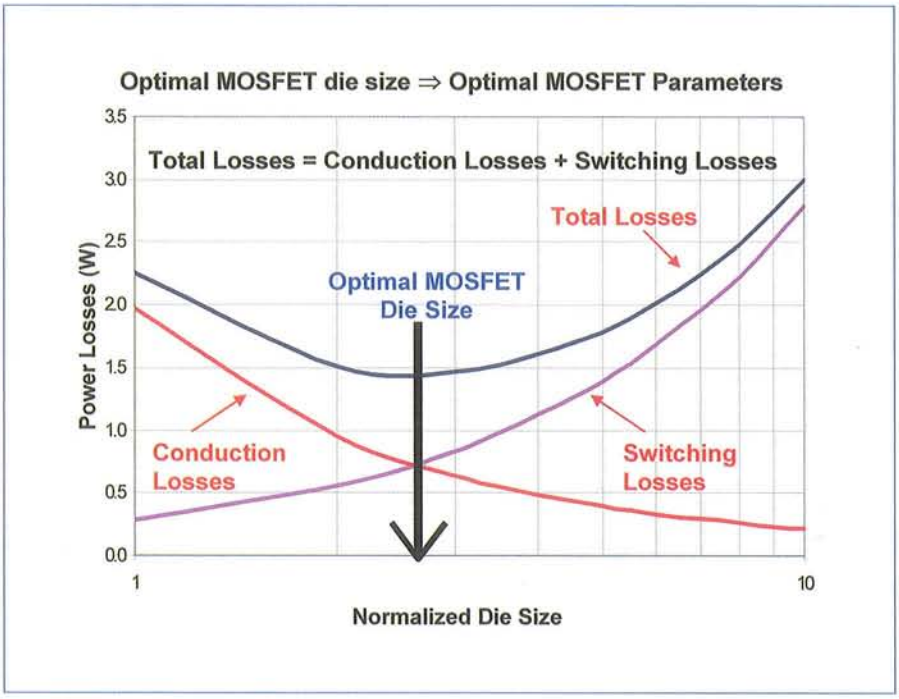

Figure 1: Select the MOSFET die size for equal conduction and switching losses.

must provide accurate signal processing into the MHz, which makes component selection and layout a more critical part of the design.

The successful completion of three tasks helps assure a successful class-D amplifier design:

- Optimizing the power-device choice
- Managing spikes from hard switching to ensure low THD and EMI
- Adhering to good high-frequency PCB-design rules
- A 100 W/ch design illustrates these three design challenges

The Bigger the Better?

Choosing the right MOSFET is essential to class-D amplifier design. A large MOSFET die does not always deliver the best efficiency. There is an optimum die size for a given design and choosing a device that is as close as possible to the optimal size is crucial to high efficiency.

A class-D amplifier's dissipation consists of switching- and conduction-loss terms:

$$P_{CONDUCTION} = \left(I_{D(RMS)}\right)^2 R_{DS(on)}$$

$$P_{SWITCHING} = I_D V_{BUS}\left(t_r + t_f\right) f_{SW} + C_{OSS} V_{BUS}^2 f_{SW} + 0.5 K Q_{RR} V_{BUS} f_{SW}$$

The tradeoff between switching and conduction losses is a function of the silicon process. However the terms follow characteristic curves independent of process node (Figure 1): Increasing the die size to minimize $R_{DS(on)}$ slows the switching speed due to the increased gate charge, which leads to longer switching transition times and greater switching losses.

Though the characteristic shape of the loss curves are independent of process technology, the absolute loss magnitudes do scale. Advanced silicon technologies provide better optimization points, which is important to class-D. This indicates that efficiency is still subject to improvement, unlike topologies that operate the output devices in linear mode. One way to assess the relative merits of competing MOSFET technologies is to compare products of $R_{DS(on)}$ and gate charge, Qg.

For a given rated power, the conduction loss is inversely proportional to the load impedance. The switching-loss components increase with PWM frequency. Therefore, the optimal die size is a function of rated power, load impedance, and PWM frequency.

For example, International Rectifier's IRF6645 trench MOSFET has a 14-nC gate charge and 28 milliohm $R_{DS(on)}$. At a 400-kHz PWM frequency, the loss distribution is 60% and 40% to switching and conduction, respectively.

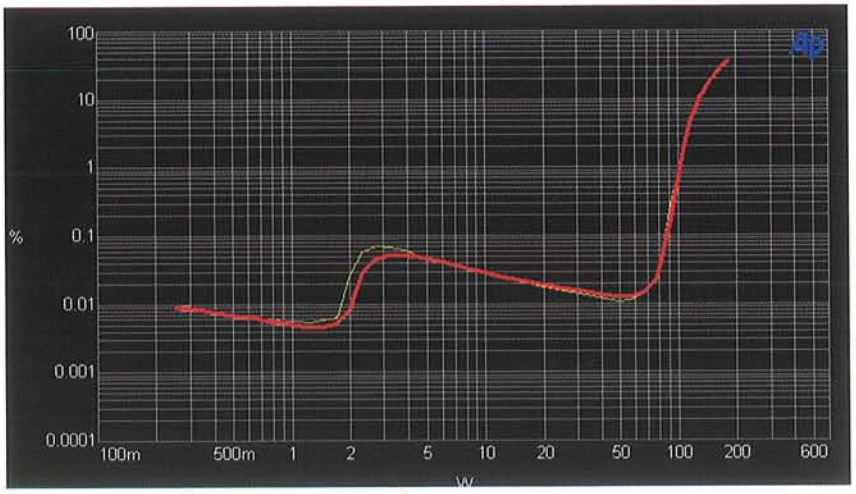

Figure 2: Use THD+N plots to diagnose performance anomalies such as noise from hard switching coupling into sensitive nodes.

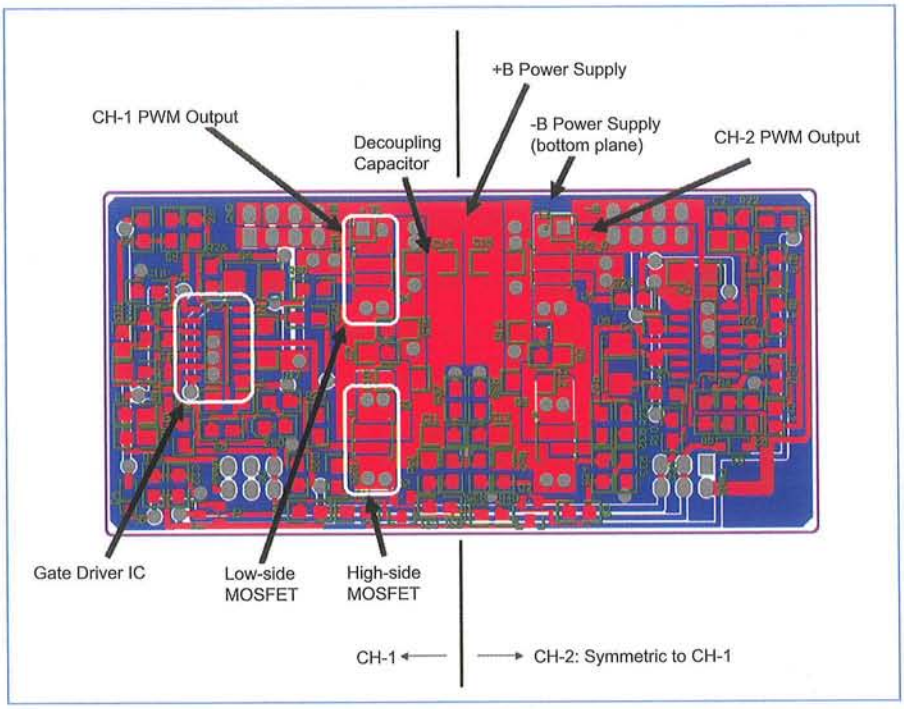

Figure 3: Route the two channels of a stereo amplifier separately to minimize common impedances but provide high-frequency coupling between the ground systems to reduce EMI.