DDR2 – The Next DRAM Generation

May 18th, 2004 – New York

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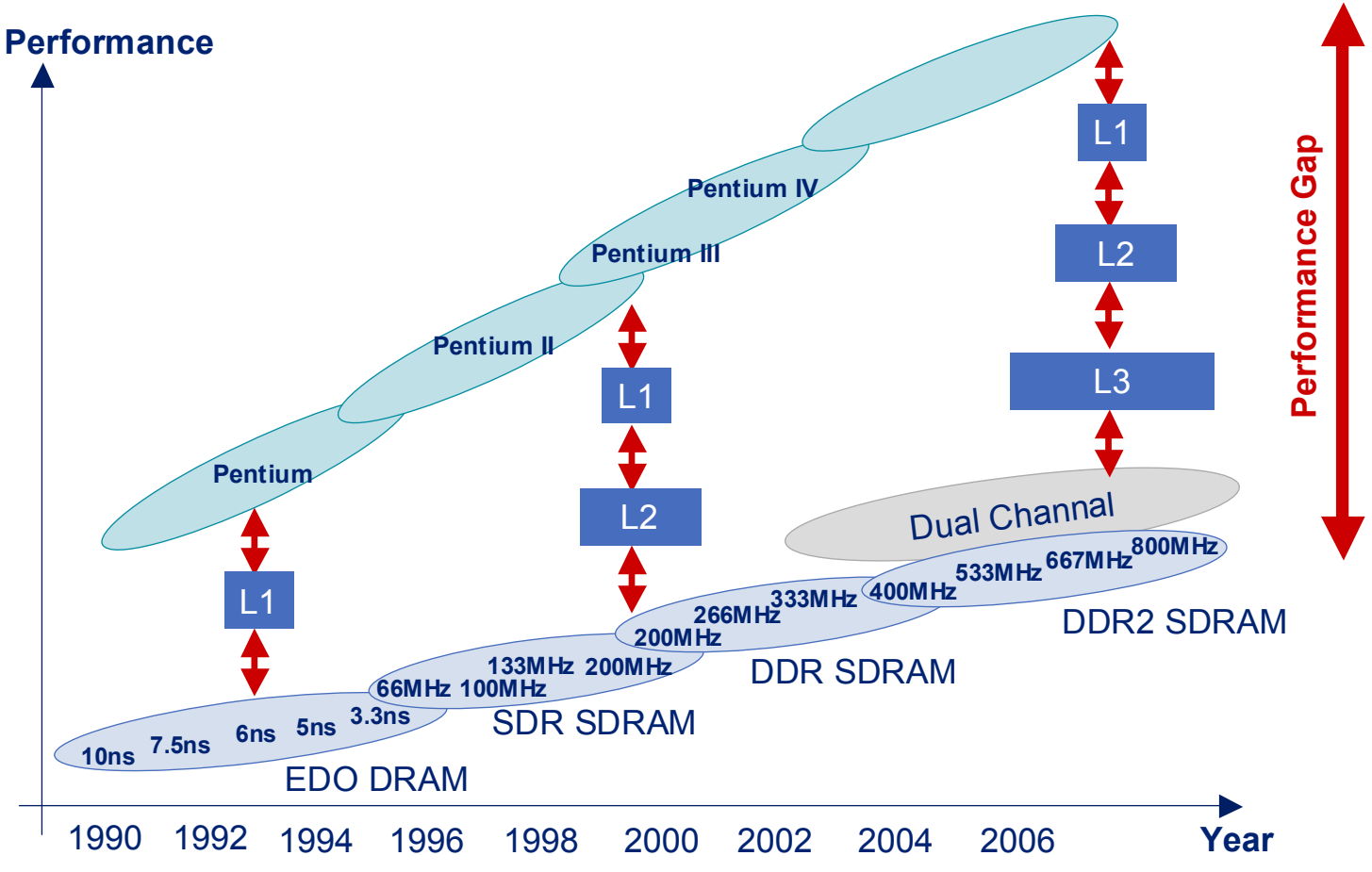
Joachim W. Binder
Director Investor Relations

The Performance Gap



Why DDR2?

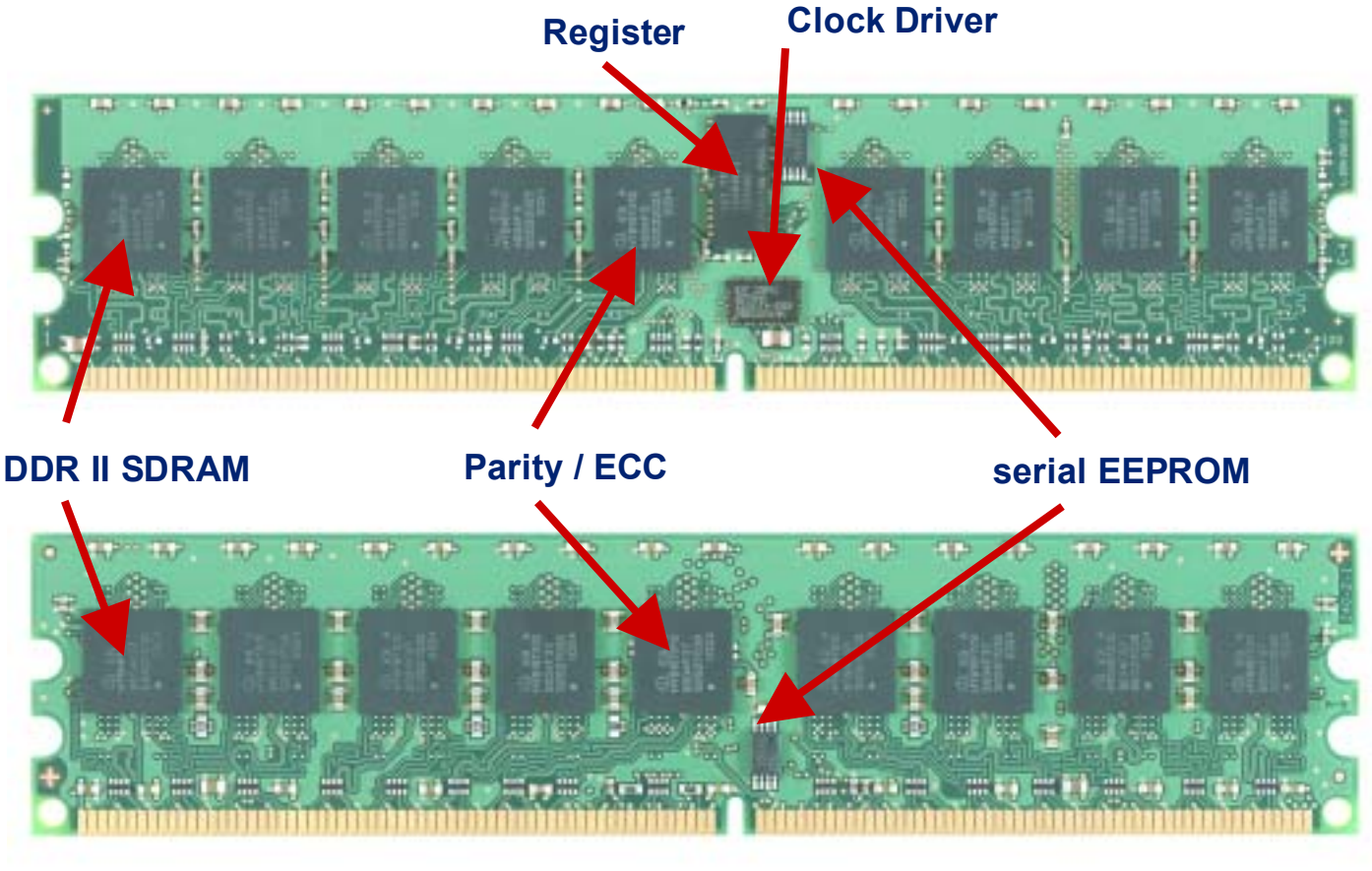
- To increase clock frequency up to 400 MHz
  (i.e. 800Mbit/s per pin bandwidth)
- To decrease power consumption
- To extend the physical limits by another 3 to 4 years
  (volume DRAM solution for 2005-2008)
- To improve bus utilization
- To keep cost, cost, and cost as low as possible

DDR Memory Module versus DDR2 Memory Module

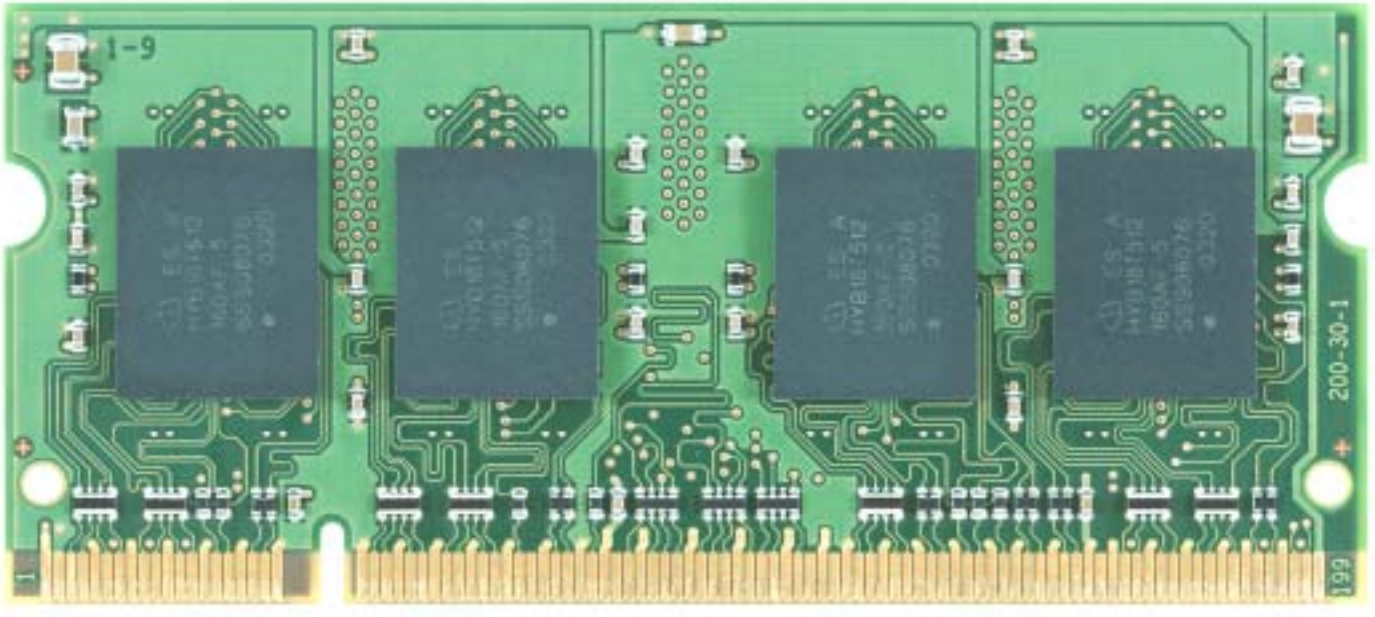
TSOP package (thin small outline package)

FBGA (fine-pitch ball grid array)

Memory Modules:
Registered (RDIMM) and Unbuffered Modules (DIMM)



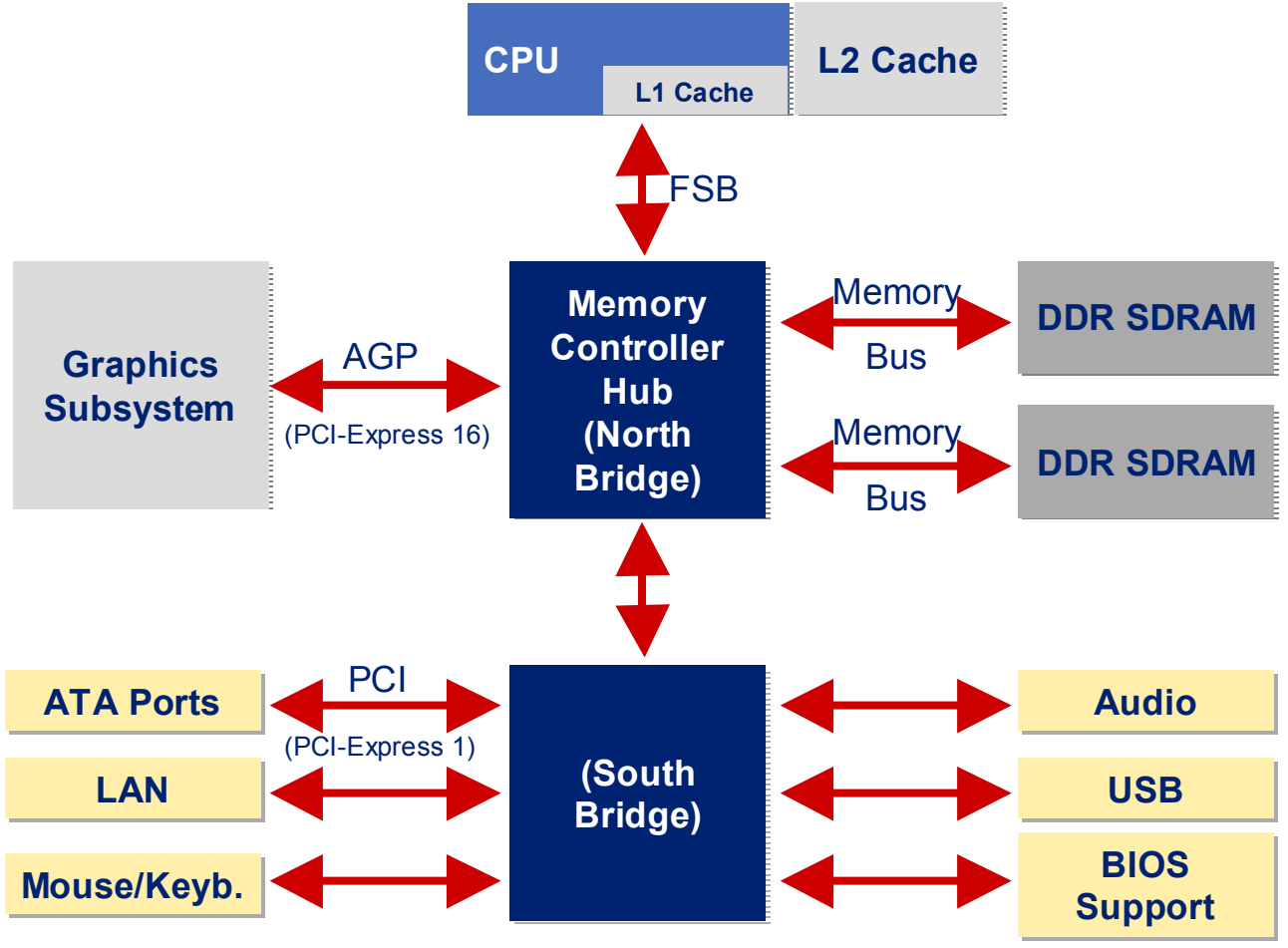
Notebook Memory Modules:
Small Outline DIMM (SO-DIMM)



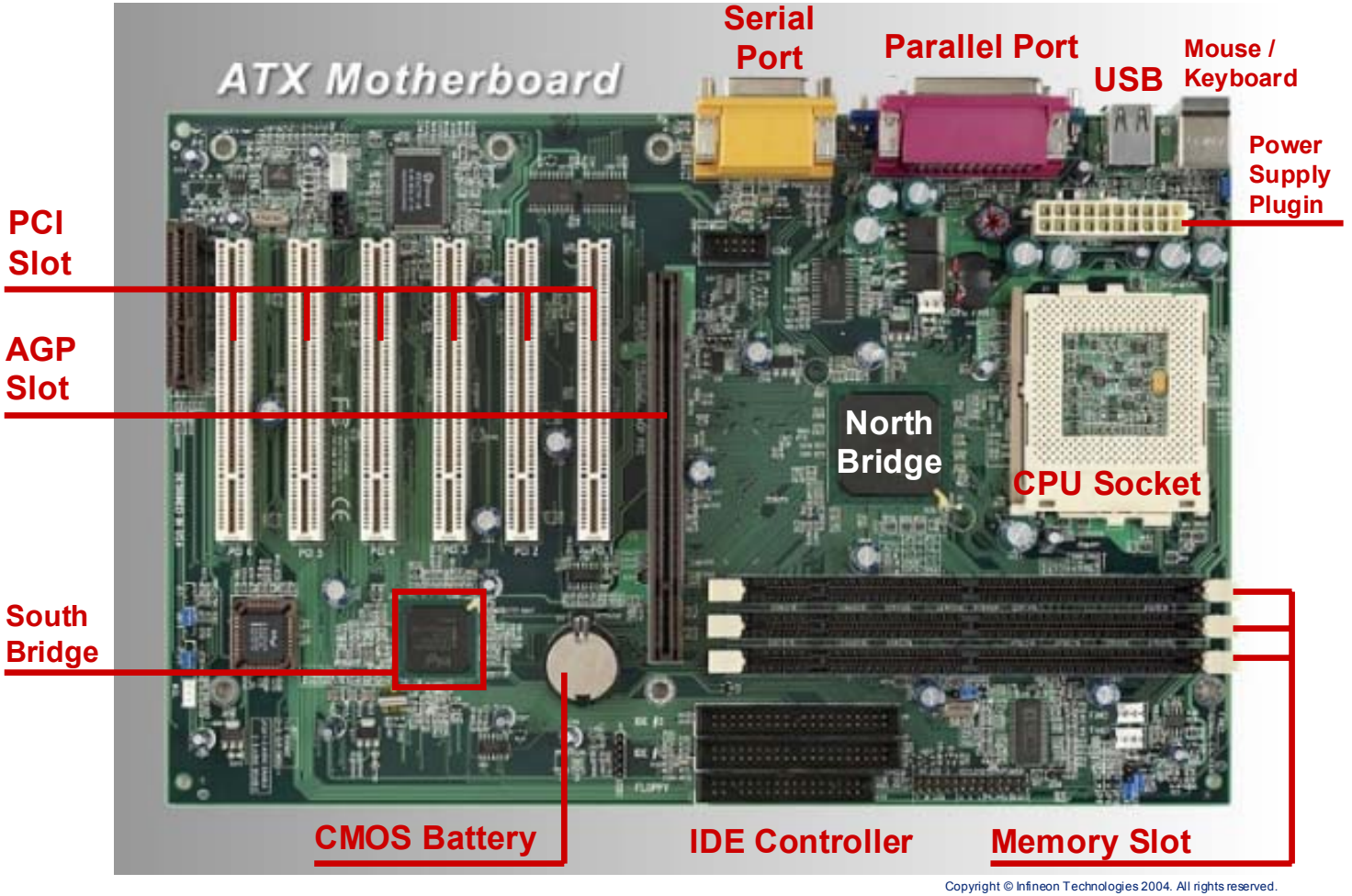
Different Target Markets

- **Server**
  - registered modules (RDIMM); x4, x8 devices
  - focusing on 400MHz devices this year
  - up to 32 modules (8 channels by 4 modules each) per machine; typ. 8 modules
- **Workstations**
  - registered modules; x4, x8, x16 devices
  - focusing on 533MHz devices this year
  - 2 to 4 modules per machine
- **PCs**
  - registered or unbuffered modules; x8, x16 devices
  - focusing on 533MHz devices this year
  - up to 3 modules per machine (Dual Channel: 2 modules per channel)
- **Notebooks**
  - x16 devices; x8 for high-density module only
  - focusing on 400MHz and 533MHz devices late 2004
  - up to 2 modules per machine

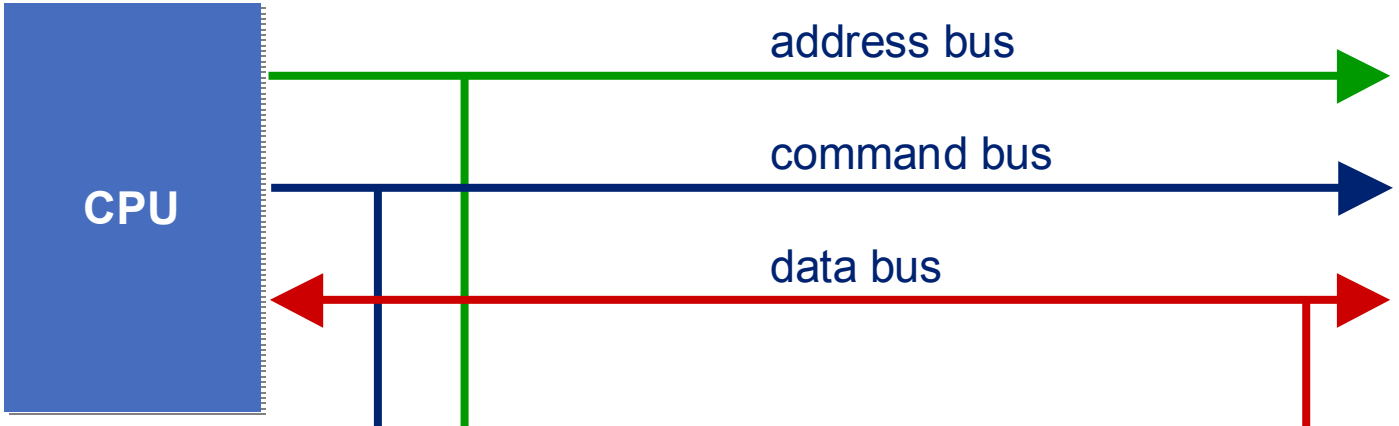
Block Diagram of PC System



PC Motherboards (ATX Format)

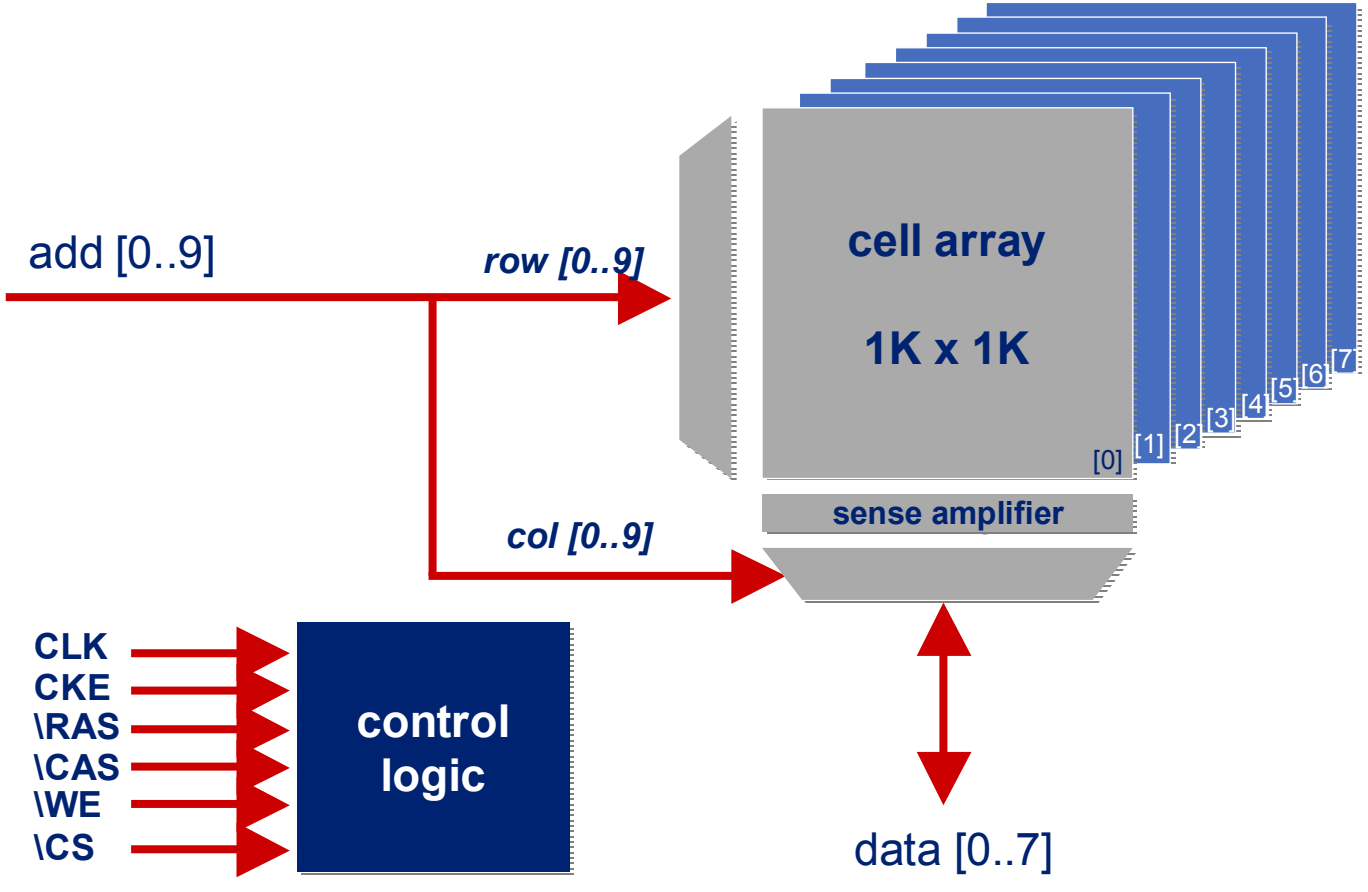


Processor / Memory Interconnection (von Neumann Architecture)

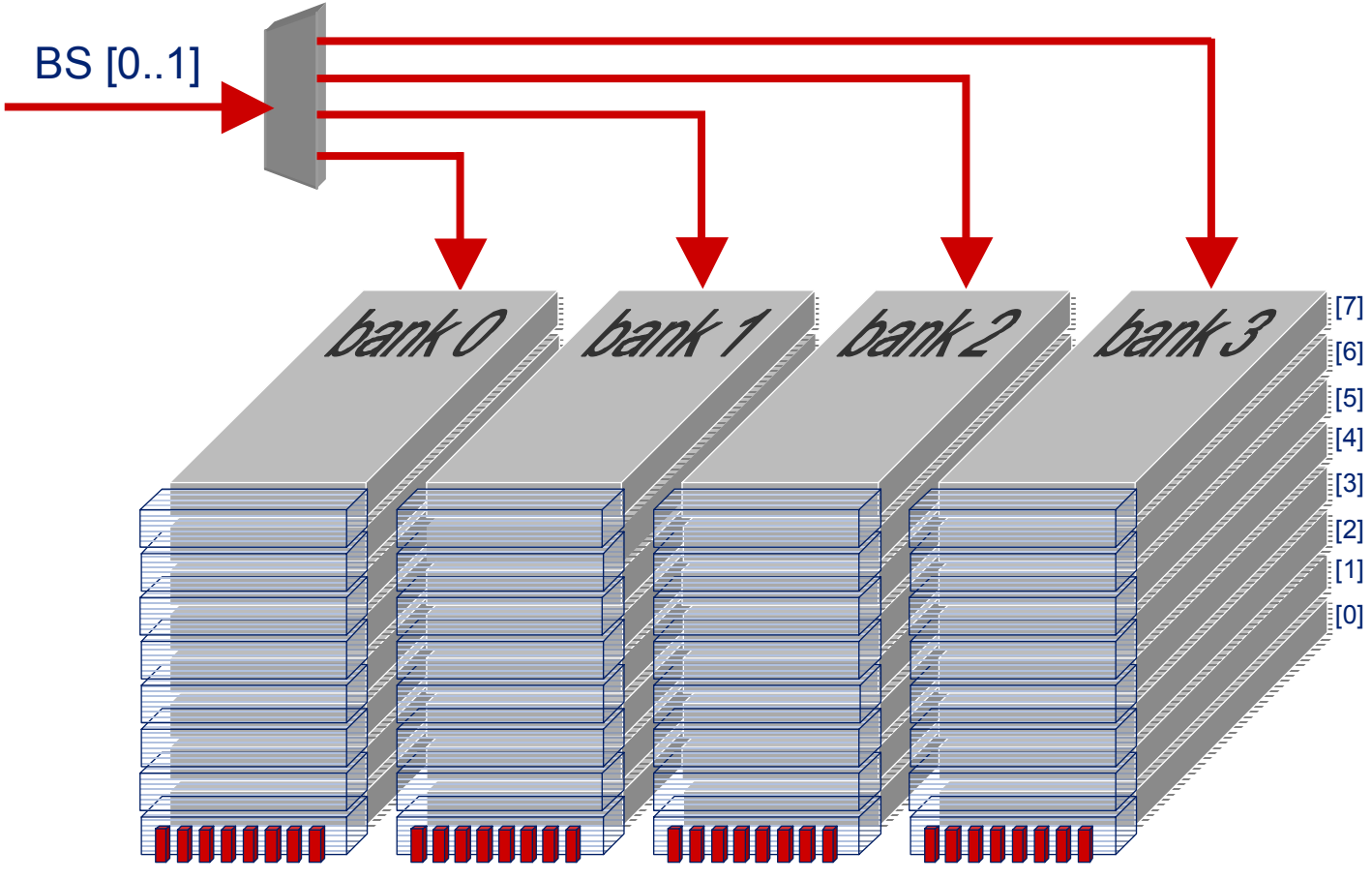


John von Neumann (1903 – 1957)

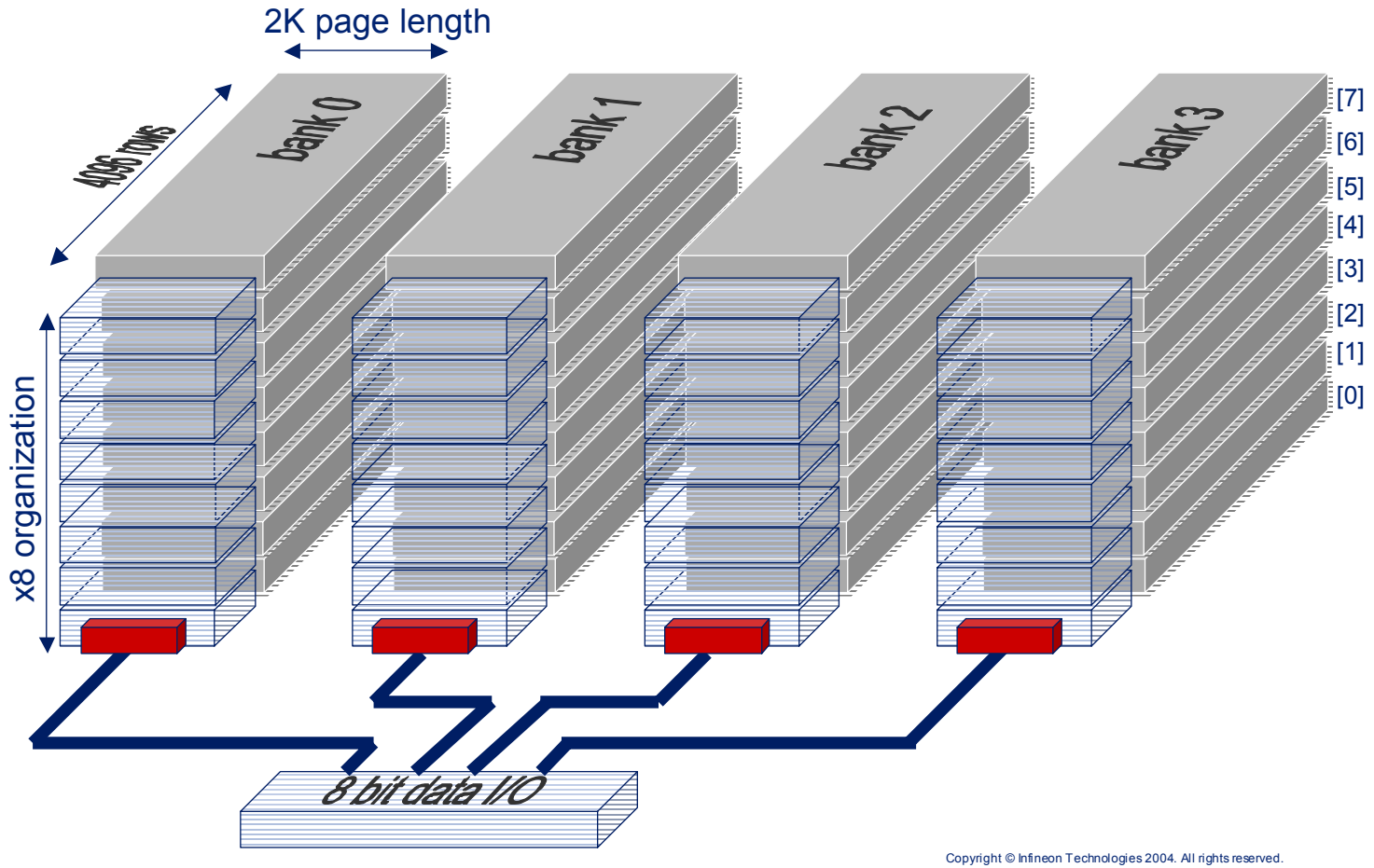
Block Diagram of a DRAM



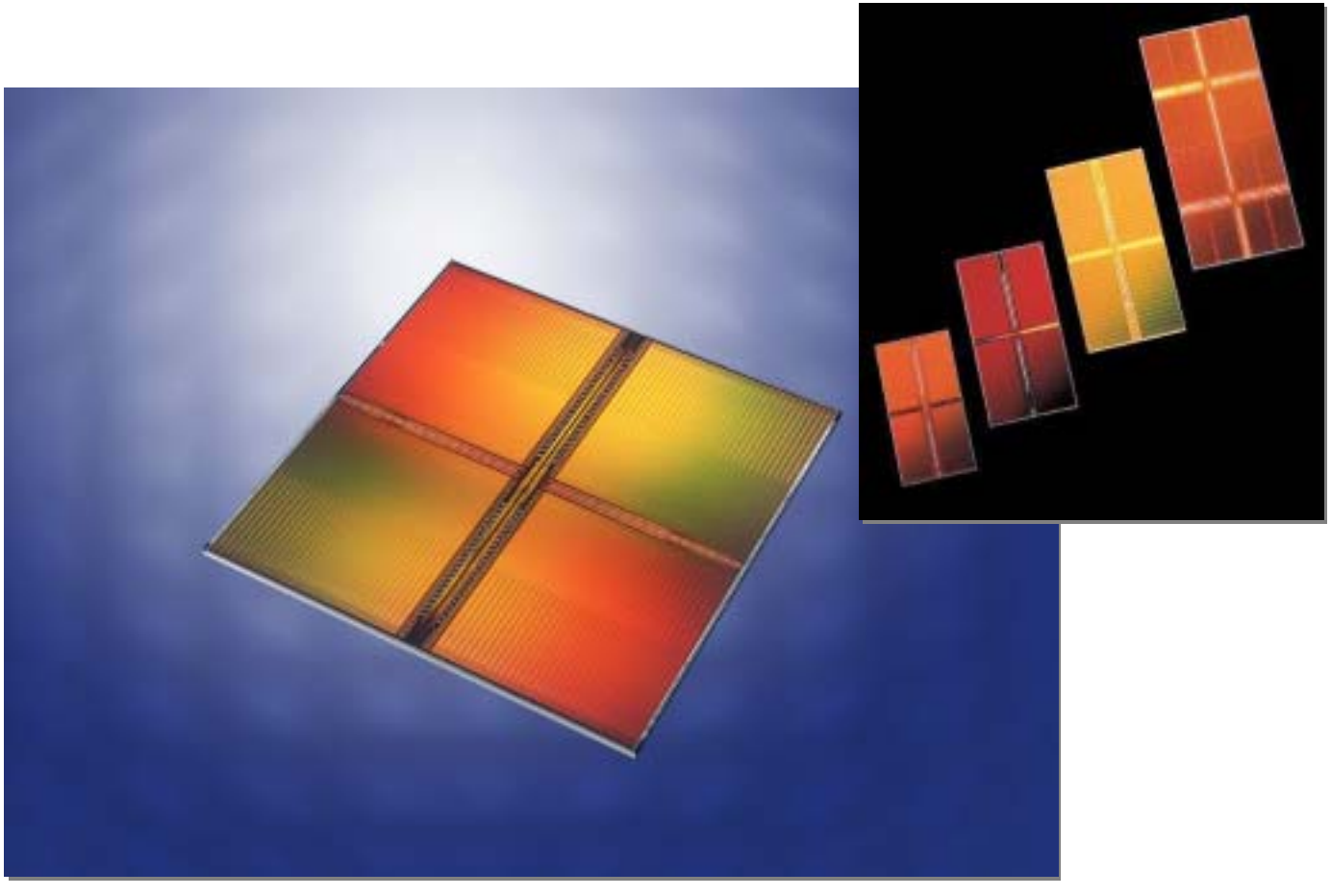
The Introduction of Banks
Independent Memory Sections Within the Chip



Example: 256 Mbit (32M x 8) = 4 x 4K x (2K) x 8
4 Banks, 4096 Rows, 2K Page, x8 Organization

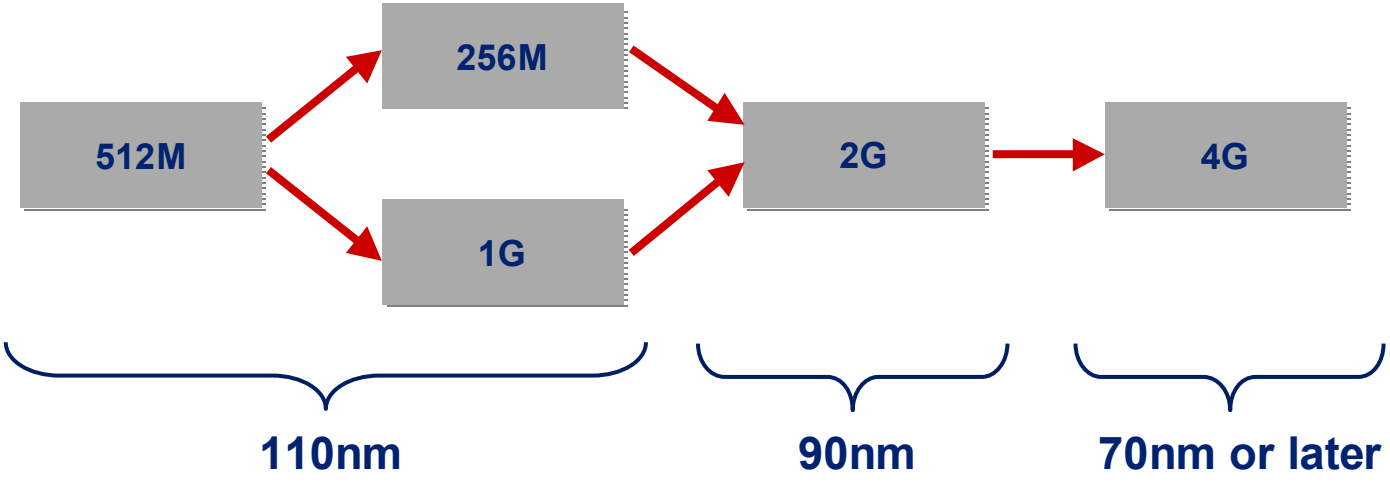


512M DDR2 SDRAM Die Photo



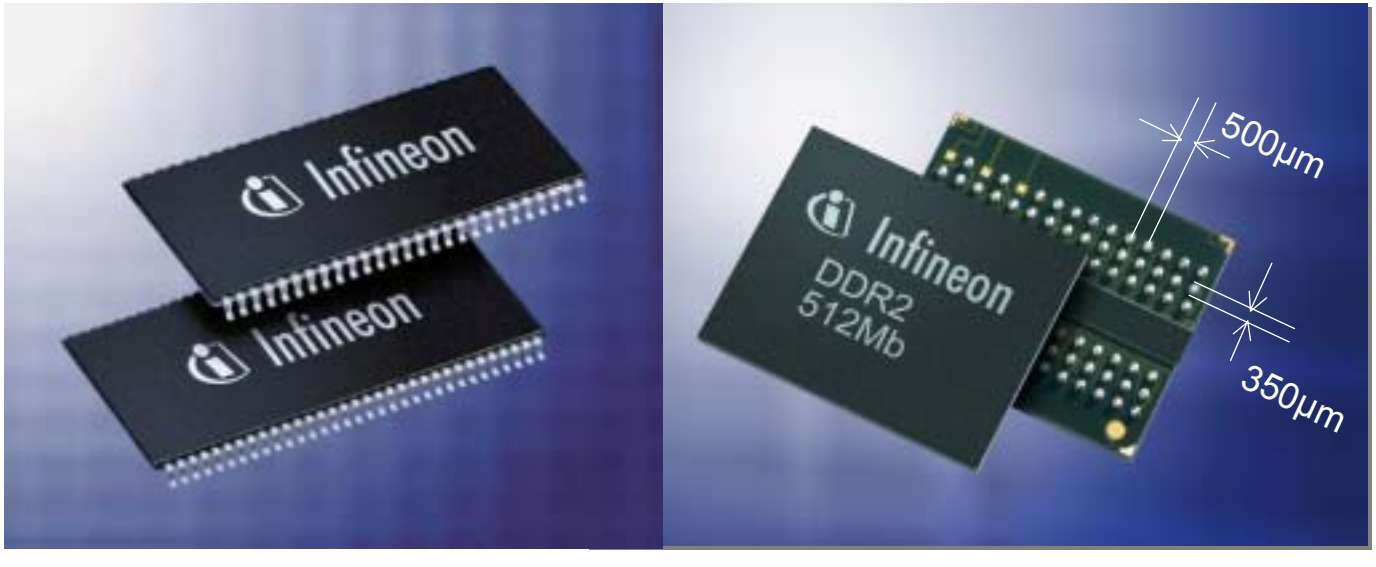
Changes from DDR to DDR2
a) Densities

DDR	DDR2	DDR2 Advantage
128M, 256M, 512M, 1G	256M, 512M, 1G, 2G (4G)	larger memory subsystems possible



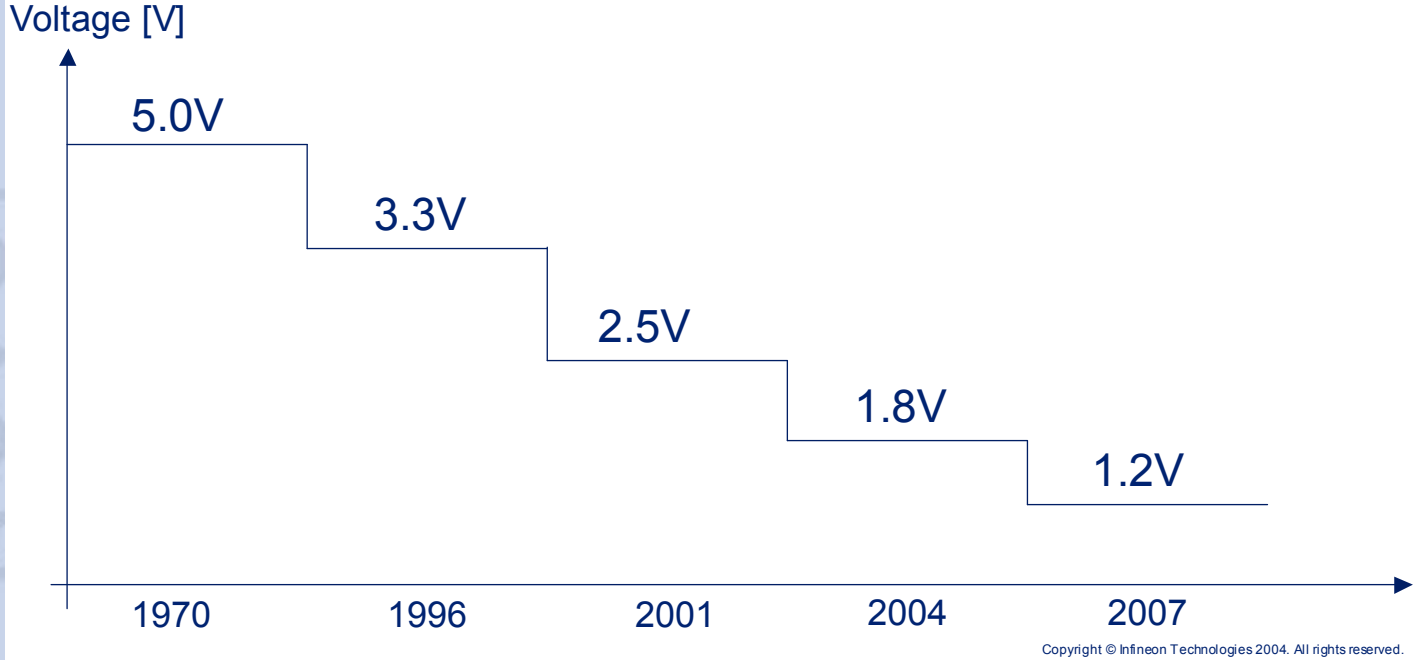
Changes from DDR to DDR2
b) Package

DDR	DDR2	DDR2 Advantage
TSOP (66 pins), some in FBGA (TSOP = thin small outline package)	FBGA only (FBGA = fine-pitch ball grid array)	better electrical characteristics; reduced parasitics; smaller footprint; stacked/dual die (two dies in a package)



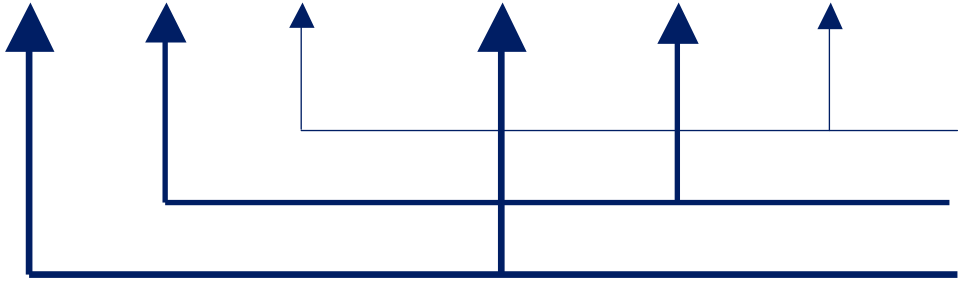
Changes from DDR to DDR2
c) Operating Voltage

DDR	DDR2	DDR2 Advantage
2.5V for core 2.5V for I/O	1.8V for core 1.8V for I/O	reduced power consumption



Changes from DDR to DDR 2
d) Clock Frequencies

DDR	DDR2	DDR2 Advantage
200MHz (100MHz) [100MHz], 266MHz (133MHz) [133MHz], 333MHz (166MHz) [166MHz], 400MHz (200MHz) [200MHz]	400MHz (200MHz) [100MHz], 533MHz (266MHz) [133MHz], 667MHz (333MHz) [166MHz], 800MHz (400MHz) [200MHz]	migration to higher-speed I/Os; more relaxed internal timing requirements



internal clock

chip clock

clock for data transfer

Impact on Front End Manufacturing (1)

- **Manufacturing challenges: none**
- **Overall die size increase: about 5-10%**
  - ~ 2-3% increase due to wider internal data busses because of 4-bit-data-prefetch
  - ~ 3-7% increase due to architectural changes
- **4-bit-data-prefetch:**
  - more relaxed internal timing, therefore better yields
- **On-die-termination (ODT): none**
- **I/O callibration (OCD): none**

Impact on Front End Manufacturing (2)

- **Reduced power consumption for comparable densities**
  - will go down due to lower internal clock frequencies
  - will go down (activation currents) due to shortened page length
  - will go down due to some I/O power savings
  - will go up due to higher densities
  - will go up due to higher clock frequencies

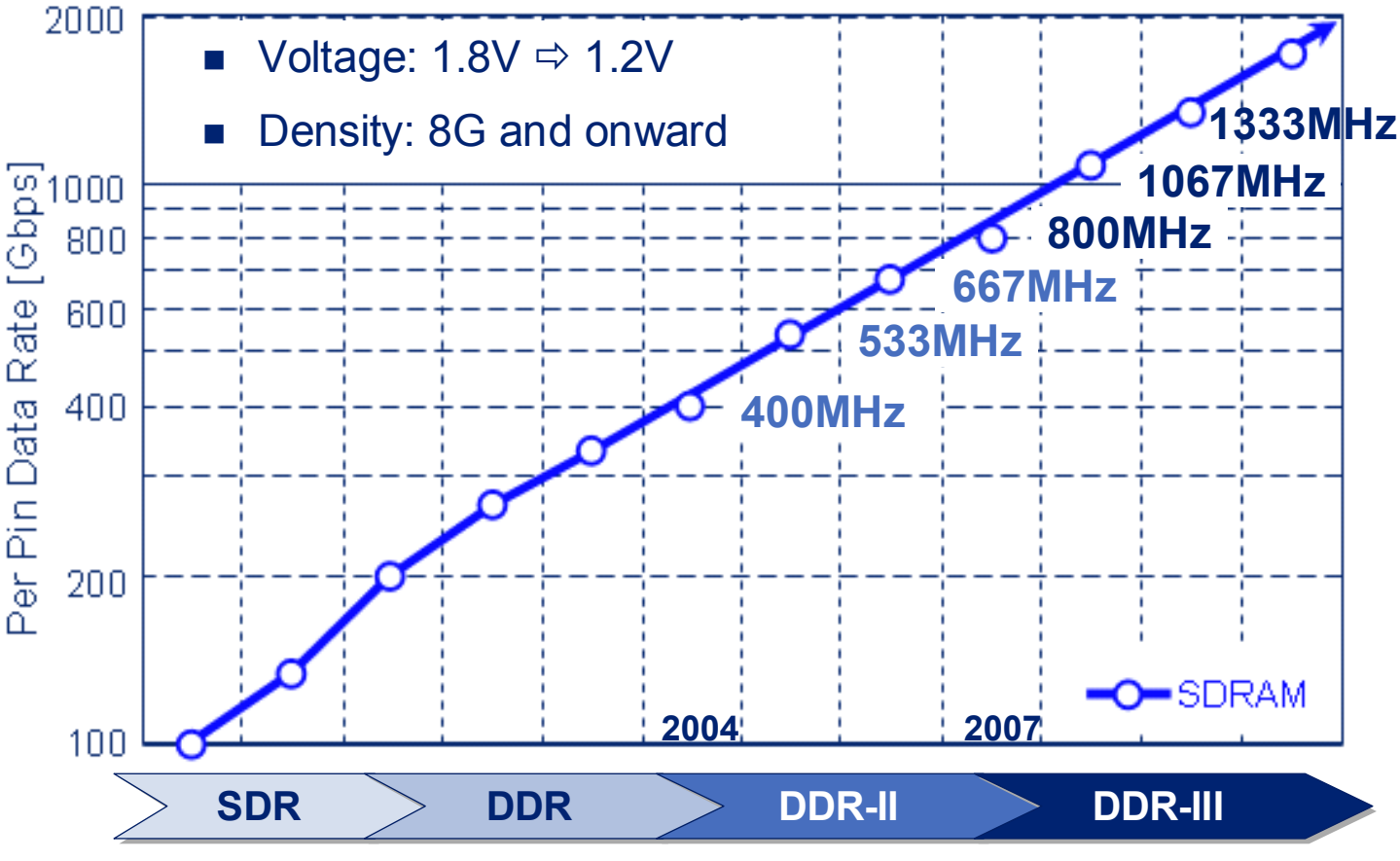
Impact on Backend Manufacturing

- **Testing time: none**
- **New testing tools required?**
  - No, basically not for 400MHz.
  - Perhaps, could be required for 533MHz.
    (depending on the state-of-the-art of the existing tools)
  - Yes, definitely for 667MHz and 800 MHz.
- **Packaging tools required?**
  - New packaging tools definitely required as FPGA is used only.
- **Packaging costs?**
  - Will go up as FBGA is more expensive as TSOP.

Conclusion

- Step from DDR I to DDR II has small impact on cost; major contribution comes from FBGA package.
- Step from DDR I to DDR II not significantly different than transition from SDR to DDR I with respect to volume ramp-up and price transition.
- There will be an initial price premium due to capacity limitation.
  With a DDR II share of more than 50% (expected for 2H05) premium will be close to parity.

Roadmap for DDR III



Validated DDR2 400MHz SDRAM Components

Bibliography

- DDR II memory boards validated by Intel:
  www.intel.com/technology/memory/ddr/valid/ddr2_dram_results.htm
- "Denali Memory Report":
  www.denali.com
- Technical notes about DDR II by Micron:
  www.micron.com/products/dram/ddr2sdram/technote.html

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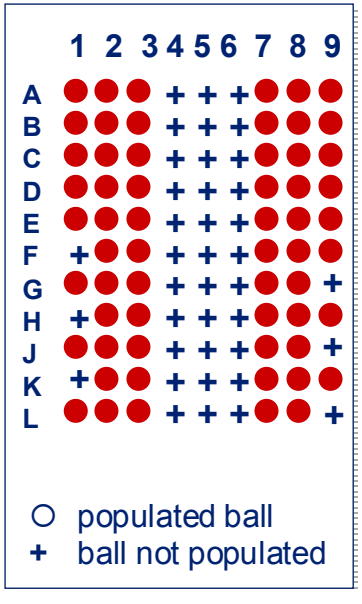
– Appendix –

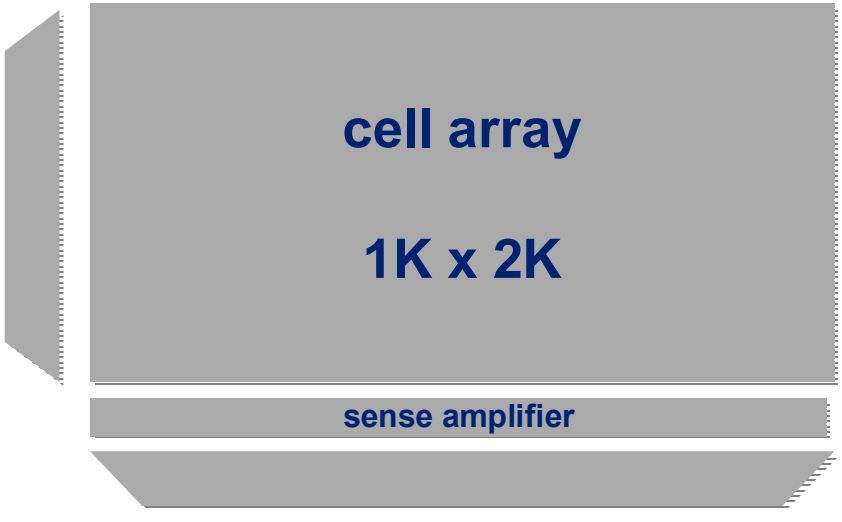
DDR2 Package Ballout for a x8 Device

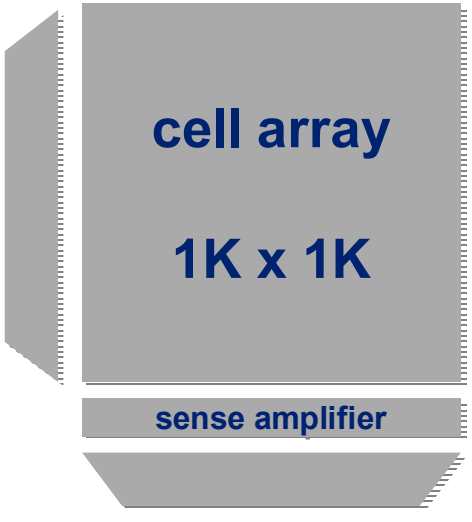


	1	2	3				7	8	9
A	V_{DD}	\RDQS	V_{SS}				V_{SSQ}	\DQS	V_{DDQ}
B	DQ6	V_{SSQ}	DM				DQS	V_{SSQ}	DQ7
C	V_{DDQ}	DQ1	V_{DDQ}				V_{DDQ}	DQ0	V_{DDQ}
D	DQ4	V_{SSQ}	DQ3				DQ2	V_{SSQ}	DQ5
E	V_{DDL}	V_{REF}	V_{SS}				V_{SSDL}	CK	V_{DD}
F		CKE	\WE				\RAS	\CK	ODT
G	BA2	BA0	BA1				\CAS	\CS	
H		A10	A1				A2	A0	V_{DD}
J	V_{SS}	A3	A5				A6	A4	
K		A7	A9				A11	A8	V_{SS}
L	V_{DD}	A12	A14				A15	A13	

Changes from DDR to DDR2
e) Page Size Reduction

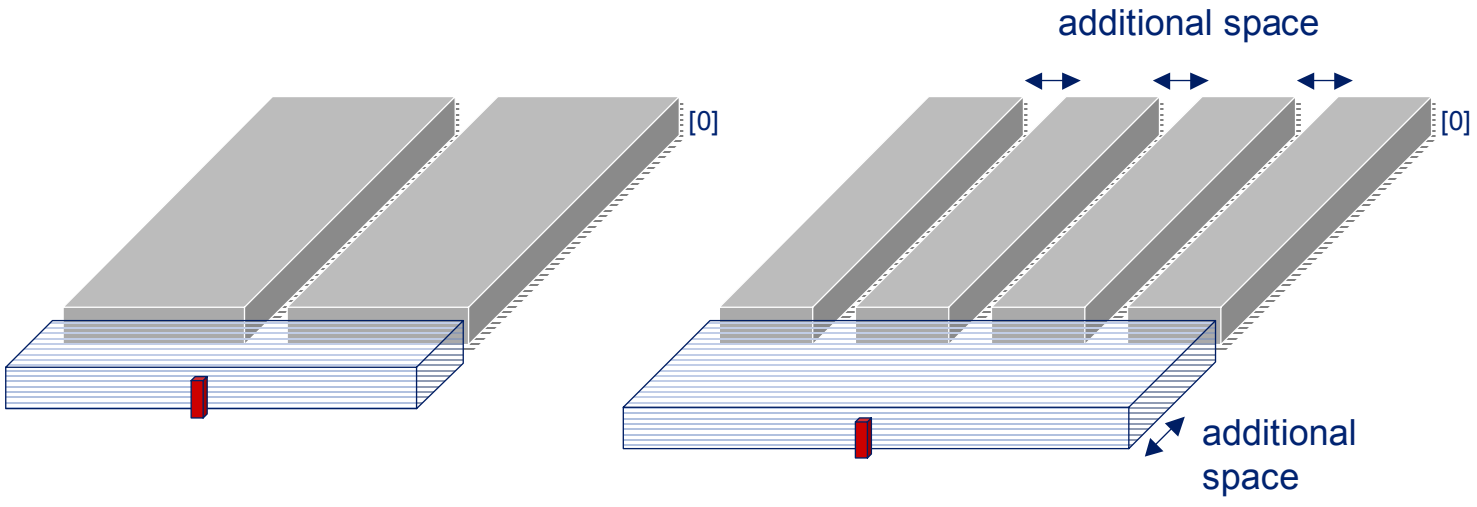
DDR	DDR2	DDR2 Advantage
256M: 1KB 512M, 1G: 2KB	256M: 1KB 512M, 1G, 2G: 1KB (x4, x8) 2KB (x16)	reduced activation power due to shortened page size





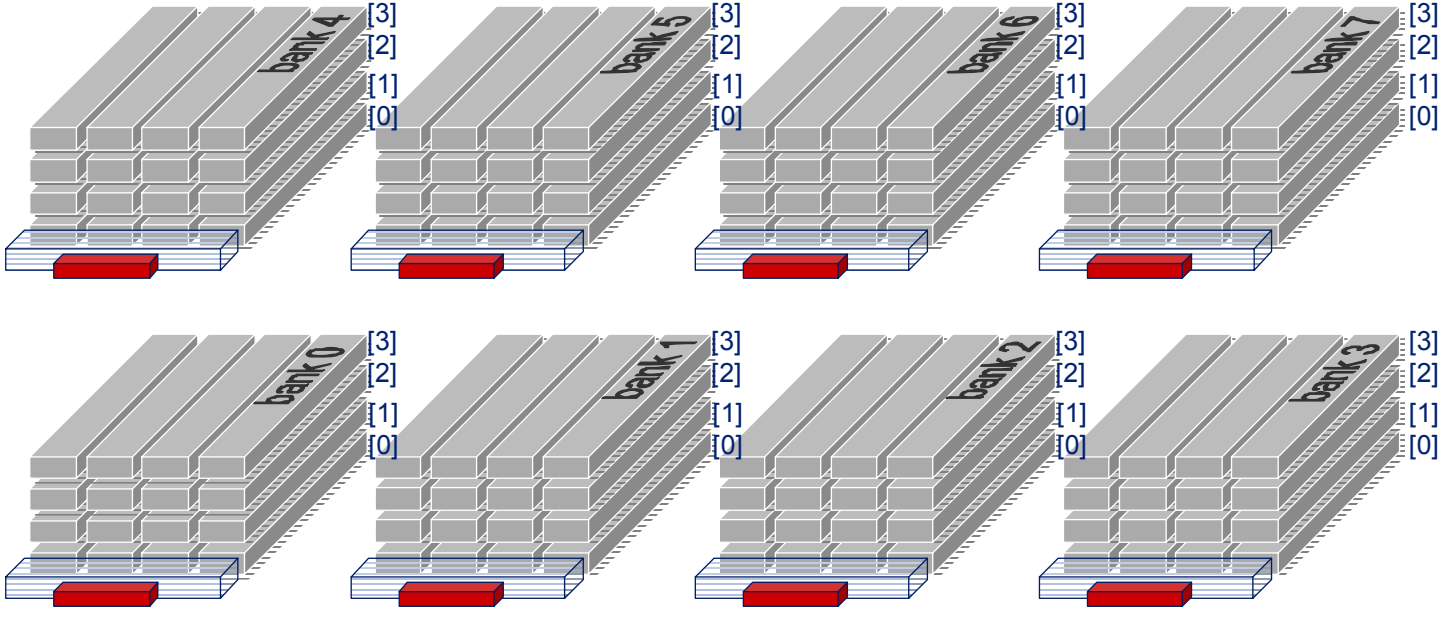
Changes from DDR to DDR2
f) Prefetch

DDR	DDR2	DDR2 Advantage
2 bit	4 bit	memory core internally operates only with half the frequency; reduced core speed dependency for better yields; reduced power consumption; internal data bus has to be doubled; slightly increase of the die size;



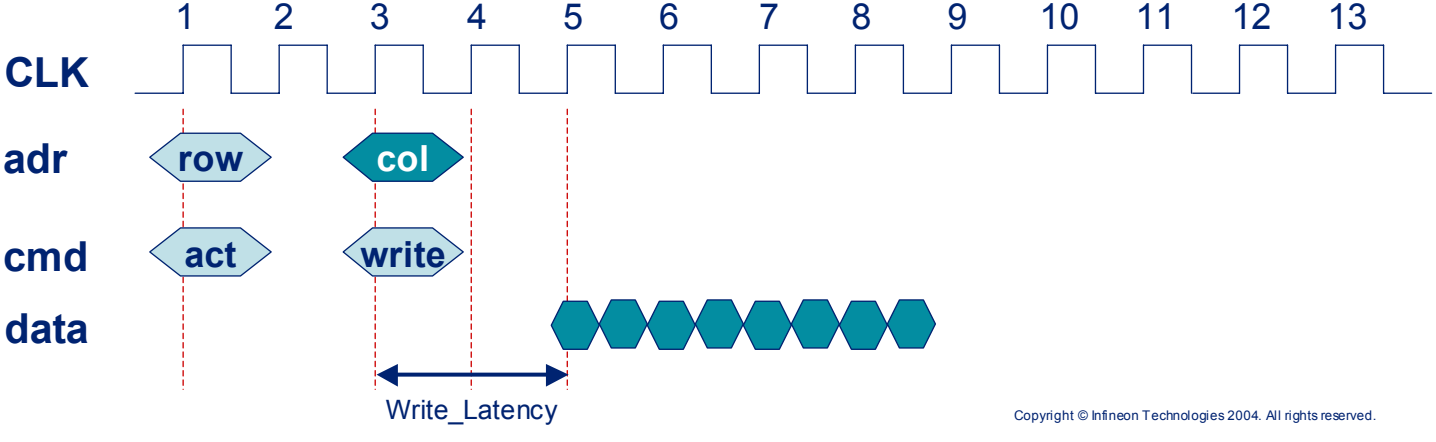
Changes from DDR to DDR2
g) Internal Banks

DDR	DDR2	DDR2 Advantage
256M, 512M, 1G: **4 banks**	256M, 512M: **4 banks** 1G, 2G: **8 banks**	8 banks give better performance than 4 banks



Changes from DDR to DDR2
h) Read and Write Latencies

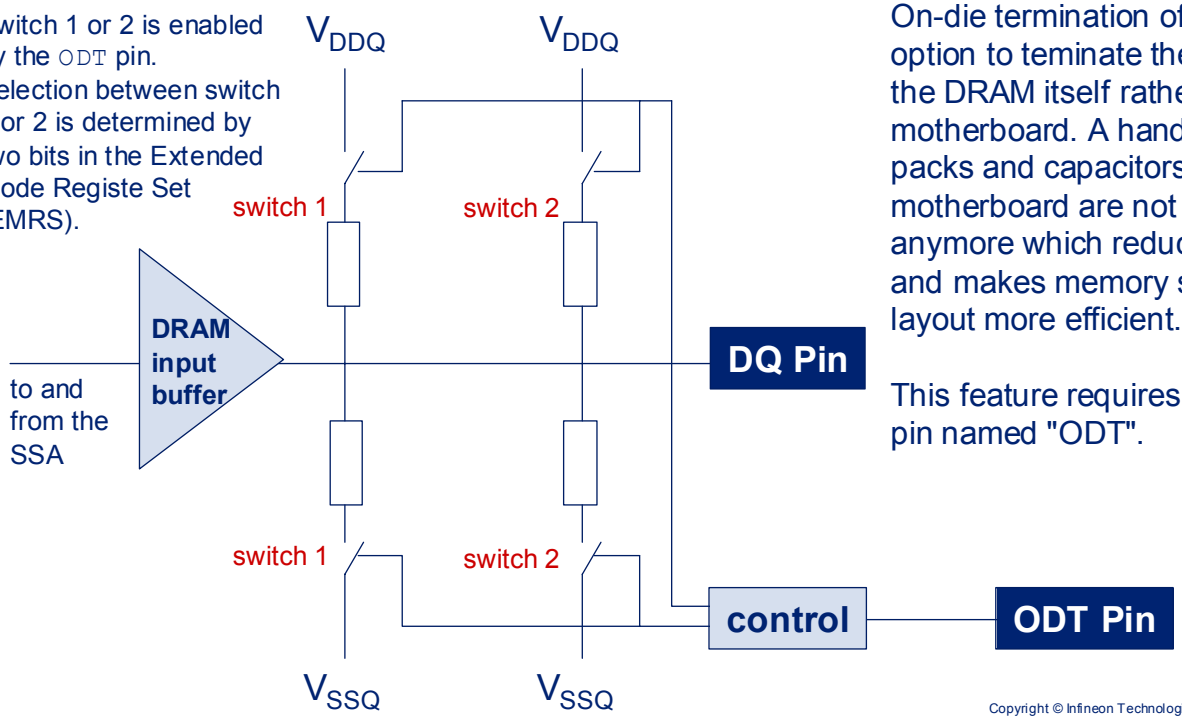
DDR	DDR2	DDR2 Advantage
Read_Latency: 2; 2.5; 3 CLK	Read_Latency: CL + AL CL = (3; 4; 5)	eliminating half-clock cycles helps speed internal DRAM logic, improves yields, and reduces test cost
AL not implemented	AL = (0; 1; 2; 3; 4) (AL = additive latency)	additive latency mainly used in server applications to improve command bus efficiency
Write_Latency: 1 CLK	Write_Latency = Read_Latency - 1	improves command bus efficiency



Changes from DDR to DDR2
i) On-Die Termination

DDR	DDR2	DDR2 Advantage
on-motherboard termination	on-die termination (ODT)	ODT for both memory and controller improves signalling and reduces system cost

Switch 1 or 2 is enabled by the ODT pin. Selection between switch 1 or 2 is determined by two bits in the Extended Mode Registe Set (EMRS).



On-die termination offers the option to teminate the signals in the DRAM itself rather than on the motherboard. A handful of resistor packs and capacitors on the motherboard are not necessary anymore which reduces some cost and makes memory subsystem layout more efficient.

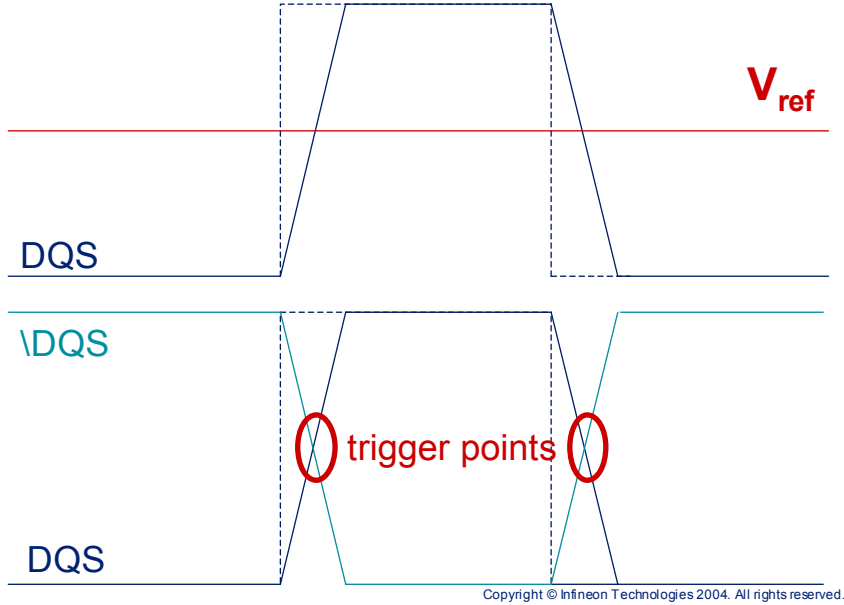
This feature requires an additional pin named "ODT".

Changes from DDR to DDR2
j) Data Strobes

DDR	DDR2	DDR2 Advantage
single-ended	differential or single-ended	improves system timing margin by reduced strobe crosstalk; increases pin count for the memory controller

single-ended data strobe

differential data strobe



Changes from DDR to DDR2
k) I/O Callibration (Off-Chip Driver Impedance Adjustment)

DDR	DDR2	DDR2 Advantage
no	off-chip driver (OCD) impedance adjustment; memory controller configured	enables system to align pull-up / pull-down drive strengths to nominal conditions; feature not expected to be widely used

Explanation

In DDR the output drivers have to confirm the minimum and maximum V/I curves defined by JEDEC commitee. Furthermore, due to process variations the R_{on} resistance can also vary from device to device.

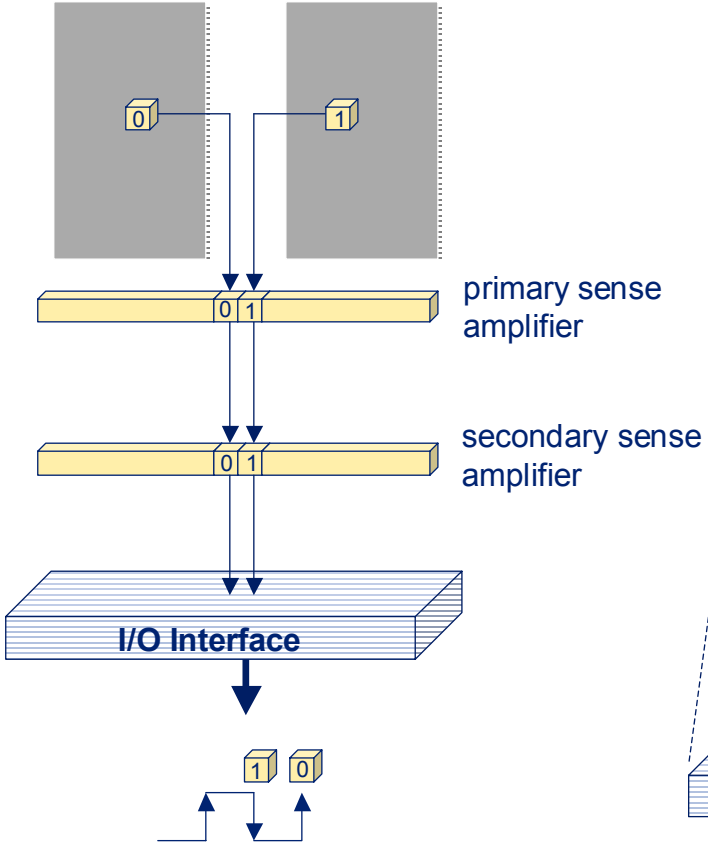
In DDR II the output driver R_{on} resistance can be adjusted and optimized for the system application. This new feature is called "OCD". Programming the OCD can be done via three bits in the Extended Mode Register.

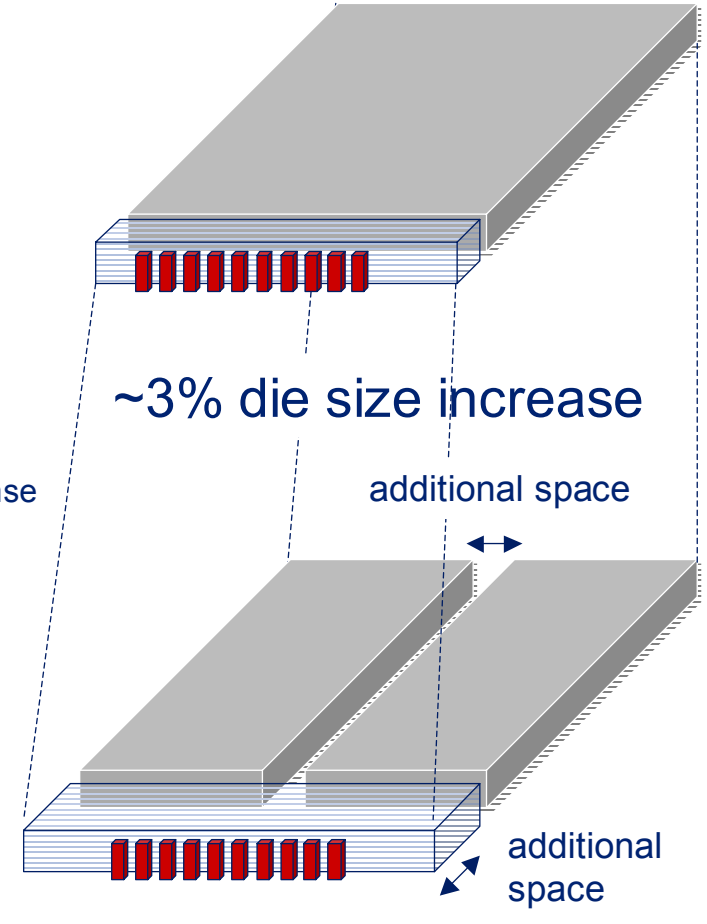
Since the R_{on} characteristic is a function of temperature and voltage, the R_{on} value can be re-adjusted any time it is needed during operation.

Changes from DDR to DDR2
I) Modules

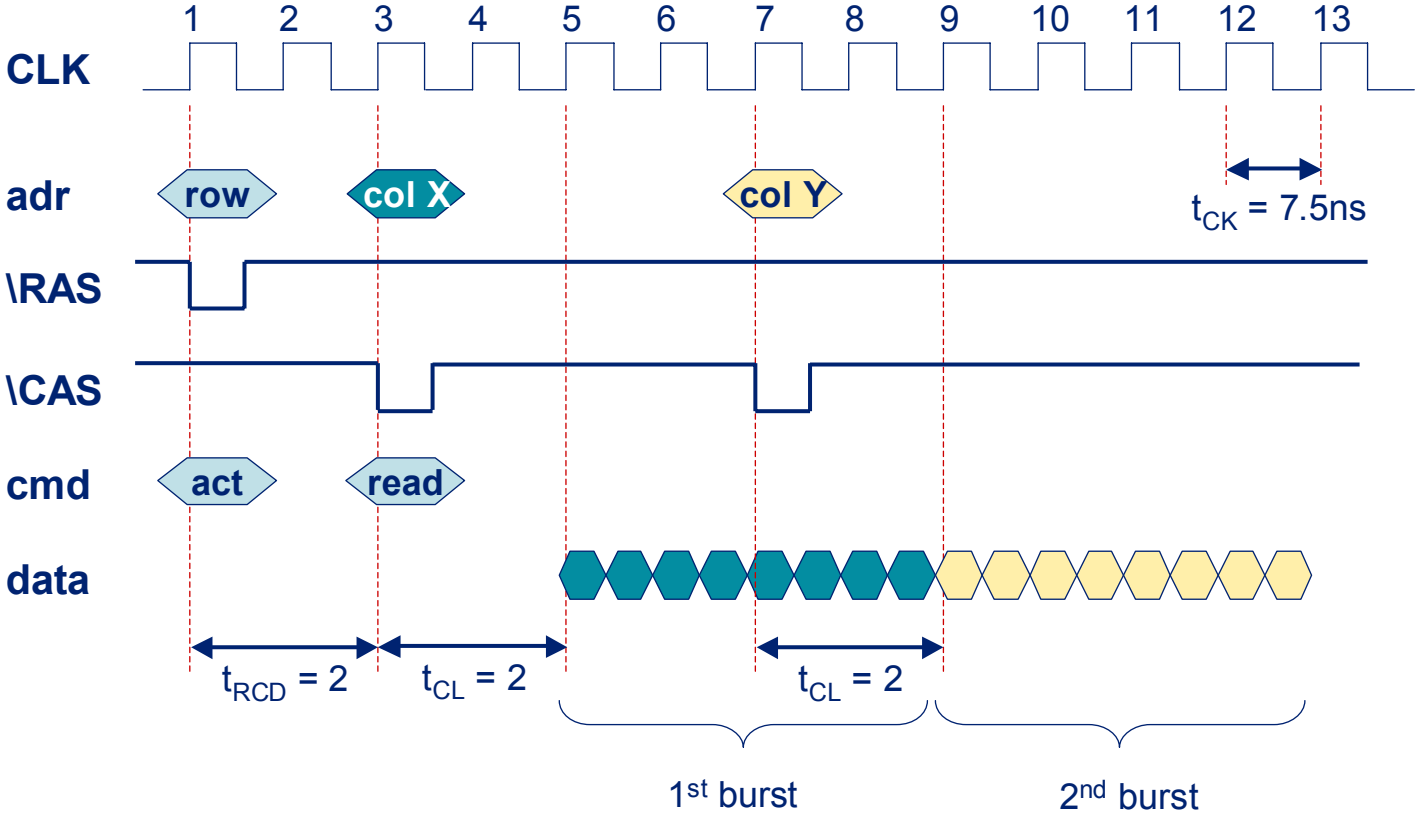
DDR	DDR2	DDR2 Advantage
184-pin unbufered 184-pin registered	240-pin unbuffeered 240-pin registered	modules are same length, with added pins;
200-pin SO-DIMM	200-pin SO-DIMM	DDR2 SO-DIMM is same connector;
172-pin MicroDIMM	214-pin MicroDIMM	different pinout as DDR
	244-pin MiniDIMM	

From SDR to DDR:
The Introduction of "Prefetch 2"

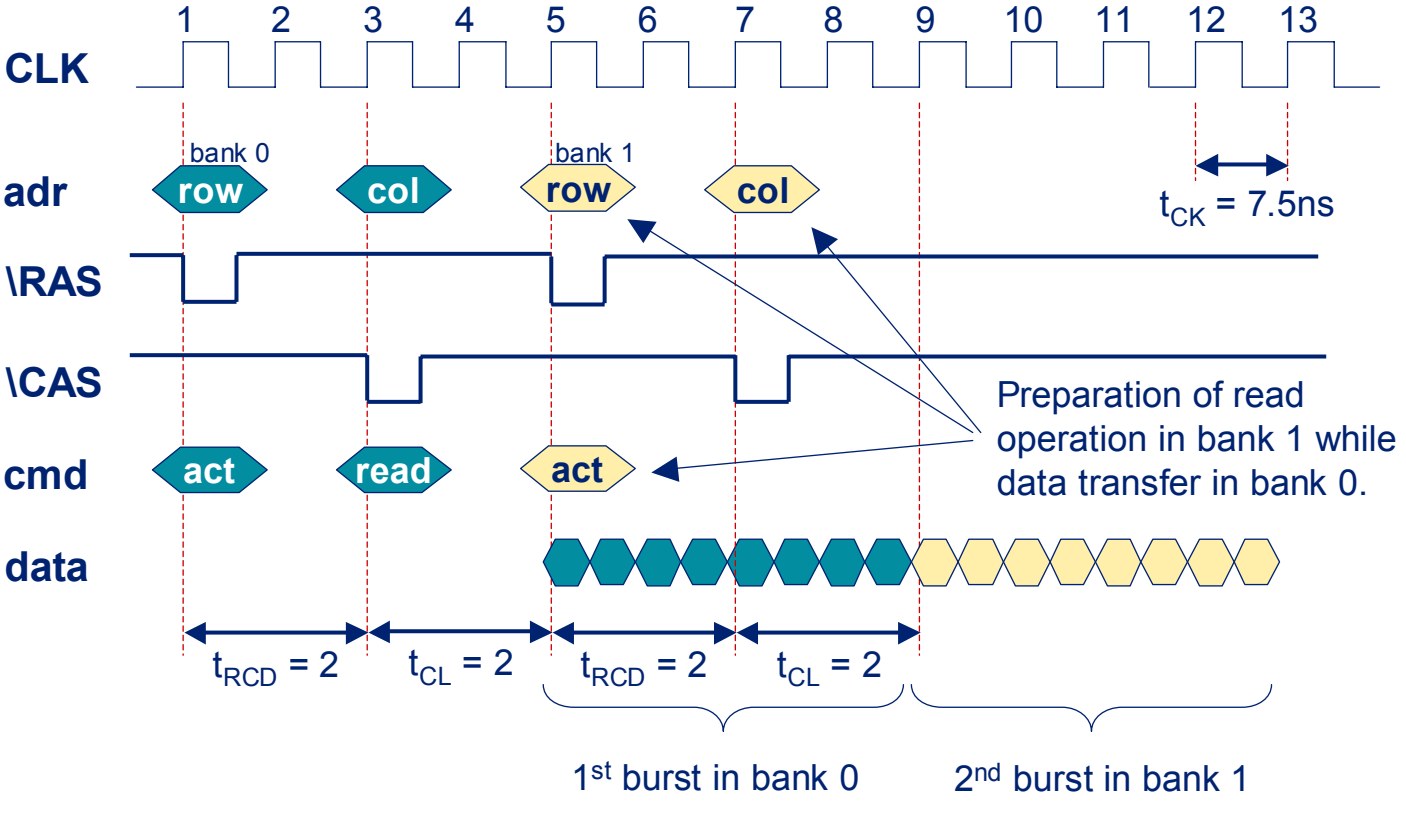




Latencies: t_{RDC}, t_{CL}
133MHz; Burst Length = 8; Page Hit; Same Bank



Latencies: t_{RDC}, t_{CL}
133MHz; Burst Length = 8; Page Hit; Different Banks



Latencies: t_{RDC}, t_{CL}, t_{RP}, t_{RC}
133MHz; Burst Length = 8; Page Miss