Worst-Case Test Conditions of SEGR for Power DMOSFETs

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***Abstract*—Heavy ion test results show worst-case test conditions for single-event gate rupture (SEGR) of power MOSFETs. Contrary to common belief, the worst-case ion condition for SEGR is not the ion with the deepest penetration depth in the device or highest LET at the die surface, but the ion beams with Bragg Peak positioned at or near the interface of the epitaxial layer and the highly doped substrate. The factors that have significant impact on SEGR thresholds are evaluated and discussed. The factors that are considered include: ion beam, drain bias, gate bias, ion species, ion range, surface LET and the construction layer of the power DMOSFET. An estimated worst-case ion range table for krypton, xenon and gold is provided for reference.**

***Index Terms*—MOSFET, Single Event Effect (SEE), Single Event Gate Rupture (SEGR), worst-case.**

I. Introduction

THERE continue to be questions about the proper test conditions for single-event gate rupture (SEGR). Specifically, what ions should be used; what ion energy or range produce the lowest failure threshold voltages; and are data provided in the manufacturers' datasheets useful for the specific mission? To answer these questions, one needs to identify what test conditions (bias and ion conditions) cause SEGR; what test conditions yield the lowest failure threshold voltage; what are the failure modes for SEGR; what device performances are affected by SEGR; how destructive is the failure mode (is it catastrophic and does it have micro-breaks [1] or a cumulative effect), and what space environment (ion spectra and energies) will the device encounter allowing the use of adequate SEE safe operating area (SOA) curves to predict the mission life time.

A recent proposal suggests that the ion range selected be based upon the device's voltage rating and the total device thickness [2]. Basically, this guideline suggests that a device's voltage rating and total device thickness are sufficient to determine the ion penetration depth and that the test ion energy be selected such that the ion penetrates at least two thirds into the total silicon thickness (epitaxial-layer thickness plus substrate-layer thickness).

However, this approach contradicts several published papers [3]–[6] demonstrating that the worst-case response is achieved when the Bragg Peak of the selected ion is placed at or near the interface of the epitaxial layer and substrate. Reference [3] shows clearly that ion energy/ion range can affect the measured SEGR threshold voltage. Reference [4] is the first study to isolate and examine the ion energy/ion range of the gate oxide (the capacitor response). This study shows that the measured SEGR failure threshold voltage of the capacitor response remains constant for a given ion species irrespective of its energy, range, or LET value. It also shows that heavier ions decrease the measured SEGR failure threshold voltage and lighter ions increase the measured SEGR failure threshold voltage. Reference [6] describes a new SEGR test protocol and shows that the ion penetration depth is critical to determine the worst-case response. It further shows that placement of the Bragg peak at or near the epi-substrate interface produces the lowest failure thresholds. The majority of this earlier work is based upon MOSFETs that are no longer available in the marketplace.

In this paper, we examine radiation-hardened MOSFETs manufactured by International Rectifier (IR) and we identify the worst-case test conditions for SEGR with a primary focus upon what ion ranges yield the worst-case SEGR response in addition to the gate bias, drain bias, ion species, impact LET value, and other test conditions.

II. Sample Info and Test Setup

Test samples for this study were radiation-hardened power MOSFETs made by International Rectifier (IR). Samples were from different design generations and were mainly n-channel devices. Many of those tested were engineering test samples built for SEE evaluations only (engineering samples do not represent the SEE performance of the final product). Test samples included modified GEN4 500 VN, R5 60 VN, R6 200 VN, R6 250 VN, R6 600 VN, and R7 250 VN, which covered devices using a single epitaxial layer and dual-epitaxial layers (the second epitaxial layer of the dual-epitaxial layers is commonly referred to as a buffer layer). Fig. 15 illustrates a device cross-section showing all material layers.

Samples were assembled and tested in TO-3 packages without a covering lid. The ion beam shutter was opened after each set of V_{GS} and V_{DS} bias conditions were applied. During irradiation, the drain current (I_D) and gate current (I_G) were monitored and recorded. The run was automatically terminated (beam was shuttered) when a preset fluence was achieved (our pre-set fluence was 3×10^5 ions/cm^2) or when the leakage currents reached a maximum pre-set value. For single-event gate rupture (SEGR), I_G was set at 30 μA and for single-event burnout (SEB), I_D was set at 3 mA. Upon completion of the test condition, the biases were removed, and the integrity of

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the gate oxide was verified by applying V_{GS} up to ± 20 V. All tests were performed with ion beams at normal incident angle to the device surface. All irradiated samples were electrically tested and visually inspected to confirm pass/fail and the failure mode (typically, SEB failures produce discoloration and/or burn marks on the die surface; whereas, SEGR failures produce no visible signs of damage on the die surface).

III. SEGR Basics

A. SEGR Failure Definition

On a typical power MOSFET datasheet, gate leakage current specification limits are usually ± 100 nA at full rated gate voltage. However, good devices usually exhibit gate leakage currents of a few nano-amperes at full rated gate voltage. If the leakage current exceeds 100 nA, the device is considered a failure (leaky); although electrically, the device may still be fully functional (i.e., the device is capable of switching from an off-state to an on-state and operating within the other specified parameters).

Current SEE test methodology (e.g., MIL-STD-750E, Test Method 1080) defines SEGR failure as a sudden increase in the gate leakage current during irradiation to heavy ions with the gate and/or drain terminals under bias. The criterion used to define SEGR failure in this paper is if the gate current exceeds 30 μA during ion irradiation to a fluence of 3×10^5 ions/cm^2 (referred to as a test run), then SEGR has occurred. If the gate current exceeds 100 nA during the post SEE electrical test, the device is considered to have failed the SEE test even though the in-situ gate leakage current did not exceed 30 uA under ion irradiation.

There have been several observations of incremental increases in gate leakage current under ion irradiation, which are not considered SEGR since they did not exceed pre-set limits [1], [7]. Scheick *et al.* [1] proposes an interesting concept of micro-breaks where the device remains functional, until the accumulation of micro-breaks lead to catastrophic gate oxide breakdown rendering the device useless. Fig. 1 is an example of an observed step increase in gate leakage current during the test of a 250 VN logic device using krypton beam. The initial krypton energy was 924 MeV, impact LET 57.8 MeV-mg/cm^2, and total range 73.2 μm. The gate leakage current increased from its initial starting value of 20 nA to 1 μA at a fluence of 1.5×10^5 ions/cm^2 with another step increased to 2.5 μA at a fluence of 2.5×10^5 ions/cm^2. The gate leakage current did not exceed the pre-set value of 30 μA to trigger the software flag for SEGR failure during ion irradiation. However, the gate leakage current measured 18 μA during post-SEE electrical test, which exceeded the maximum specification limit of 100 nA causing the device to fail the SEE test under this krypton beam. Other device performance parameters such as breakdown voltage, gate threshold voltage, on-resistance and forward body diode voltage drop remained unchanged. How the krypton beam caused device failure during irradiation raises two questions: (1) is 30 μA appropriate as the SEGR test limit and (2) did the device experience micro-breaks during irradiation which ultimately broke completely during post-SEE electrical test (when ± 20 V was directly applied to the gate) is a research project for future investigation.

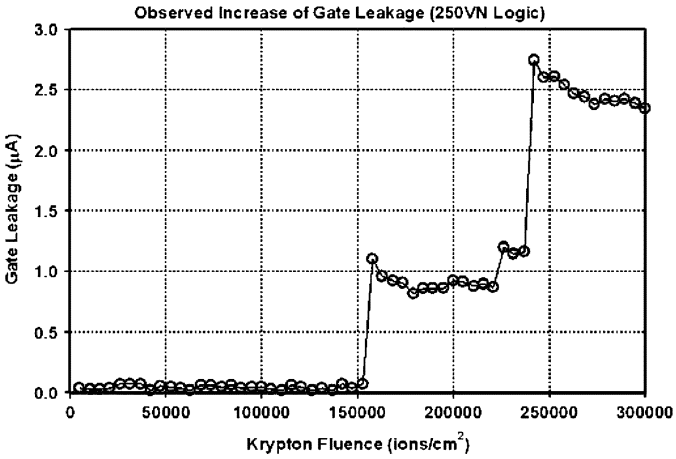

Fig. 1. Observed step increase in gate leakage current of a 250 VN logic device under krypton ion irradiation to a fluence of 3×10^5 ions/cm^2.

B. SEGR Threshold Definition

The SEB threshold voltage is mainly defined by the minimum drain voltage applied at which SEB occurs under heavy ion irradiation [6]. The SEB failure threshold voltage varies slightly from part-to-part or from one ion beam to the next, but remains relatively constant when the minimum LET values and ion ranges are met. Based upon past test data, ion beams with ranges greater than 30 μm are sufficient to trigger SEB. Therefore, ion beams from either Brookhaven National Lab (BNL) Tandem Van de Graaff or Texas A&M Cyclotron are capable of triggering SEB if present.

However, the SEGR failure threshold voltage behaves quite differently from the SEB failure threshold voltage. SEGR failure threshold voltages are more dynamic and can vary dramatically based upon the ion beam and biases.

SEGR failure thresholds cannot be defined by only a minimum drain voltage, or by only a minimum gate voltage or by even a combination of drain and gate voltages. SEGR failure thresholds are influenced by a combination of many conditions and depend upon the drain voltage, gate voltage, ion species, and ion range. All of those conditions must be considered. For example, the minimum drain voltage at which SEGR occurs can change dramatically when the ion species and/or ion range (ion energy) changes. Even for the same ion species, the single event response changes as the ion penetration depth changes. Those factors are described in more detail in the next section.

The fact the SEGR performances are strongly influenced by the ion beams creates tremendous difficulties in comparing SEE test results for the same device but under different ion beam conditions. Sometimes system users raise questions about devices that fail within the $V_{GS} - V_{DS}$ SEE SOA provided in the device's datasheet without realizing that the devices were tested under very different ion beam conditions than those specified in the datasheet. We will touch upon this topic later in the paper.

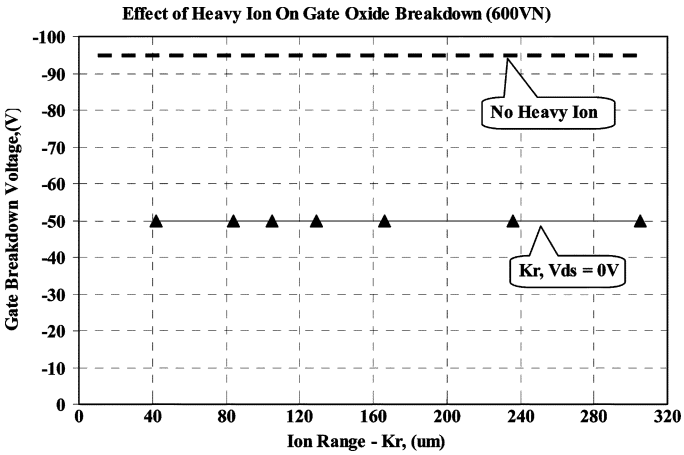

Fig. 2. Comparison of gate oxide breakdown voltages of a 600 V device under two test conditions: (1) with no heavy ion irradiation; (2) under various krypton ion beam irradiations.

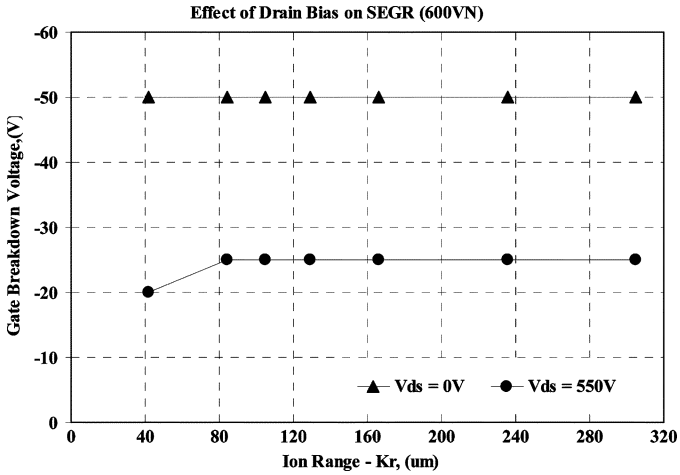

Fig. 3. Impact of drain voltage at 0 V (circles) and 550 V (triangles) upon the SEGR failure threshold voltages (minimum gate voltage) observed on a 600 V power MOSFET with krypton at various total energies.

IV. SEGR Threshold Factors

A. Impact of Heavy Ion on Gate Oxide Breakdown Voltage

Earlier studies [3], [4] on the effects of heavy ions upon the gate oxide breakdown voltage are presented on MOSFETs that are no longer available on the market. To examine the gate oxide breakdown voltage on newer devices, experiments were performed on a 600 VN device. The normal distribution of the gate oxide breakdown voltage of this device was acquired at the wafer level by increasing the gate voltage in 5 V steps and measuring the gate leakage current. Ninety-eight percent of the tested samples exhibited breakdown of the gate oxide at 95 V and/or 100 V.

SEE test samples were subsequently taken from same wafer lot, packaged, and tested under various krypton ion beams. Similar to the wafer test, the gate voltage was incremented in 5 V steps. In Fig. 2, the gate oxide breakdown voltage decreased from its initial value of 95 V (no ion irradiation) to 50 V (during irradiation to krypton ions). This test was performed without any drain bias. It is interesting to note that the gate oxide breakdown voltage did not change as the range, energy, and initial LET value of the krypton ion beam changed. The total krypton ion energy varied from 342 MeV to 1958 MeV and the range varied from 42 μm to 305 μm. Different ion ranges are achieved using degraders. However, this measured response may change when a heavier test ion is used. Heavier ions such as xenon and gold may have higher impact on the gate oxide breakdown voltage than krypton. Therefore, the gate oxide breakdown voltage should decrease during irradiation with heavier ions yielding lower SEGR thresholds. The measured SEGR response may vary from one design generation to the next (e.g., older generations of radhard power MOSFETs may easily fail under krypton irradiation).

B. Impact of Drain Bias Upon SEGR

The impact of drain voltage upon SEGR is more complicated than the impact of gate voltage. There are some device types that fail for SEGR with only a drain voltage applied. It is not intuitive how the drain voltage affects the gate oxide breakdown voltage. If we examine the structures of those devices that exhibit SEGR with only a drain voltage applied, most are commercial power MOSFETs and earlier generations of radiation-hardened power MOSFETs. Those types of devices typically have a wider neck width and they would pass a normal rated breakdown voltage test (a test without ion irradiation) but would fail (SEGR failure) with a drain voltage at or below the rated breakdown voltage under heavy ion irradiation.

The body-to-body spacing (commonly referred to the JFET neck width) has been shown to affect how much drain voltage is coupled to the oxide interface [7]. The interaction of the drain voltage to SEGR is commonly referenced in the literature as the substrate or epitaxial layer response [8].

Fig. 3 is a comparison of the measured SEGR failure threshold voltages of a 600 V N-channel power MOSFET at two different drain biases, a drain voltage of zero volts ($V_{DS} = 0$ V) and 550 volts ($V_{DS} = 550$ V), under krypton irradiation. The minimum gate voltage to induce SEGR decreased from 50 volts at V_{DS} of 0 V to 25 volts at V_{DS} of 550 V. Clearly, the drain voltage plays a significant role in defining the SEGR failure threshold voltages. Numerical simulations may help to understand how the drain bias affects the SEGR thresholds by analyzing the electrical field across the oxide and the potential changes within the silicon.

C. Impact of Gate Voltage Upon SEGR

The SEGR failure threshold response using only gate bias and no drain bias is commonly referred to as the oxide response in the literature [3]. The oxide response represents the interaction of the ion with the dielectric (in this case the gate oxide) inducing a temporary lowering of the dielectric breakdown field (commonly referred to as the critical breakdown field).

The impact of gate voltage upon SEGR is relatively straight forward and easy to understand. If a gate voltage is applied to the device, that gate voltage is transferred directly across the gate oxide (i.e., the gate oxide electric field is basically equal to the gate voltage divided by the gate oxide thickness). If the drain voltage is kept at 0 V and the gate bias is increased, then

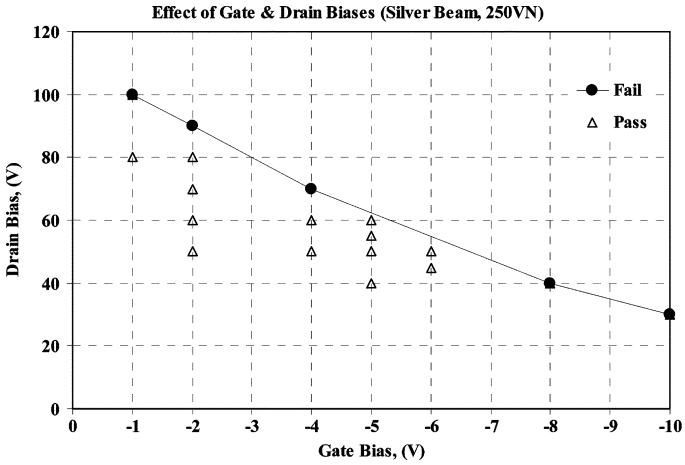

Fig. 4. Impact of drain voltage upon SEGR failure threshold voltages observed on a 250 V power MOSFET using 1217-MeV silver ion beam.

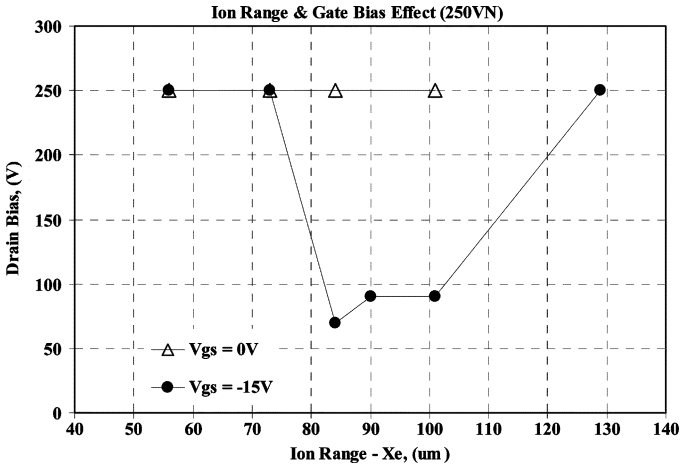

Fig. 5. Impact of drain voltage upon SEGR failure threshold voltages observed on a 250 V power MOSFET using xenon ion beam.

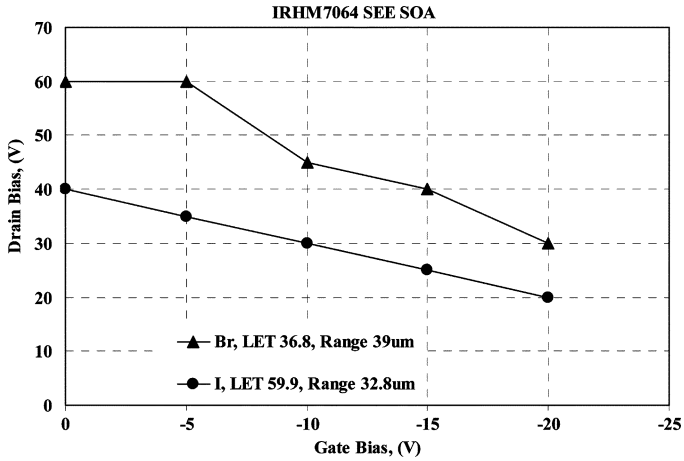

Fig. 6. SEE SOA curves of IR's IRHM7064, for older generation radhard power MOSFET, the SEGR can occur even with light ion such as bromine and short ion range such as 32.8 um with Iodine. Gold (atomic weight 197) is heavier than iodine (atomic weight 127), iodine is heavier than bromine (atomic weight 80).

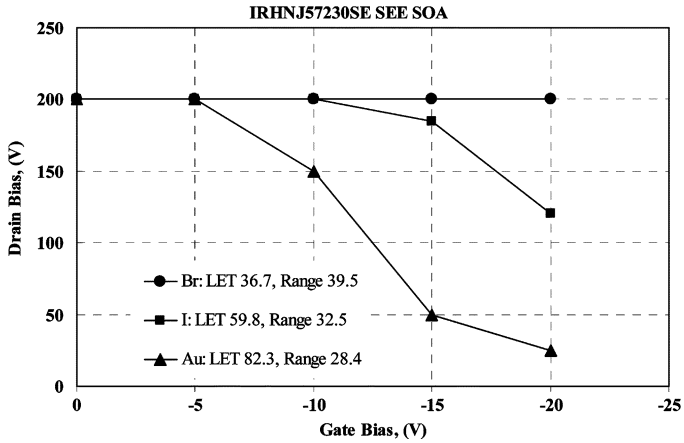

Fig. 7. SEE SOA curves of IR's IRHNA57230SE, the SEGR can occur even with short ion range beams at negative gate bias. Heavier ions would yield worse SEGR performances. Iodine (atomic weight 127) is heavier than bromine (atomic weight 80).

the SEGR failure threshold voltages are determined only by the gate voltage and ion species (see Fig. 2 as an example of gate oxide response).

Fig. 4 shows the measured SEGR failure threshold voltages of a 250 V logic-level MOSFET irradiated with silver (Ag) ions. The SEGR failure threshold voltages were determined dynamically by both drain and gate voltages. There was a clear interaction between the drain and gate voltages that define the SEGR failure threshold voltages. In this case, the drain voltage decreased almost linearly (at a ratio of $\sim 9:1$) with increasing gate voltage. Clearly, the gate bias was more influential on the SEGR thresholds than the drain bias.

Fig. 5 reproduces data from an earlier publication [8]. For this 250 VN device, no SEGR failures were observed when irradiated with xenon beam with V_{GS} of 0 V; but, with V_{GS} of -15 V, SEGRs were recorded and worst-case SEGR ion ranges were identified. This data supports our observation that the gate bias has a strong impact on the measured SEGR thresholds. With that said, it should be noted that SEGR using negative gate biases should not pose too much concern for system users because negative gate bias is not a typical bias in many applications.

D. Impact of Ion Species Upon SEGR

There is consistent agreement among published sources [3]–[5] that heavier ion species lower the measured SEGR failure threshold voltages. Figs. 6 and 7 reproduce two sets of SEE SOA curves for the IRHC7064 and IRHC57230SE [9], [10] and were irradiated at Brookhaven National Lab (BNL) using bromine, iodine and gold ions. The ion ranges of these three ions were relatively short when compared to the ion ranges available at the Texas A&M Cyclotron facility. However, even with the use of these lower ion range beams, heavier ions lower the SEGR failure threshold voltages (threshold voltages becomes lower in terms of the highest passing drain voltages at the same gate voltage).

Fig. 8 is a plot of an ion range study for engineered Gen4 500 VN device. This device performed well under krypton (atomic number 36, atomic weight 84) irradiation regardless of the ion range, but under silver (atomic number 47, atomic weight 108) and xenon (atomic number 54, atomic weight 131) irradiation, the SEGR threshold voltage decreased significantly. However,

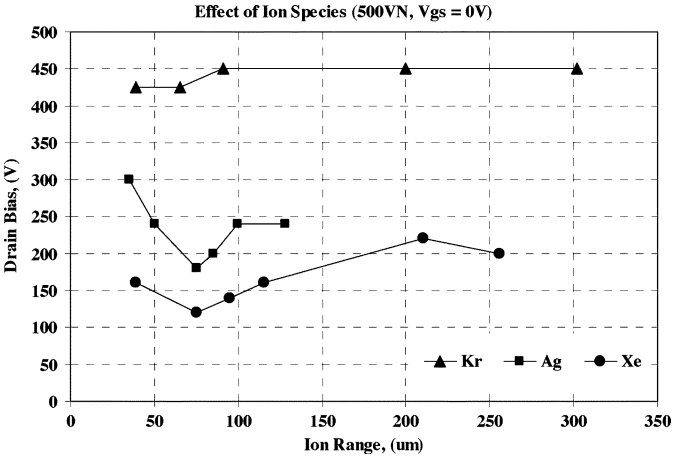

Fig. 8. Ion range study on engineered IR's Gen4 500 VN device. Shows device performed well under krypton, but showed much lower SEGR thresholds when tested with silver and xenon.

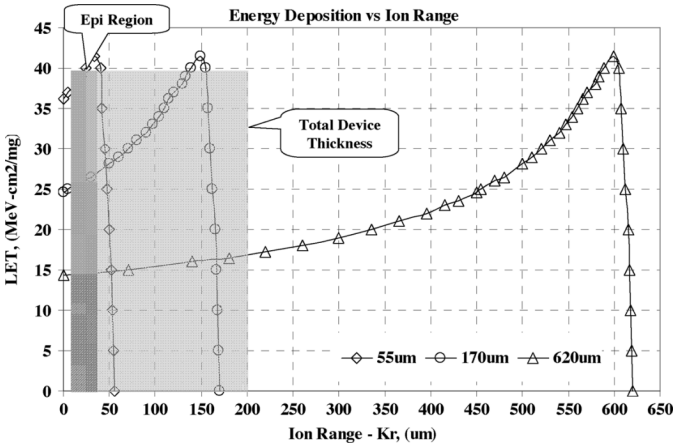

Fig. 9. Comparison of energy deposition in the sensitive region of krypton ion beams with three different ion ranges: 55 μm, 170 μm and 620 μm. The beam with the longest ion range (highest total energy) deposits the least energy in the sensitive region.

the lower fluence of ions heavier than iron (atomic number 26, atomic weight 55.8) in the natural space environment makes the benefit of testing with heavier ions questionable.

E. Impact of Ion Energy/Range Upon SEGR

Titus *et al.* [5] were the first to report that longer ion ranges such as those provided by the Texas A&M cyclotron facility produce worst-case SEE performances for power MOSFETs rated above 150 V when compared to less penetrating ions such as those provided by the tandem Van de Graff at BNL. Consequently, users interested in SEE issues have been requesting SEE testing be performed with longer ion ranges.

Some researchers are proposing to use ion beams with the longest ion range available for every ion specie at Texas A&M. Their reasoning is that actual ions encountered in outer space have significantly higher energies than any cyclotron on earth could produce. Thus, simulated ground tests are not reproducing the real mission environment.

One of current proposals [1] states that heavy ion irradiation should be performed at facilities that provide ions of sufficient range to penetrate the device from the die surface to a depth of $2/3$ the bulk silicon region (substrate region). End users are starting to request this type of data from the vendor. However, published SEGR failure observations [6], [8], [13] do not support using ions that penetrate so deeply into the substrate as producing the worst case SEGR response. To further support this assertion, evaluations of the measured SEGR failure threshold voltages (V_{DS} and V_{GS}) as a function of different ion ranges have been performed.

Fig. 9 is a comparison of energy loss (dE/dx) in the sensitive region (epitaxial layer) in a 200 VN single epitaxial device with krypton ion beams of three different beam energies: 450 MeV, 1270 MeV and 3175 MeV (with respective ion ranges of 55 μm, 170 μm and 620 μm).

In this example (Fig. 9), the longest ion range (curve with triangles) corresponds to the ion with the highest energy (available at Texas A&M). Clearly, the ion beam with the longest ion range and highest total energy deposits the least amount of energy in the sensitive region because the LET values are actually lower than the LET values of the other two short range beams (curves in diamonds and circles). The average LET value in the sensitive region is less than 15 MeV-cm^2/mg for krypton with the 620-μm range; while the average LET value in the sensitive region is 26 MeV-cm ^{2}/mg for krypton with the 170- μm range; and 39 MeV-cm ^{2}/mg for krypton with the 55-μm range. It is well known that the SEGR threshold is inversely related to the beam LET values in the sensitive region, which translate into energy deposition in the sensitive region. Thus, for those three krypton beams analyzed here, the beam with the 55- μm range should produce the worst SEGR performance for this 200 VN device.

When the total energy is increased even further such as in real space environment, the LET values in the sensitive region become even lower, which translates to even lower energy deposition in the sensitive region. In other words, for the same ion, the beams with the highest energy results in lowest energy deposition in the sensitive region of the device, and thus have the least impact on the device performance. In many situations, the ions with the highest energies just pass through the device causing little or no damage to the device.

Fig. 10 is a comparison of the measured SEE failure threshold voltages of a 200 VN dual-epi device using a xenon ion beam at ion ranges of 66 μm and 205 μm. The total die thickness is about 250 μm; therefore, the xenon ion beam with a 205-μm range penetrates the entire thickness of the epitaxial layer and 2/3 the thickness of the highly doped substrate region. The measured test data for the 205- μm xenon ion beam does not yield worse-case SEGR failure thresholds when compared to measured test data for the 66- μm xenon ion beam.

A similar SEE evaluation was performed on IR's modified GEN4 radiation-hardened product to examine the response of a single epi device. Figs. 11 and 12 show the measured passing and failing SEGR points in terms of drain voltage as a function of ion range for silver and xenon ions when 500 VN single epi

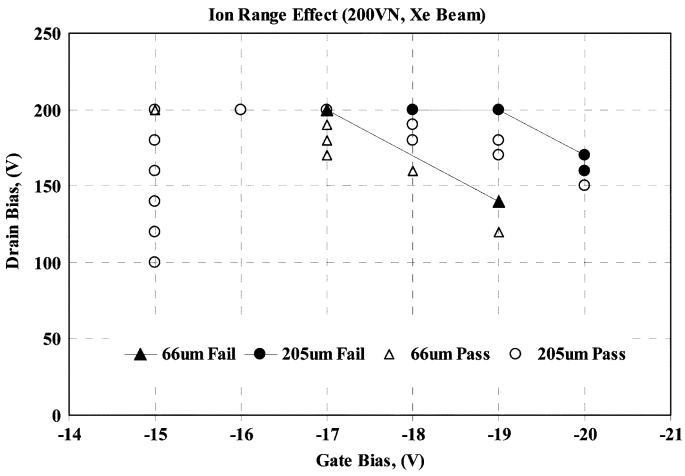

Fig. 10. Comparison of measured SEGR failure threshold voltages of a 200 V N-channel MOSFET irradiated with Xenon at Texas A&M showing that ions which completely penetrate the device may not yield the worse-case response.

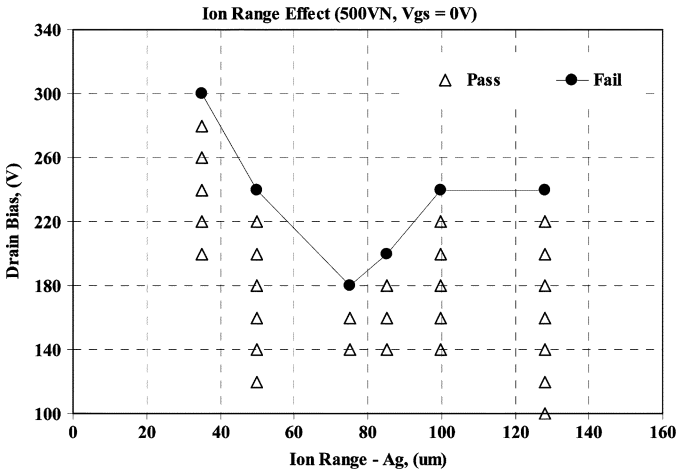

Fig. 11. Passing and SEGR failing points for a 500 V N channel device under silver ion irradiation with no bias on the gate ($\mathrm{V_{GS}} = 0$ V).

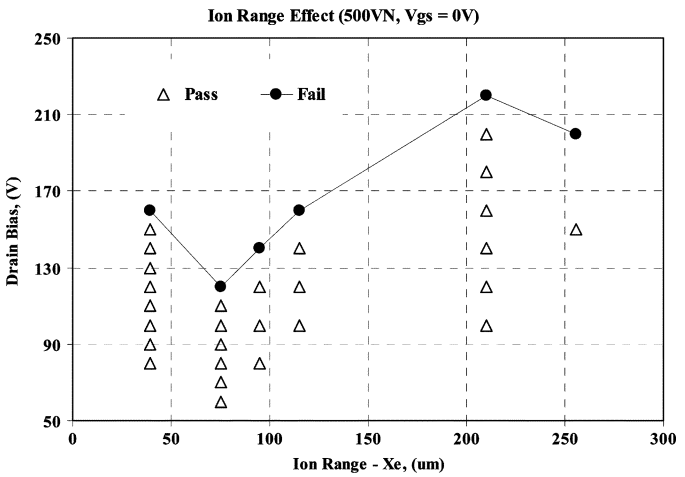

Fig. 12. Passing and SEGR failing points for a 500 V N channel device under xenon ion irradiation with no bias on the gate ($\mathrm{V_{GS}} = 0$ V).

devices were irradiated. The gate voltage was zero volts ($\mathrm{V_{GS}} = 0$ V).

The measured responses are similar to the measured response of the R6 250 VN dual epi devices. The SEGR failure threshold initially decreases with increasing ion ranges, reached a minimum threshold, and as the ion range continued to increase, the threshold increased from this minimum. The worst-case SEGR response was not produced by ions with the shortest range nor was it produced by ions with the longest range. When the ion range was relatively shallow (e.g., 30 to 40 μm), the measured SEGR failure thresholds were relatively high, but when the ion range increased, the SEGR failure thresholds decreased and reached their lowest thresholds when the ion range was at 75 μm for both silver and xenon beams. As the ion range continued to increase, the measured SEGR failure thresholds increased from 180 V to 240 V under silver beam, and increased from 120 V to 220 V under xenon beam. Clearly, those data demonstrate that an ion that penetrates too deep into the substrate produces higher SEGR failure threshold voltages and not the worst-case SEGR response (the lowest SEGR failure threshold voltage).

F. Impact of LET Value and Bragg Peak Position Upon SEGR

Similar to ion species where higher Z ions produce lower SEGR failure threshold voltages, in general, this trend is also true for LET value (higher LET values produce lower SEGR failure threshold voltages). SEE testing ultimately measures a device's capability of handling localized charge deposition in the most sensitive region within the device while the gate and drain are biased at their desired operating conditions. Usually, higher LET values translate into higher energy deposition and charge generation inside the device. However, higher surface LET values (impact LET value) do not necessarily produce the worst-case SEGR response.

Figs. 13 and 14 show how the LET value (secondary Axis) changes as the ion penetrates the silicon for three different initial surface LET values (impact LET) until it comes to rest (ion range) and how the SEGR failure threshold voltage (primary y-axis) changes for each of those three ion beams with different impact LET values and ranges. The test results demonstrate that ion beam with highest surface LET (or impact LET) or ion beam with longest range does not necessarily produce the worst-case SEGR failure threshold.

Fig. 13 depicts the three xenon ion beams used in the 500 VN single epi device (no buffer layer) test. Beam #2 (range of 75 μm) yields the lowest SEGR threshold voltage with a 120 V drain bias (indicated by circled dot); whereas, Beam #1 (range of 39.1 μm) yields a 160 V drain bias (indicated by circled triangle) and Beam #3 (range of 160 μm) yields a 200 V drain bias (indicated by circled diamond). When we compare the impact LET-Ion Range curve with the device layer construction, the position of the Bragg Peak for Beam #2 occurs at or near the epi/substrate interface.

Fig. 14 depicts the three Xenon ion beams used in the 250 VN dual-epi device (epitaxial layer and buffer layer) test. Beam #2 (range of 84 μm) yielded the lowest SEGR threshold voltage with a 70 V drain bias (indicated by circled dot); whereas, Beam #1 (range of 56 μm) yielded a 250 V drain bias (indicated by circled triangle) and Beam #3 (range of 130 μm) yielded a 250 V drain bias (indicated by circled diamond). When we compare the impact LET-Ion Range curve to the device layer construction,

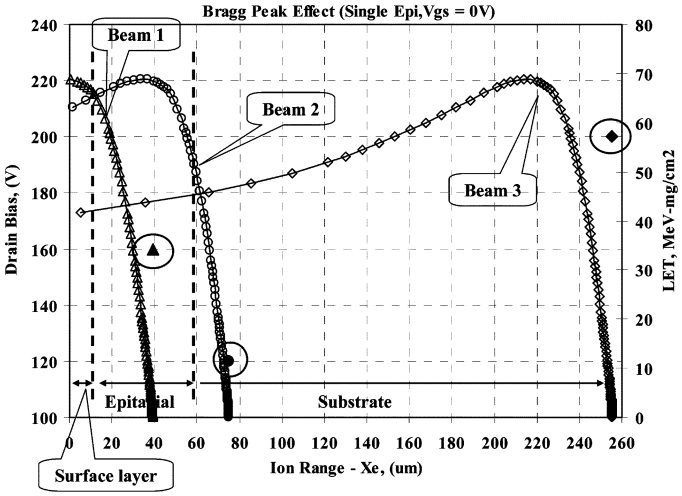

Fig. 13. Evaluation of initial LET values/ranges versus measured SEGR failure threshold voltages under different xenon beams. The xenon ion beam for worst-case SEGR does not have highest surface LET nor longest range but with Bragg Peak near epi/substrate interface.

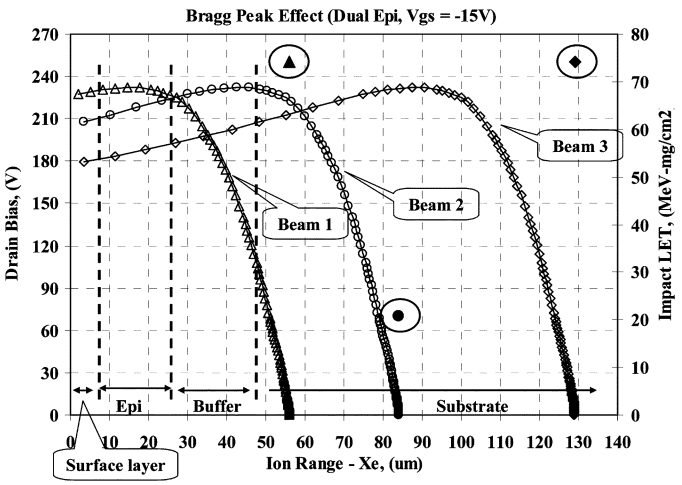

Fig. 14. Evaluation of initial LET values versus measured SEGR failure threshold voltages for a 500 V N-channel device under different xenon beams. The xenon ion beam for worst-case SEGR does not have highest surface LET nor longest range but with Bragg Peak positioned at the buffer/substrate interface.

the position of the Bragg Peak for Beam #2 occurs at or near the buffer/substrate interface.

An earlier publication [8] already demonstrated that the worst-case ion energy condition for SEGR of IR's R6 250 V N-channel device occurred when the Bragg Peak of the xenon ion was positioned at or near the buffer layer/substrate interface.

V. Discussions

A. The Role of Substrate

When the construction details of a power DMOSFET are examined, one usually finds a passivation layer at the die surface, then a front metal for the source and gate contacts, then an interlayer dielectric for gate-to-source isolation, then a polysilicon layer for the gate, then a gate oxide layer, and then beyond

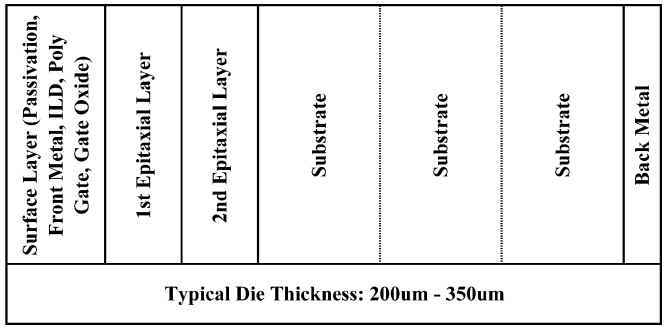

Fig. 15. An illustration of a typical material stacking of a power DMOSFET. It consists of surface layer, epitaxial layer, substrate and back metal. Layers are not to scale.

this layer, there is bulk silicon material consisting of (1) epitaxial layer—high resistivity, low doped concentration silicon where the device is built; and (2) substrate—highly doped, extremely low resistivity silicon to provide support. At the substrate bottom is a thin layer of back metal for drain contact. For older generation and almost all commercial power MOSFETs, one epitaxial silicon material is used. While for newer generation radiation hardened power MOSFETs, two epitaxial silicon layers are adopted to improve device SEB performance [6]. Fig. 15 is an illustration showing possible material stacking of a power DMOSFET with dual epitaxial layers.

The surface layers are commonly referred to as dead layers, composed mostly of non-silicon material except for the poly silicon gate. The total thickness of surface layers typically varies from 7 μm to 12 μm and depends heavily upon the thickness of the passivation and metal layers. The substrate is always a highly doped, extremely low resistivity, silicon layer on which the epitaxial silicon layers are grown and where the power MOSFET is built.

For MOSFETs, the highly doped substrate serves mainly as a supporting layer. The substrate thickness has little effect on device performance except for very low Rdson devices where tenths of a milliohm adds to the already low on resistance. In other words, from a device performance point of view, the thickness of the highly doped substrate does not play a role in the device response. The only reason that older generation MOSFETs have total die thicknesses between 300 μm and 350 μm is the limitation of grinding tools available at that time. There were no backside wafer grinding tools that allowed the wafer to be thinned beyond this thickness without high mechanical yield loss. Today, most final die thicknesses for power MOSFETs are between 200 μm and 250 μm regardless of the device voltage rating, and for some low voltage commercial parts, the total die thickness is less than 150 μm. Unless there is a special requirement to reduce the extra 0.2 mohm substrate resistance from total on-resistance of 1–2 mohms, manufacturers are not likely to thin the die thickness any further due to process complexities, but this does not imply that the remaining substrate thickness is needed for device performance.

Since the substrate is a highly doped, very low resistivity layer, carrier lifetime in a highly doped substrate is very short. Carries generated from an ion strike in the substrate recombine too quickly to drift to the surface. That is most likely why

TABLE I
ESTIMATED WORST-CASE SEGR ION RANGES FOR 30–1000 VN DEVICES (BOTH SINGLE AND DUAL EPITAXIAL MATERIALS) IF TO BE TESTED WITH KRYPTON, OR XENON OR GOLD ION BEAMS

Appr. Epi Thickness (um)	Device Rating (V)	Estimated Worst-Case Ion Range (Single Epi) (um)			Estimated Worst-Case Ion Range (Dual Epi) (um)		
		Kr	Xe	Au	Kr	Xe	Au
5	30	40	46	67	45	51	72
7	60	42	48	69	49	55	76
10	100	45	51	72	55	61	82
20	200	55	61	82	75	81	102
25	250	60	66	87	85	91	112
50	500	85	91	112	135	141	162
100	1000	135	141	162	?	?	?

energy deposition and charge generation in the substrate does not cause notable changes in the SEGR threshold voltages when compared to changes from the epi region (a higher resistivity/lower doping) or epi/substrate interface. As explained earlier [6], under normal avalanche breakdown, the highest electric field is at the p-n junction. However, the highest electric field shifts from the p-n junction to epi/substrate interface under extremely high transient current conditions, which occur in a power MOSFET under single event testing. It is possible in devices employing a buffer layer for the worst-case ion range to vary from the epi/buffer interface to the buffer/substrate interface. The mechanism of why the worst-case ion range for SEGR is to position the Bragg Peak at/near the epi/substrate interface will be examined in future work using numerical device simulations.

B. Estimated Worst-Case SEGR Ion Ranges

Many users request information regarding the sensitive region or epitaxial thickness for their respective devices to be used in worst-case calculations or failure rate predictions. Table I provides approximate epi thicknesses for device ratings from 30 VN to 1000 VN for single epitaxial and dual epitaxial layer devices. The epi thicknesses are for reference only and do not represent the exact thickness used in a real device. The epi thickness may vary depending upon the material resistivity, manufacturer, design generation and whether or not the device is commercial or radiation hardened. The overall thicknesses may vary slightly or significantly, but for the purposes mentioned earlier (failure rate predictions), Table I is useful.

Estimated worst-case ion ranges for SEGR are calculated by adding an equivalent surface layer of 10- μm silicon depth, plus the epitaxial layer thickness, and the Bragg Peak position. For example, if we examine a 200 VN device, the approximate epi thickness is 20 μm, and the Bragg Peak position before xenon ions stop is 31 μm. Therefore, the worst-case ion range (Xe) for this 200 VN device is 61 μm: (10 μm +20 μm +31 μm = 61 μm). For devices with a buffer layer, the buffer layer thickness is assumed to be the same thickness as the epitaxial layer. Therefore, the worst-case ion range (Xe) for this 200 VN dual epi device is 81 μm: (10 μm +20 μm x 2 + 31 μm = 81 μm). Although in reality, the buffer layer thickness can be thinner or thicker depending upon the resistivity used.

C. Probability of Worst-Case SEGR Ion Beams

As clearly shown earlier (see Fig. 9), heavy ions with extremely high energies, extremely long ion ranges in silicon, are likely to deposit the least amount of energy in the sensitive region and pass through the device without significant damage. The ion beams, which are more likely to cause worst-case SEGR, are ion beams with lower total energy and limited penetration depth in silicon. Based upon estimated worst-case SEGR ion ranges for krypton, xenon and gold (see Table I), the longest ion range needed to perform an adequate SEGR evaluation would be no more than 160 μm. At this time, there is no justification to irradiate power MOSFETs with ion beams deeper than the estimated worst-case ion ranges.

One question remains: if most ions in space are extremely high energy, what is the probability of encountering an ion with required energy/range to trigger worst-case SEGR? Unfortunately, we are not able to address this question in this paper. However, there is a small probability that one of those worst-case ions may strike the MOSFET, and before it does, that ion will traverse many different layers, which lower the ion energy/range before it reaches the sensitive region of the MOSFET. There are also probabilities that when extremely high energy ions strike certain materials causing nuclear reactions that may generate secondary ions with the required energy/range.

VI. SUMMARY

In this paper, we provide some key graphs to demonstrate that worst-case SEGR conditions do exist for radiation-hardened power MOSFETs. Those graphs demonstrate that the worst-case test conditions for SEGR depends upon four variables: gate and drain voltages, ion specie, and ion range (or energy). Those four variables are key factors in determining the lowest SEGR failure threshold voltages—SEE SOA curves. We also show that using an ion beam (ion specie with a specific energy) with the highest impact LET (surface LET) does not yield the lowest SEGR failure threshold voltage and that using an ion beam with the highest ion range (ion penetration depth) does not always yield the lowest SEGR failure threshold voltage either.

Instead, we show that the worst-case SEGR response for radiation hardened power MOSFETs occur when the Bragg peak of the ion beam is positioned at or near the epitaxial/substrate interface. Our test results contradict recent proposals to use ion beams with the highest ion range/energy available at heavy ion test facilities like Texas A&M. Finally, our observations provide useful insights in understanding SEGR mechanism.

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