75 W power supply using CoolSET™ SiP ICE188LM

EVAL_75W1_ZVS_188LM

About this document

Scope and purpose

This engineering report describes the EVAL_75W1_ZVS_188LM Evaluation Board for a flyback converter with an isolated 12 V, 6.25 A output using the latest Infineon CoolSET™ ICE188LM System in Package (SiP) zero-voltage switching (ZVS) flyback integrated solution with CoolSiC™ MOSFET. This 75 W evaluation board serves the purpose of understanding the technical features and capability of the CoolSET™ ICE188LM. For detailed features and power delivery capability, see the device datasheet [1].

Highlights of this power supply:

- Overall high efficiency to meet energy efficiency requirement
- Simplified circuitry with high-level integration of power control and protection features
- Auto-restart protection scheme to minimize interruption and enhance the user experience
- Zero voltage switching (ZVS) technology to boost efficiency
- CoolSiC™ MOSFET to enable higher output power

Intended audience

The intended audiences for this document are design engineers, technicians, and developers of electronic systems.

CoolSET™

Infineon's CoolSET™ AC-DC integrated power stages in fixed frequency and quasi-resonant switching schemes offer increased robustness and outstanding performance. This family offers superior energy efficiency, comprehensive protective features, and reduced system costs and is ideally suited for auxiliary power supply applications in a wide variety of potential applications such as:

- SMPS
- Home appliances
- Server
- Telecom

Table of contents

1 Introduction

This engineering report describes the EVAL_75W1_ZVS_188LM Evaluation Board designed in a zero-voltage switching (ZVS) quasi-resonant (QR) flyback converter using CoolSET™ ICE188LM System in Package (SiP) from Infineon's first fully integrated controller. The evaluation board provides 75 W output at 12 V and 6.25 A, with an input range of 90 VAC to 264 VAC. The evaluation board can achieve 94.2% peak efficiency.

The CoolSET™ ICE188LM is ideally targeted for auxiliary power supplies for SMPS, home appliances, servers, and telecom applications. The SiP integration includes an 800 V CoolSiC™ MOSFET, primary and a secondary controller, and isolated communication. An advanced PWM switching pattern forces a zero-voltage switching (ZVS) quasi-resonant (QR) operation, reducing the turn-on switching losses and optimizing the EMI signature. A comprehensive set of protection features supports ease of design-in.

Table 1 lists the general system requirements for a power supply and the corresponding Infineon solution using ICE188

Table 1 General system requirement and proposed design solution

	General system requirement	Proposed design solution – ICE188LM
1	High efficiency to meet energy efficiency requirements	Primary zero-voltage switching and secondary optimal synchronous rectifier (SR) control
2	Simplified circuitry with high-level integration	Primary 800 V CoolSiC™ MOSFET, primary and secondary controller, and communication integrated in a DSO-27 package
3	Minimize interruption to enhance user experience	All protections are defined to enter auto-restart mode

2 EVAL_75W1_ZVS_188LM Evaluation Board

This document contains the list of features, power supply specifications, schematics, bill of materials (BOM), and performance data. Typical operating characteristics, such as performance curve and scope waveforms are shown at the end of the report.

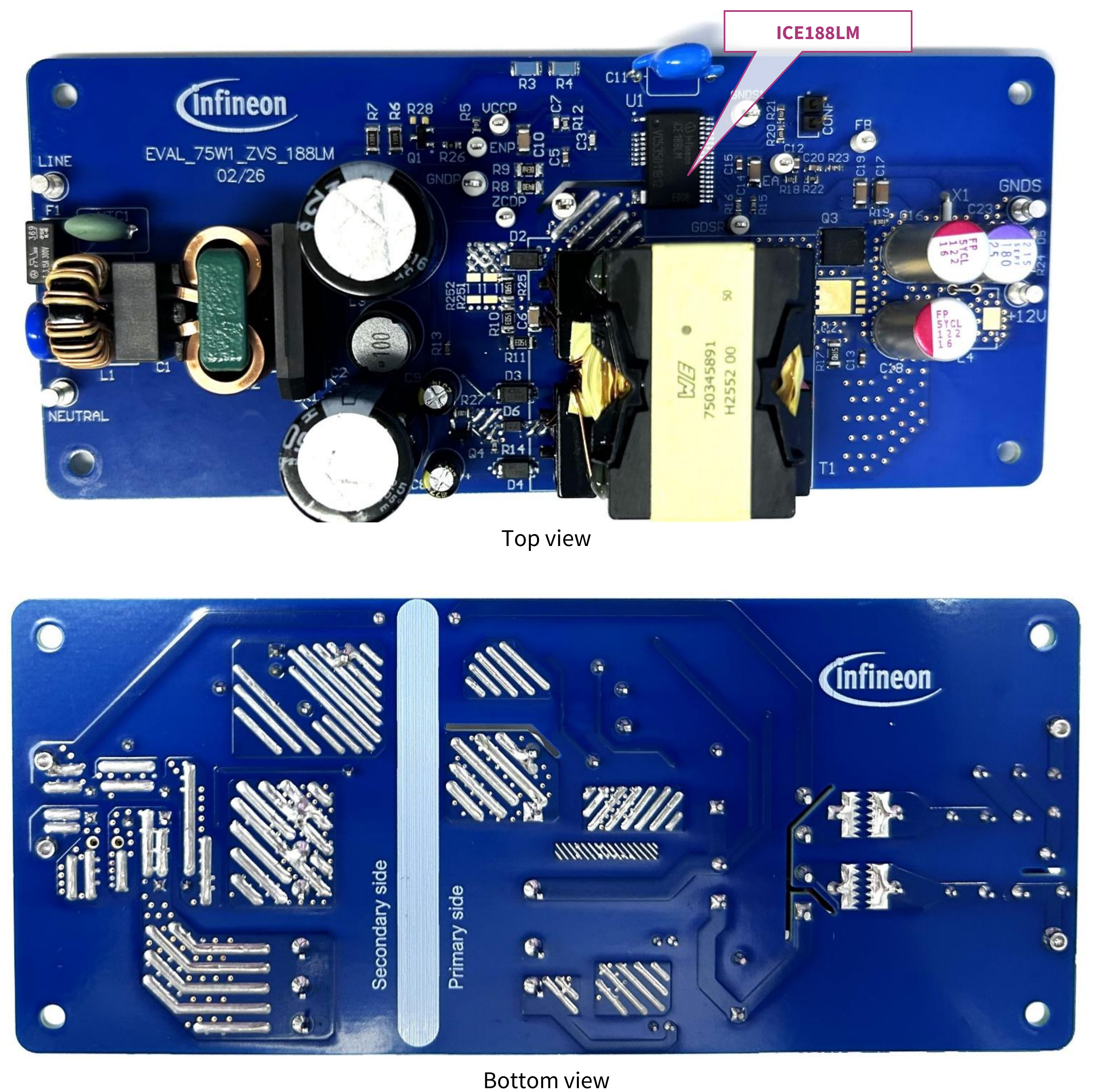


Figure 1 **EVAL_75W1_ZVS_188LM Evaluation Board**

3 Specifications of evaluation board

Table 2 Specifications of EVAL_75W1_ZVS_188LM

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions/notes
Input						
Voltage	V_{IN}	90	–	264	VAC	2-wire (no P.E.)
Frequency	f_{LINE}	47	50/60	64	Hz	–
Output						
Voltage	V_{OUT}	12			V	–
Current	I_{OUT}	6.25			A	–
Output power	P_{OUT}	75			W	–
Overcurrent protection	–	< 150% of rated current			A	–
Ripple and noise voltage	V_{pk-pk}	280			mV	-
Environmental						
Conducted EMI	–	6			dB	EN55022
Surge immunity – Differential mode (DM)	–	±2			kV	EN 61000-4-2
Surge immunity – Common mode (CM)	–	±4			kV	
ESD – Contact discharge	–	±8			kV	EN 61000-4-5
ESD – Air discharge	–	±15			kV	
Ambient temperature	T_{amb}	–	25	–	°C	Free convection, sea level
Size	–	140 x 60			mm	L × W

Note: *The table above represents the minimum acceptable performance of the design. Actual measurement results are listed in the Test results section.*

4 Schematic

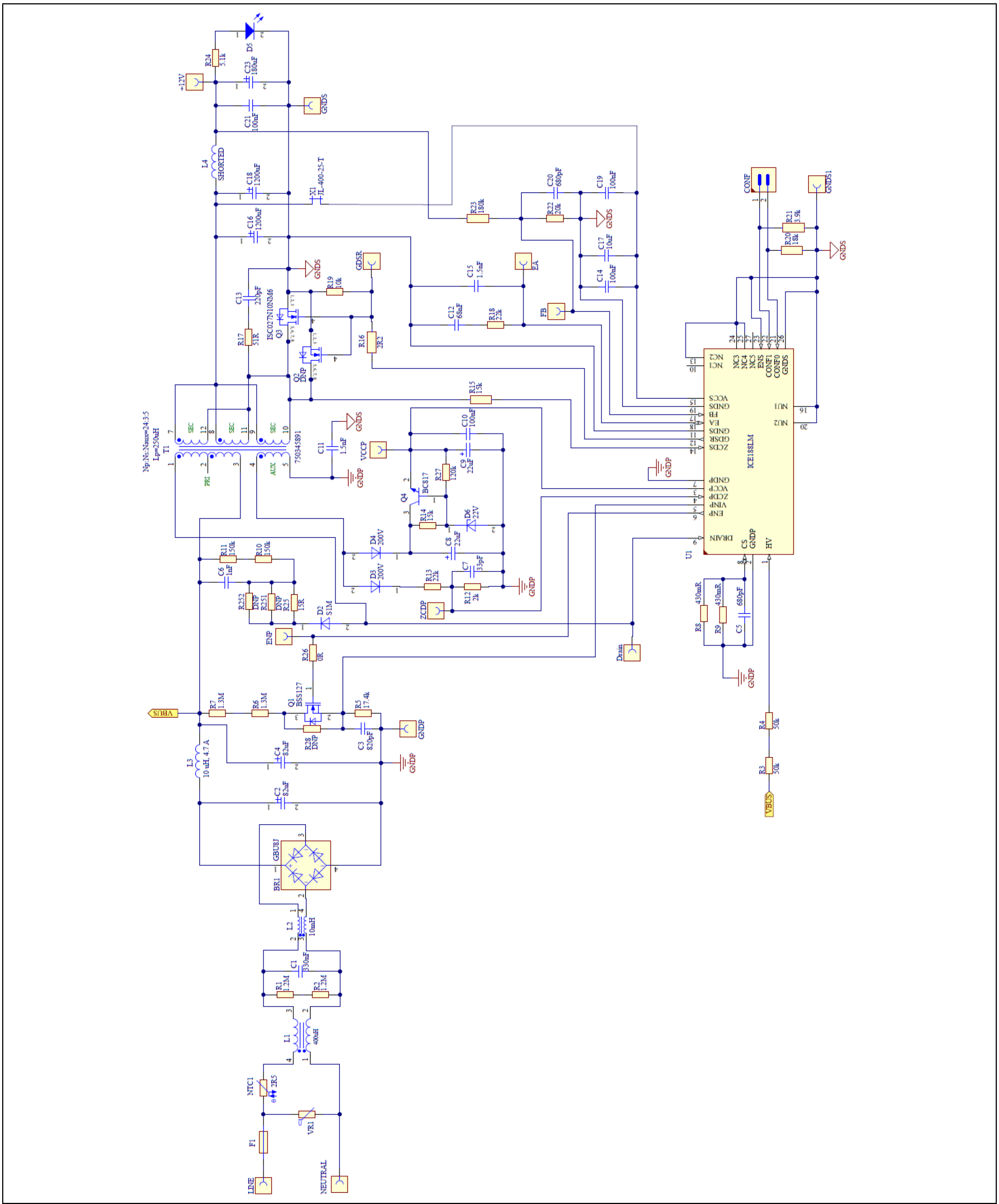


Figure 2 **Schematic of EVAL_75W1_ZVS_188LM**

5 Circuit description

This section briefly describes the design circuit by different functional blocks. For details of the design procedure and component selection for the flyback circuitry, see the IC datasheet [1] and design guide [2].

5.1 EMI filtering and line rectification

The input of the power supply is taken from the AC power grid, which is in the 90 VAC ~ 264 VAC range. The fuse (F1) is right at the entrance to protect the system in case of excess current entering the system circuit due to a fault. Following is the varistor (VR1), which is connected across L and N to absorb the line surge transient.

Common mode choke L1, L2, and the X-capacitor C1 form a basic filter to reduce the EMI noise. The bridge rectifier (BR1) rectifies the AC input into DC voltage, filtered by the π filter (C2, C4, and L3). R1 and R2 resistors discharge C1 when the power supply is disconnected from the AC mains. NTC1 is used to suppress the inrush current when the AC is connected to the board.

5.2 CoolSET™ SiP power stage

The flyback converter power stage consists of a power transformer, primary power MOSFET, secondary synchronous rectifier (SR) MOSFET, secondary output capacitors, etc.

Primary and secondary sides, power management are separated for isolated power supply domains (VCCP, GNDP and VCCS, GNDS). ICE188LM provides reinforced isolation and safe communication between primary and secondary sides.

5.2.1 CoolSET™ SiP primary side

The CoolSET™ ICE188LM SiP integrates a 950 V startup cell at the primary side. The IC self-starts through the startup resistors (R3 and R4) in series with this startup cell to charge the VCCP pin capacitors (C9, C10) when DC supply is applied. These startup resistors, together with ZCDP pin external configuration resistor R_{ZCDPL} (R12), determine the brown-in and brown-out protection, as shown in Table 3.

Table 3 Primary-side configuration options

Option	$R_{ZCDPL(min)}$; $R_{ZCDPL(max)}$	Brown-in current threshold I_{HV_BI}	Brown-out current threshold I_{HV_BO}	Internal shunt resistor $R_{HVshunt}$
1	[1.00 kΩ; 1.05 kΩ]	2.00 mA	1.40 mA	0.5 kΩ
2	[1.87 kΩ; 2.70 kΩ]	1.00 mA	0.70 mA	1.0 kΩ
3	[4.30 kΩ; 5.00 kΩ]	0.67 mA	0.47 mA	1.5 kΩ
4	[9.20 kΩ; 9.50 kΩ]	0.50 mA	0.35 mA	2.0 kΩ

Option 2 is selected with R_{ZCDPL} (R12) = 2 kΩ, the brown-in voltage can be estimated as:

$$V_{BI} = (R_{HV} + R_{HVshunt}) \times I_{HV\_BI} = (100\ \text{k}\Omega + 1\ \text{k}\Omega) \times 1\ mA = 101\ V$$

Equation 1

And the brown-out voltage can be estimated as:

$$V_{BO} = (R_{HV} + R_{HVshunt}) \times I_{HV\_BO} = (100\ \text{k}\Omega + 1\ \text{k}\Omega) \times 0.7\ mA = 70.7\ V$$

Equation 2

Moreover, R12 and R13 resistors offer zero-crossing detection during the soft-start period and primary-sensed output overvoltage protection.

$$V_{OUT\_OVP} = \left(\frac{(R_{ZCDPH}+R_{ZCDPL}) \times V_{ZCDP\_OVP\_min}}{R_{ZCDPL}} + V_{Daux}\right) \times \frac{N_{SEC}}{N_{AUX}} - V_{Dsec}$$
$$= \left(\frac{(22\ k\Omega + 2\ k\Omega) \times 2.05\ V}{2\ k\Omega} + 0.3\ V\right) \times \frac{3}{5} - 0.1\ V \approx 14.84\ V$$

Equation 3

Where,

N_{SEC}: Number of secondary turns

N_{AUX}: Number of auxiliary turns

V_{Daux}: Diode forward voltage drop at auxiliary winding

V_{Dsec}: Voltage drop across SR MOSFET

$V_{ZCDP\_OVP\_min}$: Minimum voltage of the output overvoltage threshold

V_{OUT_OVP}: User-defined output overvoltage level

C7 is chosen to adjust the delay time, which starts when the drain-source voltage falls below the bus voltage until the ZCDP voltage falls to $V_{ZCDPthr}$ (100 mV, typ.). Therefore, the power switch can be turned on at the valley point of the drain-source voltage.

A total 44 µF capacitor for C8, C9 are applied to ensure stable system operation and enough break time for auto-restart protection. The VCCP linear regulator (R14, R27, D6, and Q4) is placed to avoid the VCCP voltage exceeds the pin voltage rating (32 V) in case of severe voltage spike coupling from the transformer during the surge test.

DC line overvoltage protection is detected by sensing the bus capacitor voltage through the VINP pin via the divider resistor R5. Once the VINP pin voltage is higher than the line overvoltage threshold V_{VINP_LOVP}, the controller enters the line overvoltage protection and releases the protection mode when the VINP pin voltage falls below V_{VINP_LOVP}.

Typical LOVP voltage is calculated as follows:

$$V_{BUS\_OVP} = V_{VINP\_LOVP} \times \frac{R6+R7+R5}{R5} = 2.80\ V \times \frac{1.3M\Omega+1.3M\Omega+17.4\ k\Omega}{17.4k\Omega} = 421\ V$$

Equation 4

The primary overcurrent protection is sensed by the R8 and R9 resistor through the CS pin. The V_{CSOCP1} is 0.76 V and V_{CSOCP2} is 1.1 V. The R8 and R9 are selected to ensure the system will not enter the overcurrent protection before the targeted OCP level is hit.

A low-cost RCD clamp consisting of the D2 diode, R25 resistor, and the C6 capacitor is implemented to suppress the peak drain voltage when turning off the power switch inside ICE188LM. This passive snubber helps dissipate the energy stored in the transformer leakage inductance.

5.2.2 CoolSET™ SiP secondary side

The secondary side of CoolSET™ ICE188LM SiP starts to take over the PWM control when the output voltage reaches 95% of its regulation target. The ICE188LM PWM control is based on sensing the reflected voltage from the primary side via the ZCDS pin and the error amplifier (EA) output voltage. ICE188LM integrated PWM and SR control ensures that the timing of the SR power switch (Q2 and Q3) and the primary-side power switch is well-synchronized, which avoids the cross conduction of the two switches and provides reliable synchronous rectification. In addition, the current injection function via the SR power switch (Q2 and Q3) enables zero-voltage switching operation on the primary side.

R20 is connected to CONF0 and serves as R_{SET0}. The value of R20 is determined by the transformer turns ratio, which is a critical parameter in the design. According to Table 4, the transformer turns ratio is specified as 8. Based on this value, R20 is set as 18 kΩ.

Table 4 Resistance for R_{SET0}

Turns ratio N_{MAIN}/N_{SEC}	R_{SET0}
5	3.9 kΩ
6	6.8 kΩ
7	12.0 kΩ
8	18.0 kΩ
9	27.0 kΩ
10	39.0 kΩ

R21 is connected to CONF1 and acts as R_{SET1}, defining the parameters for Hysteretic-mode operation. Choose options between 1 to 3 to finetune amount of loading for which system stays in Hysteretic mode. For this board, 3.9 kΩ (option 1 in Table 5) is chosen to keep the smallest power range operating in Hysteretic mode. For details, see the design guide [2].

Table 5 Resistance for R_{SET1}

Symbol / Parameter	Option	1	2	3	4	5	6
	R_{SET1}	3.9 kΩ	6.8 kΩ	12.0 kΩ	18.0 kΩ	27.0 kΩ	39.0 kΩ
EA voltage for wakeup in Hysteretic mode	V_{EA_HMOn}	1.25 V	1.20 V	1.10 V	1.25 V	1.20 V	1.10 V
EA voltage for off-phase in Hysteretic mode	V_{EA_HMOff}	0.95 V	0.9 V	0.8 V	0.95 V	0.9 V	0.8 V
EA voltage Hysteretic mode exit threshold	V_{EA_LHM}	1.4 V	1.4 V	1.4 V	1.6 V	1.6 V	1.6 V

The output voltage feedback is through the sense resistors R22 and R23 to the FB pin. The FB reference voltage is 1.2 V. A compensation network consisting of C12, C15, and R18 is implemented to stabilize the output voltage regulation. This network is carefully designed to ensure that the power supply's output voltage remains stable and within the desired range. For a detailed understanding of the compensation network's calculation, see the design guide [2].

To minimize output voltage ripple, the choice of output capacitors is crucial. The output capacitors C16, C18 are recommended to have low equivalent series resistance (ESR) type capacitor.

6 PCB layout

6.1 Top-side layout

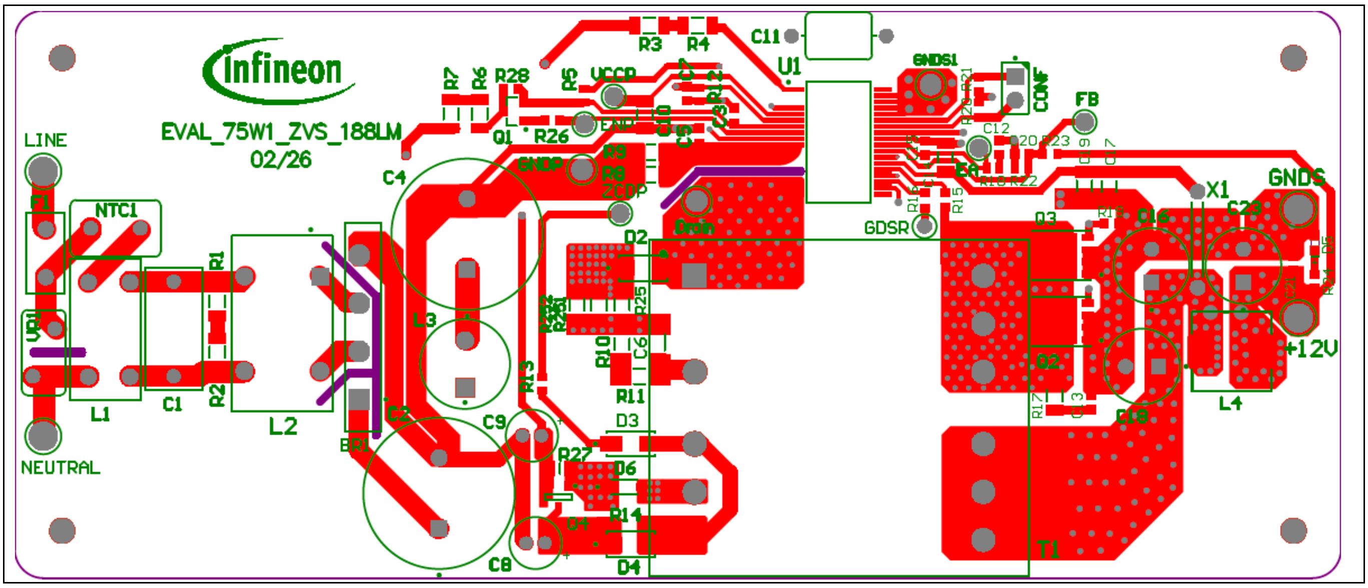


Figure 3 Top-side layout and component legend

6.2 Bottom-side layout

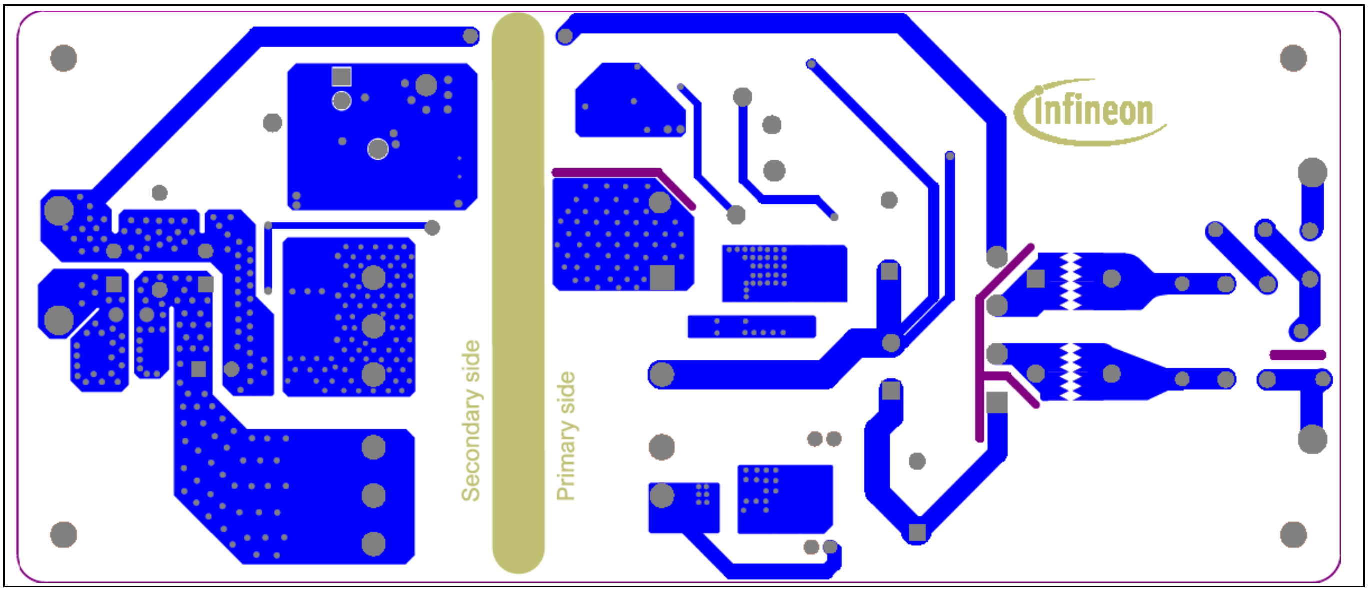


Figure 4 Bottom-side layout

7 Bill of materials

Table 6 BOM

No	Designator	Description	Manufacturer	Manufacturer order number	Qty
1	BR1	BRIDGE RECT 1PHASE 600 V 8 A GBU	Onsemi	GBU8J	1
2	C1	Safety capacitors 310 VAC 0.33 uF 20%	DGCX	MX2334KQ3C30 GB2000R	1
3	C10	MLCC - SMD/SMT 100 nF 50 VDC 10% 1206 X7T	–	–	1
4	C11	Safety capacitors 1500 pF 310 V 20%	Yageo	C741U152MSWD CA7317	1
5	C12	MLCC - SMD/SMT 50 Volts 68 nF X7R 10% 0603	–	–	1
6	C13	MLCC - SMD/SMT 100 Volts 220 pF X7R 10% 0603	–	–	2
7	C14, C19	MLCC - SMD/SMT 100 nF 50 V 10% 1206	–	–	2
8	C15	MLCC - SMD/SMT 50 Volts 1.5 nF X7R 10% 0603	–	–	1
9	C16, C18	CAP ALUM POLY 1200 uF 20% 16 V T/H	Nichicon	RNL1C122MDS1 KX	2
10	C17	MLCC - SMD/SMT 10 uF 50 V 10% 1206	–	–	1
11	C2, C4	Aluminium electrolytic capacitors - Radial leaded 82 uF 450 V	Rubycon	450HXW82MEFR 16X25	2
12	C21	MLCC - SMD/SMT 100 nF 50 V 10% 0603	–	–	1
13	C23	Aluminium electrolytic capacitors - Radial leaded 180 uF 25 V	Panasonic Electronics	25SEPF180M	1
14	C3	MLCC - SMD/SMT 100 Volts 820 pF C0G/NP0 1% 0603	–	–	1
15	C5, C20	MLCC - SMD/SMT 50 Volts 680 pF X7R 10% 0603	–	–	2
16	C6	MLCC - SMD/SMT 1000 PF 1kV 10% 1206	–	–	1
17	C7	MLCC - SMD/SMT 50 Volts 33 pF X7R 10% 0603	–	–	1
18	C8, C9	Aluminium electrolytic capacitors - Radial leaded 22 uF 35 V	BERYL	RG035M220LO5* 11TA-1A1E	2
19	CONF	Connector header through hole 2 position 0.100" (2.54 mm)	Samtec	TSW-102-08-G-S	1
20	D2	Surface mount rectifier 1.0 A/1000 V	Onsemi	S1M	1
21	D3, D4	DIODE SCHOTTKY 200 V 1A DO214AC	Micro Commercial Co	SS1200-LTP	2
22	D5	Chip LED Waterclear, size 0603, blue	Würth Elektronik	150060BS75003	1

No	Designator	Description	Manufacturer	Manufacturer order number	Qty
23	D6	Zener diode 22 V 500 mW ±2% surface mount SOD-123	Vishay	MMSZ5251C-E3-08	1
24	Drain, GNDP, GNDS1	Test point THT, white	Keystone Electronics Corp.	5012	3
25	EA, ENP, FB, GDSR, VCCP, ZCDP	Test point THT, white	Keystone Electronics Corp.	5002	6
26	F1	Time lag fuse, 300 V, 3.15 A	Littelfuse	36913150000	1
27	GNDS, +12V, LINE, NEUTRAL	Solder terminal, double turret, .109 long	Keystone Electronics Corp.	1502-2	4
28	L1	Inductor Common mode standard polarization core 4 pins, 400 uH	Endela Electronics	L-13-0100	1
29	L2	Inductor Common mode standard polarization core 4 pins, 10 mH	Tenda	TD1515-10MH 0.2*1.5	1
30	L3	Radial leaded wire wound inductor WE-TI, 10 uH 4.70 A	Würth Elektronik	7447452100	1
31	L4	Jumper	Multicomp Pro	TCW25 250G	1
32	NTC1	Power NTC 2.5ohm Y kink bulk	Bourns	BN-LG08Y2R5MYB	1
33	Q1	SIPMOS small-signal transistor	Infineon Technologies	BSS127H6327XTSA2	1
34	Q3	Power-transistor, optimized for high performance SMPS	Infineon Technologies	ISC027N10NM6ATMA1	1
35	Q4	Bipolar transistors - SOT-23, 45 V, 800 mA, NPN	Diotec	BC817-25	1
36	R1, R2	Thick film resistors - SMD 1/4 Watt 1.2Mohms 1206 5%	–	–	2
37	R10, R11	Thick film resistors - SMD 1/4 Watt 150kohms 1206 1%	–	–	2
38	R12	Thick film resistors - SMD 2kohms 1% 0603	–	–	2
39	R13, R18	Thick film resistors - SMD 22kohms 1% 0603	–	–	2
40	R14, R15	Thick film resistors - SMD 15kohms 100 mW 0603 1%	–	–	1
41	R16	Thick film resistors - SMD 0603 2.2 ohms 1%	–	–	1
42	R17	Thick film resistors - SMD 1/4 Watt 51 ohms 1206 5%	–	–	2

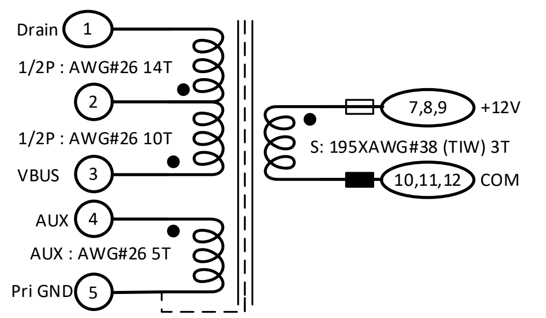
No	Designator	Description	Manufacturer	Manufacturer order number	Qty
43	R19	Thick film resistors - SMD 10kohms 100 mW 0603 1%	–	–	1
44	R20	Thick film resistors - SMD 18kohms 1% 0603	–	–	1
45	R21	Thick film resistors - SMD 3.9kohms 1% 0603	–	–	1
46	R22	Thick film resistors - SMD 20kohms 100 mW 0603 1%	–	–	1
47	R23	Thick film resistors - SMD 180kohms 0603 1%	–	–	1
48	R24	Thick film resistors - SMD 5.1kohms 100 mW 0603 1%	–	–	1
49	R25	Thick film resistors - SMD 1/4 Watt 15 ohms 1206 1%	–	–	1
50	R26	Thick film resistors - SMD 0 ohm 0603	–	–	1
51	R27	Thick film resistors - SMD 120k ohms 0805	–	–	1
52	R3, R4	Thick film resistors - SMD 50k ohms 250 mW 1206 1%	–	–	2
53	R5	Thick film resistors - SMD 17.4k ohms 500 mW 0603 1%	–	–	1
54	R6, R7	Thick film resistors - SMD 1/4 Watt 1.3M ohms 1206 1%, 500V rating	–	–	2
55	R8, R9	Thick film resistors - SMD 1206 0.43 ohm 1%	Bourns	CRL1206-FW-R430ELF	2
56	T1	Transformer PQ3220, Lp = 250 µH, 750345891Rev00	Würth Elektronik	750345891	1
57	U1	CoolSET™ SiP ICE188LM	Infineon Technologies	ICE188LM	1
58	VR1	Varistors 275 VAC 10% 7 mm	Bourns	CV275K7BL1	1
59	X1	Through hole jumper, 10.16 mm pitch, 2 pins	Samtec	JL-400-25-T	1

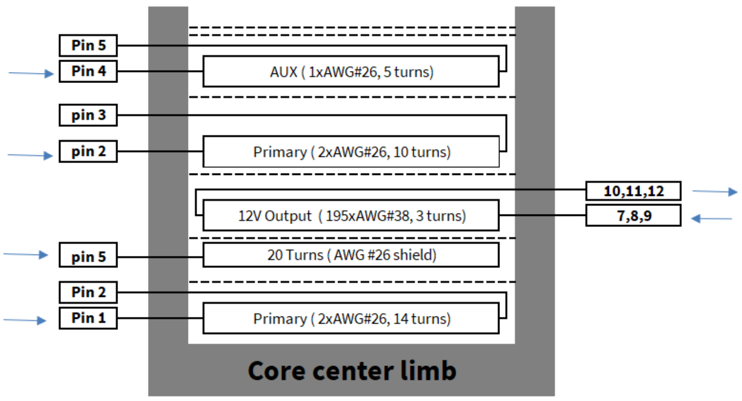
8 Transformer specification

8.1 Electrical diagram and coil build

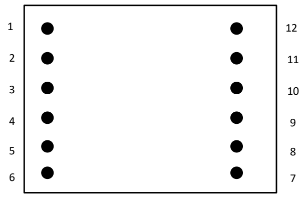
- Manufacturer and part number: Würth Electronik (750345891)

Core: PQ3220, L_p=250 µH, 24T: 3T: 5T (N_p : N_{s1} : N_{aux})



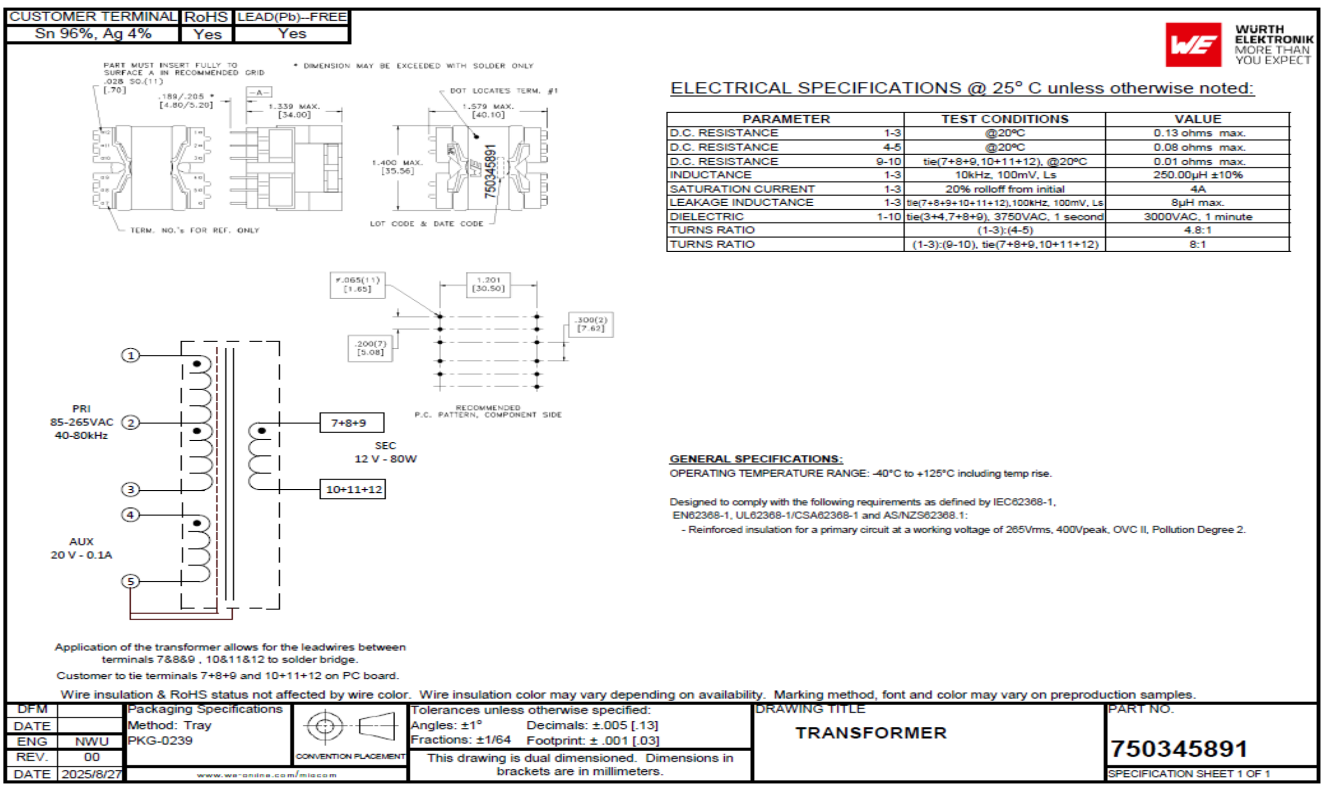


Top view (PQ3220)



Wire size requirement :

Start	Stop	No. of turns	Wire size	Layer
1	2	14	2 x AWG#26	1/2 Primary
5		20	1 x AWG#26	SHIELD
7,8,9	10,11,12	3	195 x AWG#38 (TIW)	Secondary
2	3	10	2 x AWG#26	1/2 Primary
4	5	5	1 x AWG#26	AUX



ELECTRICAL SPECIFICATIONS @ 25° C unless otherwise noted:

PARAMETER		TEST CONDITIONS	VALUE
D.C. RESISTANCE	1-3	@20°C	0.13 ohms max.
D.C. RESISTANCE	4-5	@20°C	0.08 ohms max.
D.C. RESISTANCE	9-10	tie(7+8+9,10+11+12), @20°C	0.01 ohms max.
INDUCTANCE	1-3	10kHz, 100mV, Ls	250.00µH ±10%
SATURATION CURRENT	1-3	20% rolloff from initial	4A
LEAKAGE INDUCTANCE	1-3	tie(7+8+9+10+11+12),100kHz, 100mV, Ls	8µH max.
DIELECTRIC	1-10	tie(3+4,7+8+9), 3750VAC, 1 second	3000VAC, 1 minute
TURNS RATIO		(1-3):(4-5)	4.8:1
TURNS RATIO		(1-3):(9-10), tie(7+8+9,10+11+12)	8:1

GENERAL SPECIFICATIONS:
OPERATING TEMPERATURE RANGE: -40°C to +125°C including temp rise.

Designed to comply with the following requirements as defined by IEC62368-1, EN62368-1, UL62368-1/CSA62368-1 and AS/NZS62368.1:
- Reinforced insulation for a primary circuit at a working voltage of 265Vrms, 400Vpeak, OVC II, Pollution Degree 2.

Application of the transformer allows for the leadwires between terminals 7&8&9 , 10&11&12 to solder bridge.
Customer to tie terminals 7+8+9 and 10+11+12 on PC board.
Wire insulation & RoHS status not affected by wire color. Wire insulation color may vary depending on availability. Marking method, font and color may vary on preproduction samples.

DFM | DATE | ENG NWU | REV. 00 | DATE 2025/8/27
Packaging Specifications Method: Tray PKG-0239
CONVENTION PLACEMENT
Tolerances unless otherwise specified: Angles: ±1° Decimals: ±.005 [.13] Fractions: ±1/64 Footprint: ± .001 [.03]
This drawing is dual dimensioned. Dimensions in brackets are in millimeters.
DRAWING TITLE: TRANSFORMER
PART NO. 750345891
SPECIFICATION SHEET 1 OF 1

Figure 5 Electrical diagram and coil structure

9 Test results

All performance data is measured at room temperature T_a=25°C unless otherwise specifically mentioned.

9.1 Efficiency

Efficiency data has been taken under +12 V load condition with NTC1 shorted. The average efficiency at 230 VAC input is 93.72% and the standby power at 230 VAC input is 39.5 mW. LED (D5) is further disconnected for measurement under no load condition.

Table 7 Efficiency

Input (VAC/Hz)	Load percentage (%)	P_{IN} (W)	V_{OUT} (V DC)	I_{OUT} (A)	P_{OUT} (W)	Efficiency η (%)	Average η (%)
90/60	No load	0.0140	11.9900	0.0000			
	10	8.2320	12.0200	0.6241	7.5017	91.13	
	25	20.1318	12.0190	1.5600	18.7496	93.13	92.39
	50	40.3044	12.0210	3.1181	37.4827	92.99	
	75	60.9780	12.0140	4.6763	56.1811	92.13	
	100	81.9840	12.0060	6.2344	74.8502	91.30	
115/60	No load	0.0172	11.9900	0.0000			
	10	8.2626	12.0210	0.6241	7.5023	90.79	
	25	20.0718	12.0180	1.5600	18.7481	93.40	93.11
	50	39.9774	12.0190	3.1181	37.4764	93.74	
	75	60.3000	12.0160	4.6763	56.1904	93.18	
	100	81.2940	12.0100	6.2353	74.8860	92.12	
230/50	No load	0.0395	11.9900	0.0000			
	10	8.3856	12.0190	0.6240	7.4999	89.43	
	25	20.2104	12.0190	1.5600	18.7496	92.77	93.72
	50	39.8616	12.0160	3.1172	37.4563	93.96	
	75	59.6418	12.0130	4.6763	56.1764	94.18	
	100	79.6560	12.0060	6.2344	74.8502	93.96	
264/50	No load	0.0478	11.9900	0.0000			
	10	8.4336	12.0190	0.6241	7.5011	88.94	
	25	20.2698	12.0150	1.5600	18.7434	92.47	93.64
	50	39.9270	12.0150	3.1181	37.4640	93.83	
	75	59.6448	12.0110	4.6763	56.1670	94.16	
	100	79.5660	12.0040	6.2353	74.8485	94.07	

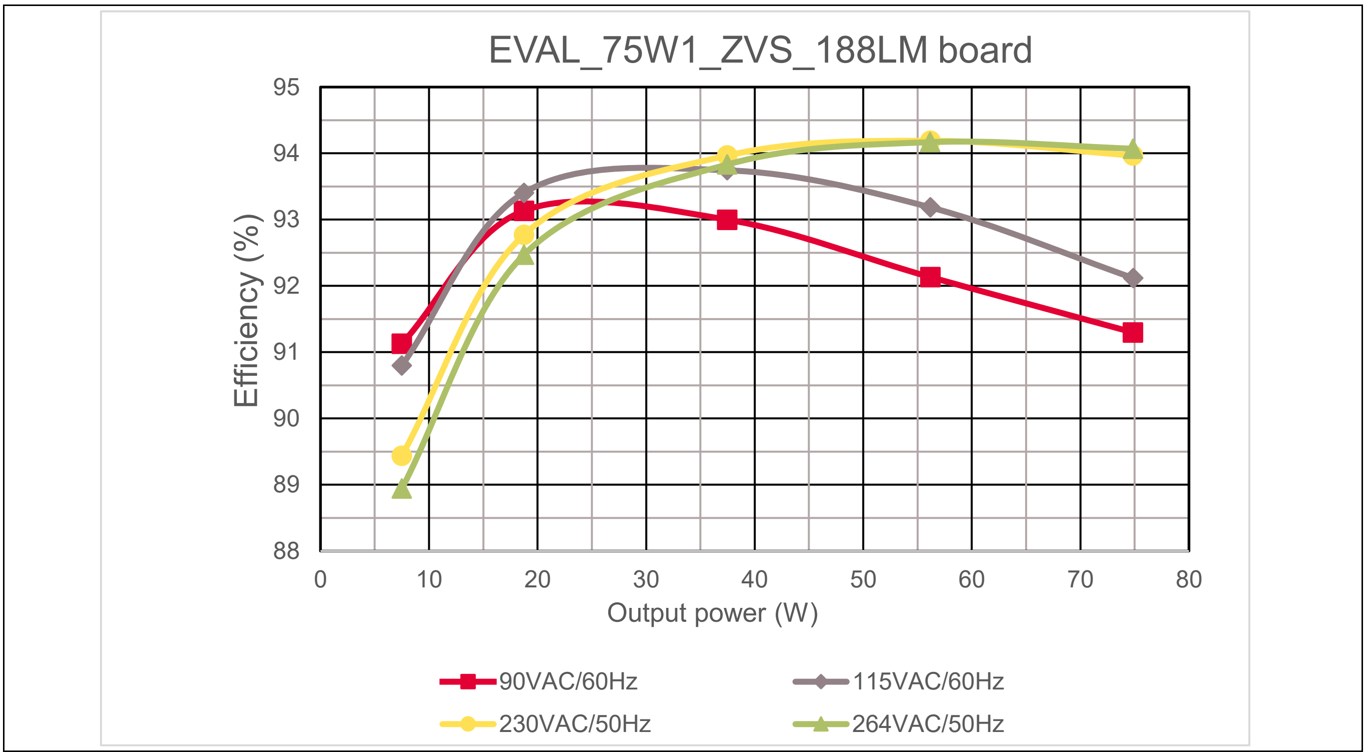


Figure 6 **Efficiency (%) vs. output power (W)**

9.2 ESD immunity (EN 61000-4-2)

The evaluation board is subjected to ESD testing according to EN 61000-4-2 level 3 (±8 kV contact and ±15 kV air discharge). It is tested at full load (resistive load) and it meets criteria A (normal performance within the specification limits).

Table 8 **ESD immunity test result**

Description	ESD test	Level	Number of strikes				Test result
			Vout	GNDS	Line	Neutral	
230 VAC, 75 W	Contact	±8 kV	10	10	10	10	Pass
	Air	±15 kV	10	10	10	10	Pass

9.3 Surge immunity (EN 61000-4-5)

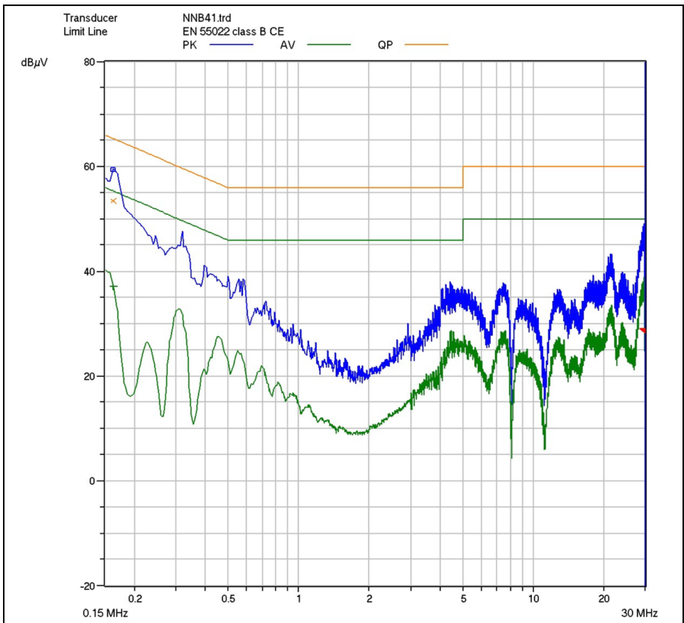
The evaluation board is subjected to a surge immunity test according to EN 61000-4-5 level 4 (±2 kV Differential mode and ±4 kV Common mode). It is tested at full load (resistive load) and it meets criteria A (normal performance within the specification limits).

Table 9 **Surge immunity test result**

Description	Test	Level		Number of strikes				Test result
				0°	90°	180°	270°	
230 VAC, 75 W	Differential mode	±2 kV	L → N	3	3	3	3	Pass
	Common mode	±4 kV	L → G	3	3	3	3	Pass
		±4 kV	N → G	3	3	3	3	Pass

9.4 Conducted emissions (EN 55022 Class B)

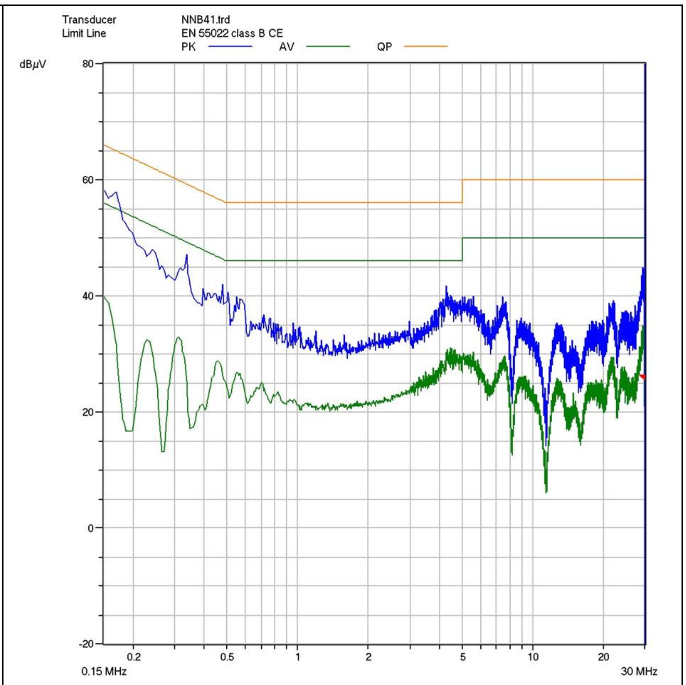
Conducted EMI was measured by Schaffner (SMR4503) and followed the test standard of EN 55022 (CISPR 22) Class B. The evaluation board was connected to resistive load with input voltage of 115 VAC and 230 VAC.



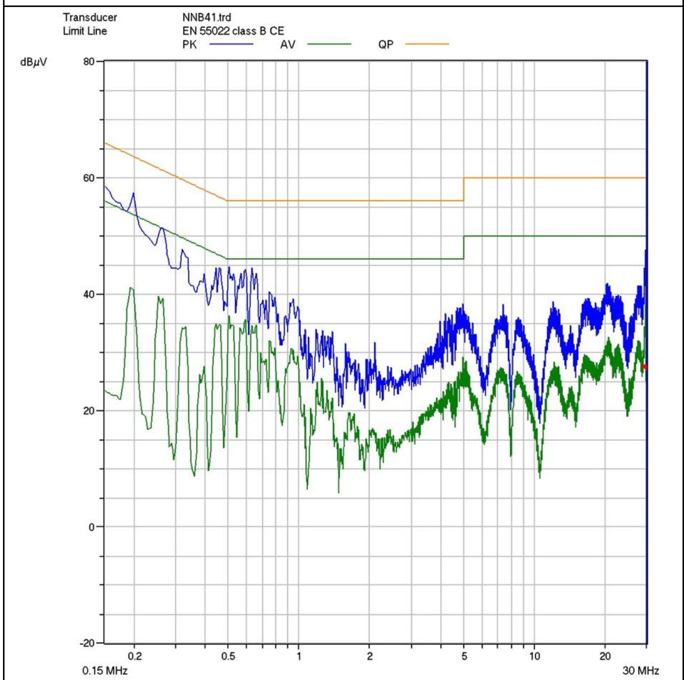
Final Measurement Results: * = Limit exceeded

Frequency		Level Pk		Level AV		Level QP	Limit AV	Limit QP	Notes
0.1620	L	59.5	L	37.2	L	53.5	55.4	65.4	

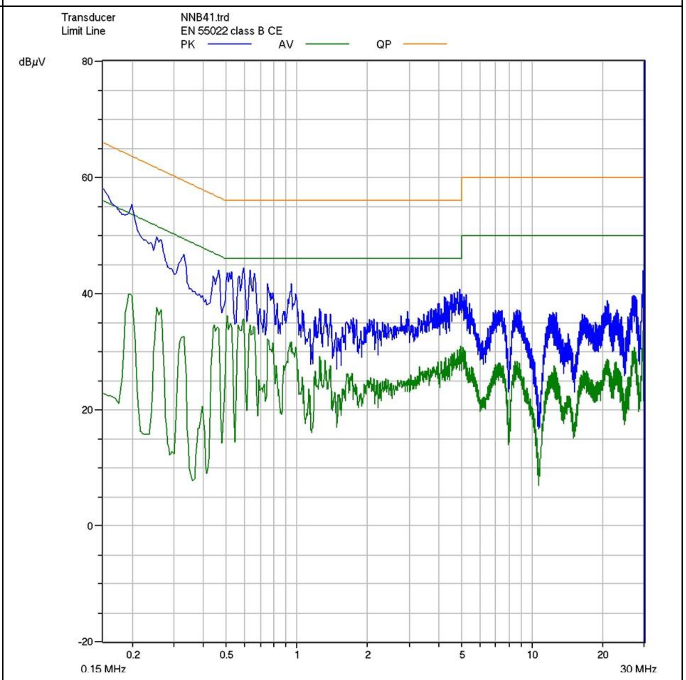
Conducted emission at 115 VAC Line



Conducted emission at 115 VAC Neutral



Conducted emission at 230 VAC Line



Conducted emission at 230 VAC Neutral

Figure 7 Conducted emissions

9.5 Thermal measurement

The thermal testing of the evaluation board was executed in open air without forced ventilation at an ambient temperature of 26°C. An infrared thermography camera (FLIR-T62101) was used to capture the thermal reading of critical components. The measurements were taken at the maximum load running for one hour with NTC1 shorted. The tested input voltages were 90 VAC and 264 VAC.

Table 10 Component temperature at full load under Ta = 26°C

Reference designator	Major component	90 VAC (°C)	264 VAC (°C)
R25	Primary side RCD snubber	53.7	55.2
IC1	ICE188LM	68.7	53.1
Q3	SR MOSFET	53.7	55.2
BR1	Bridge diode	68.0	41.8
T1	Main transformer winding	58.8	60.6

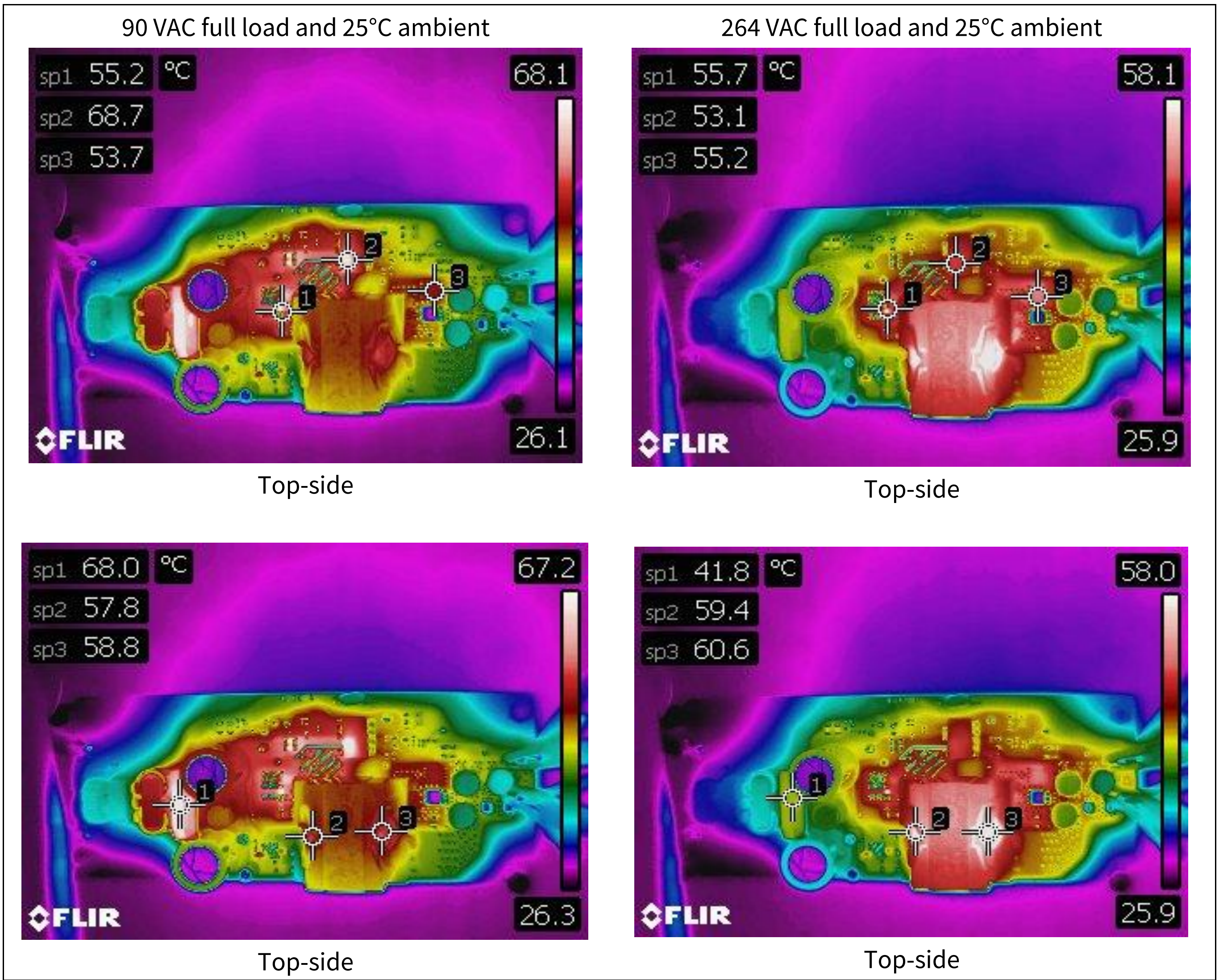


Figure 8 Infrared thermal image of EVAL_75W1_ZVS_188LM

10 Waveforms and scope plots

All waveforms and scope plots were recorded with a Teledyne LeCroy HDO6104 oscilloscope.

10.1 Start-up with maximum load

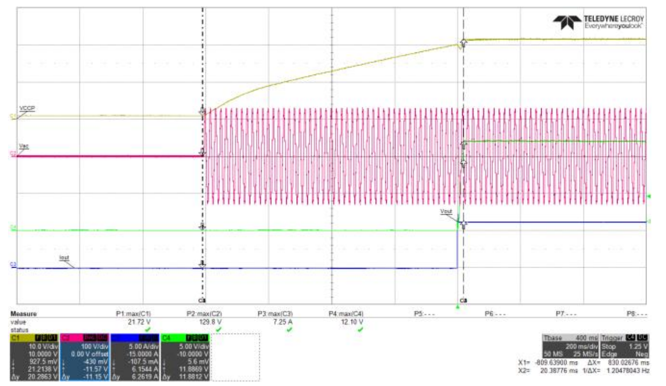
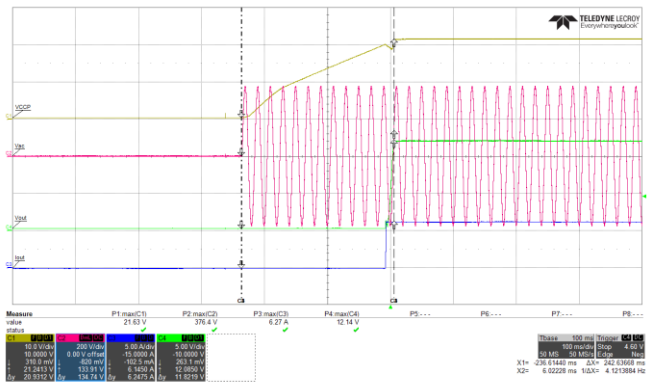
	
C1 (yellow) : VCCP voltage (V_{VCCP}) C2 (purple) : AC line voltage (V_{AC}) C3 (blue) : Output current (I_{OUT}) C4 (Green) : Output voltage (V_{OUT})	C1 (yellow) : VCCP voltage (V_{VCCP}) C2 (purple) : AC line voltage (V_{AC}) C3 (blue) : Output current (I_{OUT}) C4 (Green) : Output voltage (V_{OUT})
Start-up time at 90 VAC and maximum load ≈ 830 ms	Start-up time at 264 VAC and maximum load ≈ 242 ms
The board can startup as expected over 90~264 VAC, output voltage smoothly rises and regulates at 12 V.	

Figure 9 Start-up

10.2 Soft-start

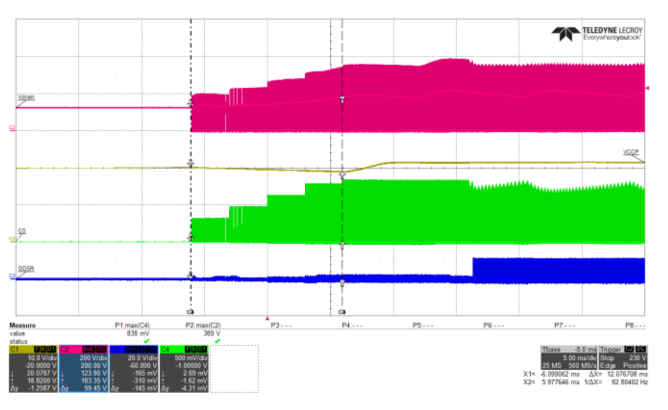
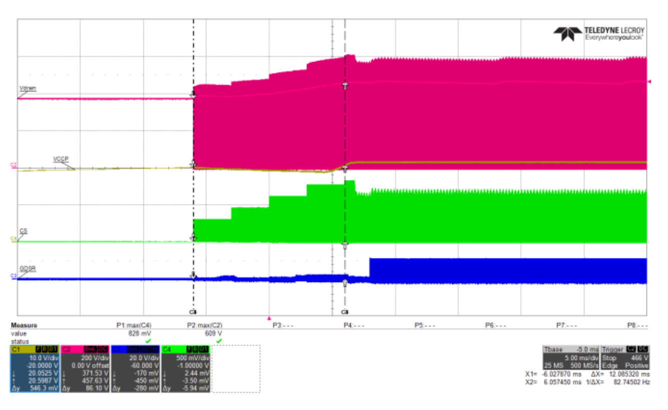
	
C1 (yellow) : VCCP voltage (V_{VCCP}) C2 (purple) : Drain voltage (V_{DRAIN}) C3 (blue) : SR Gate (V_{GDSR}) C4 (Green) : CS Voltage (V_{CS})	C1 (yellow) : VCCP voltage (V_{VCCP}) C2 (purple) : Drain voltage (V_{DRAIN}) C3 (blue) : SR Gate (V_{GDSR}) C4 (Green) : CS Voltage (V_{CS})
Soft-start time at 90 VAC and maximum load ≈ 12 ms	Soft-start time at 264 VAC and maximum load ≈ 12 ms
Stepped soft-start from V_{SS1}(typ. 0.3 V) to V_{CSOCP1}(typ. 0.8 V)	

Figure 10 Soft-start

10.3 Switching waveform at full load

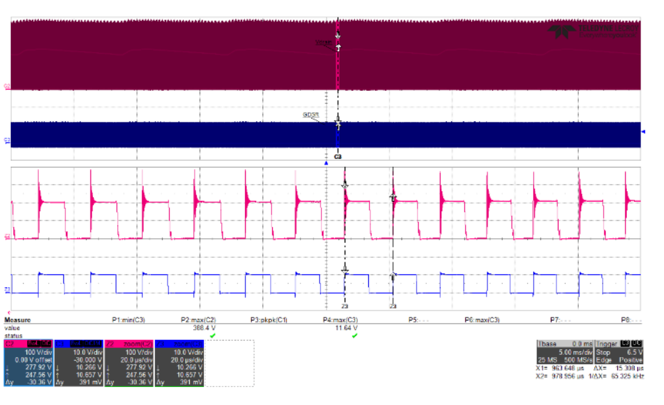
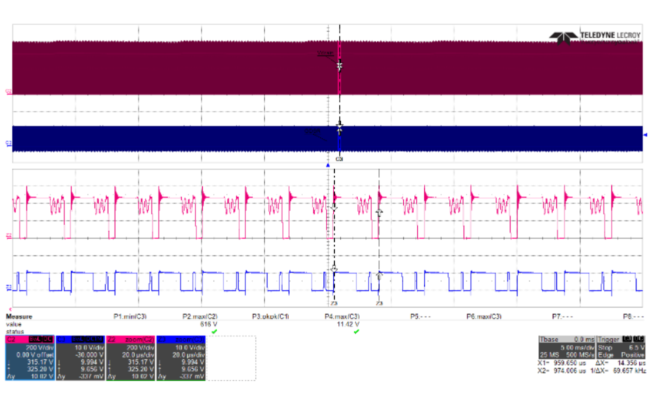
	
C2 (purple) : Drain voltage (V_{DRAIN}) C3 (blue) : SR gate (V_{GDSR})	C2 (purple) : Drain voltage (V_{DRAIN}) C3 (blue) : SR gate (V_{GDSR})
VIN = 90 VAC, full load; the first valley is measured (QR=1 at low line) V_{DS_MAX} = 388V , $f_{switching}$ = 65.3 kHz	VIN = 264 VAC, full load; the third valley is measured (QR=3 at high line with ZVS switching) V_{DS_MAX} = 616V , $f_{switching}$ = 69.6 kHz
ICE188LM operates quasi-resonant valley switching at low line and together with zero voltage switching at high line.	

Figure 11 Drain and CS voltage at maximum load

10.4 SR FET voltage at full load

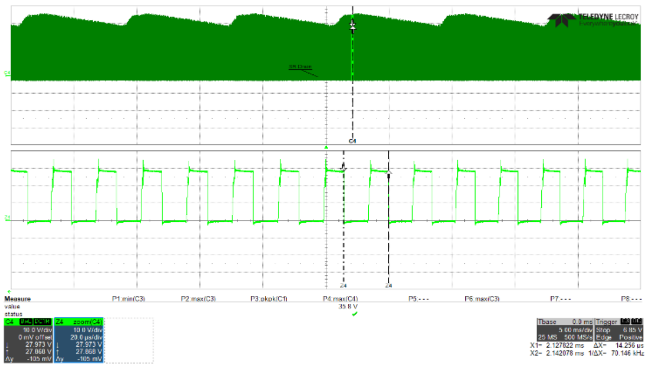
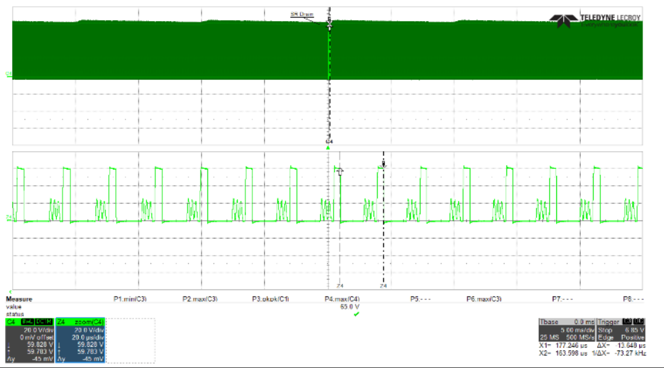
	
C4 (green) : SR drain voltage (V_{SR_Drain})	C4 (green) : SR drain voltage (V_{SR_Drain})
V_{IN} = 90 VAC, full load. Maximum drain voltage is around 35.8 V	V_{IN} = 264 VAC, full load. Maximum drain voltage is around 65.0 V
The measured SR MOSFET voltage stress at 264 VAC input is well below its voltage rating (100 V).	

Figure 12 SR FET voltage

10.5 Output ripple voltage at maximum load

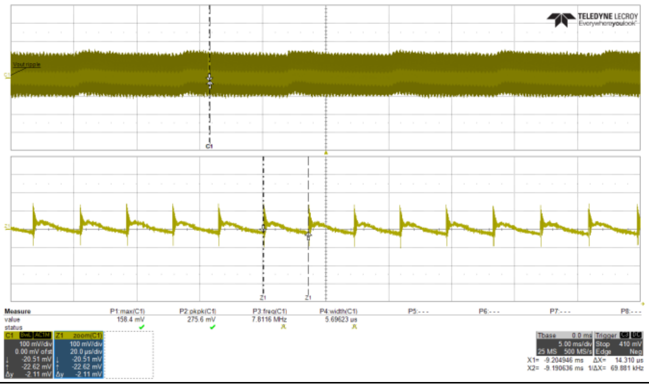
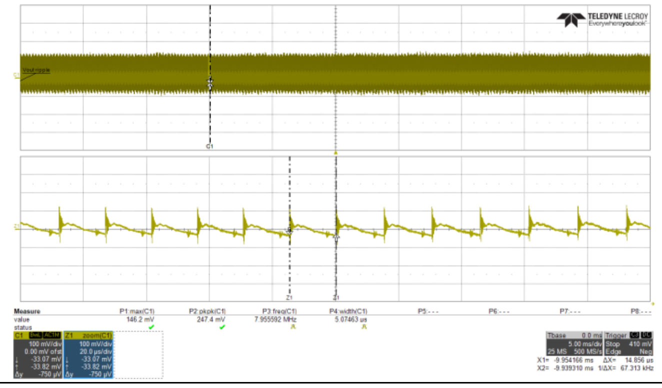
	
C1 (yellow) : +12 V output ripple voltage	C1 (yellow) : +12 V output ripple voltage
VIN = 90 VAC, full load Vripple_pk for +12 V output voltage: 275.6 mV	VIN = 90 VAC, full load Vripple_pk for +12 V output voltage: 247.4 mV
The measured output ripple is around 2.3% of the output voltage.	

Figure 13 Output ripple voltage at full load (20 MHz bandwidth and 47 µF electrolytic capacitor in parallel with 0.1 µF ceramic capacitor)

10.6 Hysteretic mode operation

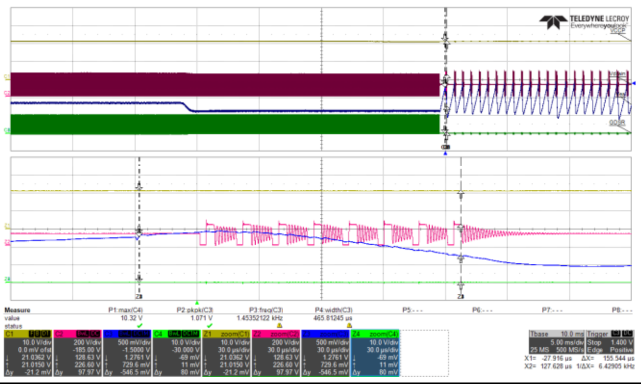
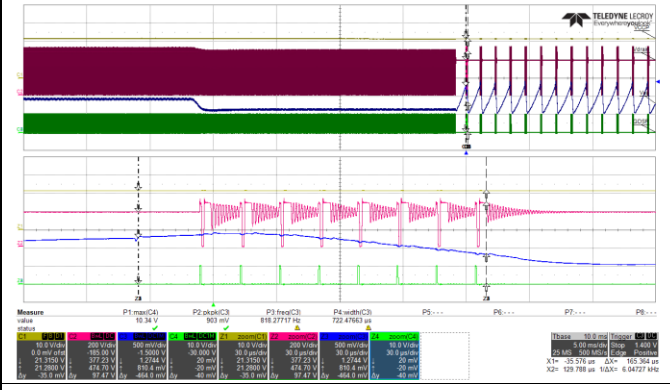
	
C2 (purple) : Drain voltage (V_{DRAIN}) C3 (blue) : EA voltage(V_{EA}) C4 (green) : SR gate (V_{GDSR})	C2 (purple) : Drain voltage (V_{DRAIN}) C3 (blue) : EA voltage(V_{EA}) C4 (green) : SR gate (V_{GDSR})
90 VAC, 8.4 W -> 2.4 W load Operation at f_{osc_ABM} = 59.2 kHz	264 VAC, 8.4 W -> 1.2 W load Operation at f_{osc_ABM} = 53.9 kHz
When the load reduces to < 1.2 W load, the system enters the Hysteretic mode to reduce the power loss.	

Figure 14 Hysteretic mode operation

10.7 Overload protection

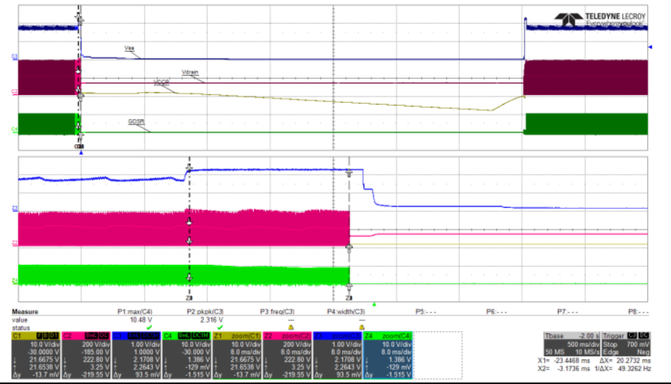
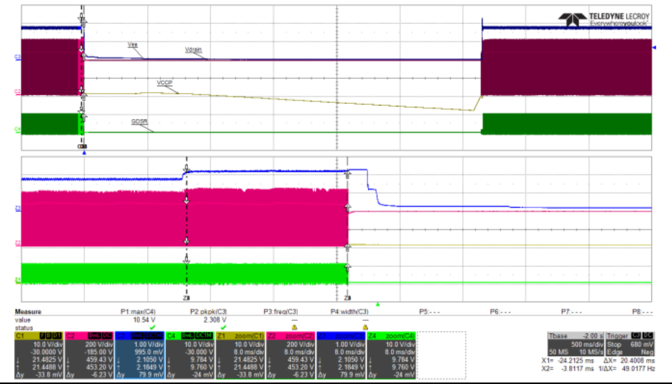
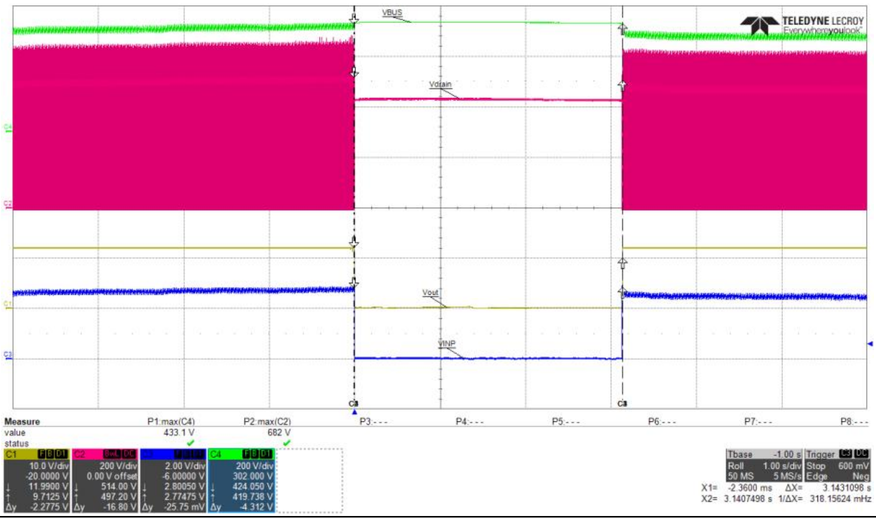
	
C1 (yellow) : VCCP voltage (V_{VCCP}) C2 (purple) : Drain voltage (V_{DRAIN}) C3 (blue) : EA Voltage (V_{EA}) C4 (Green) : SR Gate (V_{GDSR})	C1 (yellow) : VCCP voltage (V_{VCCP}) C2 (purple) : Drain voltage (V_{DRAIN}) C3 (blue) : EA Voltage (V_{EA}) C4 (Green) : SR Gate (V_{GDSR})
90 VAC, 75 W load steps to 97 W loads. System enters auto restart protection when V_{EA} >2.1 V and blanking time ~20 ms	264 VAC, 75 W load steps to 97 W loads. System enters auto restart protection when V_{EA} >2.1 V and blanking time ~20 ms
System enters overload protection as expected during load increases to 97 W.	

Figure 15 Overload protection

10.8 Line OVP

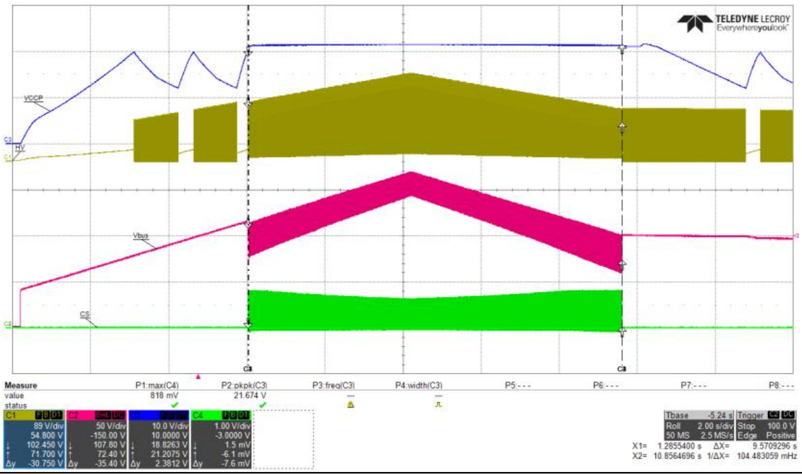


C1 (yellow) : Output voltage (V_{out})
C2 (purple) : Drain voltage (V_{DRAIN})
C3 (blue) : VINP voltage (V_{VINP})
C4 (green) : Bulk capacitor Voltage (V_{BUS})

Increase the input from 250 VAC to 300 VAC and decrease back to 230 VAC. Line OVP is measured at V_{BUS} > 424 VDC when the V_{VINP} >2.8 V. System enters non switch auto restart protection. The switching resumes when V_{BUS}<420 VDC.

Figure 16 Line OVP

10.9 Brown-in and brown-out



C1 (yellow) : HV voltage (V_{HV})
C2 (purple) : Bulk capacitor Voltage (V_{BUS})
C3 (blue) : VCCP voltage (V_{VCCP})
C4 (green) : CS Voltage (V_{CS})

Increase the input voltage from 30 VAC to 120 VAC and decrease back to 30 VAC. Brown-in is measured at V_{BUS} >107 VDC and brown-out is measured at V_{BUS} <72 VDC. Initially, the system is in non-switch auto restart protection mode and it resumes switching after brown-in. When the bulk capacitor voltage drops below brown-out, non-switch auto restart is triggered.

System enters brown-in and brown-out protection as expected.

Figure 17 Brown-in and brown-out

Design support

Developer community

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Technical support

Have technical queries? Consult experts from Infineon to get a fast turn-around by raising a request on the Technical Support page.

References

[1] Infineon Technologies AG: *CoolSET™ SiP ICE188LM datasheet*; Available online

[2] Infineon Technologies AG: *Design guide for ZVS QR flyback using CoolSET™ SiP*; Available online

Revision history

Document revision	Date	Description of changes
V 1.0	2026-06-02	Initial release

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