

XDP™ XDP72x-001 evaluation PCBA user guide

About this document

Scope and purpose

This document describes how to set up the XDP™ XDP72x-001 Evaluation Board and configure the internal registers to evaluate the performance of XDP72x 20 A digital eFuses.

Intended audience

This document is intended for test engineers who want to evaluate the performance of XDP72x-001 20 A digital eFuses.

About this product group

Target applications

- [Telecommunications infrastructure](#)
- [Data center and AI data center solutions](#)
- [Power conversion](#)

Product family

XDP™ is a high-performance digital power controller designed to optimize the IC for specific applications. They feature digital algorithms for high power efficiency and minimal standby power, digital parameter configuration for increased flexibility and lower development effort, and optimized bill of materials (BOM), making these controllers ideal for different application.

Evaluation Board

This board is to be used during the design-in process for evaluating and measuring characteristic curves, and for checking datasheet specifications.

Note: PCB and auxiliary circuits are NOT optimized for final customer design.

Reference Board

Product(s) embedded on a PCB with a focus on specific applications and defined use cases that may include software. PCB and auxiliary circuits are optimized for the requirements of the target application.

Note: Boards do not necessarily meet safety, EMI, quality standards (for example UL, CE) requirements.

Safety precautions

Safety precautions

Note: Please note the following warnings regarding the hazards associated with development systems.

Table 1 Safety precautions





	Warning: The evaluation or reference board contains DC bus capacitors which take time to discharge after removal of the main supply. Before working on the drive system, wait five minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury.
	Caution: The heat sink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.
	Caution: The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.
	Caution: The evaluation or reference board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.

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1 Introduction

1 Introduction

XDP™ XDP72x-001 eFuses are the latest members of the XDP™ protection IC family, with an integrated digital hot-swap controller, a low RDS(on) OptiMOS™ MOSFET, and a current sensor. Infineon's XDP72x-001 digital eFuses are highly integrated, wide-input-voltage devices designed for system monitoring and protection. These devices are fully digital, configurable, and support a PMBus® communication interface, enabling direct access to their register map for feature configuration through a PC-based software tool by using a USB0010 series dongle. This dongle serves as a PC-to-PMBus® bridge, allowing communication between a USB COM port and XDP720-001 eFuse (as well as other XDP7xx family devices).

This guide provides instructions for setting up the evaluation board and configuring its internal registers, and provides details of how to evaluate the performance of XDP72x-001, specifically:

- Inrush current regulation
- Safe operating area (SOA) protection for the integrated FET during startup
- Fault detection and protection features

2 Hardware and software requirements

2 Hardware and software requirements

The following hardware and software are required for the setup:

- XDP72x-001 Evaluation Board shown in [Figure 1](#)
- XDP™ Designer USB dongle USB0010 shown in [Figure 2](#)
- XDP™ Designer graphical user interface (GUI) shown in [Figure 3](#)

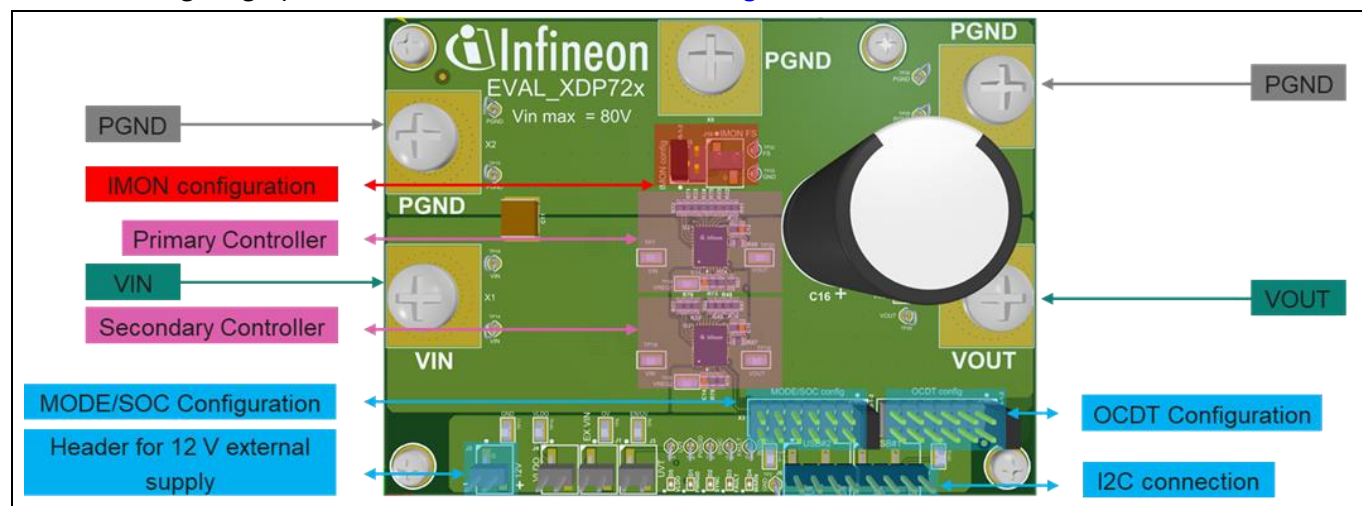


Figure 1 XDP72x-001 Evaluation Board



Figure 2 USB0010 dongle

2 Hardware and software requirements

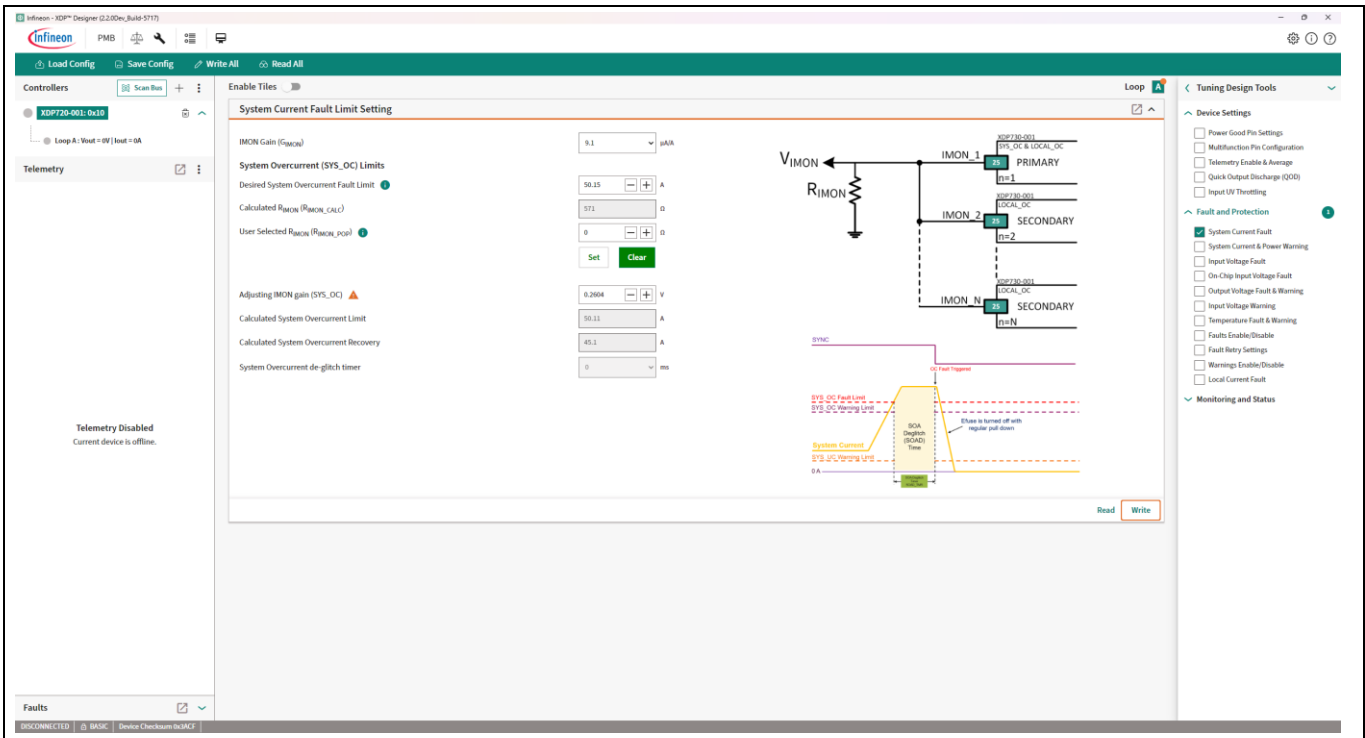


Figure 3 XDP™ Designer GUI

3 XDP72x-001 evaluation platform

3 XDP72x-001 evaluation platform

The following sections describe the XDP72x-001 Evaluation Board highlighting the electrical specifications, block diagram, schematics, layout, bill of materials (BOM), and different configuration settings that could be used on this evaluation board.

3.1 Electrical specifications

- Input and output voltage range: 7 V_{DC} to 80 V_{DC}
- Maximum continuous current: 40 A

3.2 Block diagram

The XDP72x-001 evaluation platform consists of:

- **XDP72x-001 Evaluation Board:** Positive-input eFuses and the circuitry designed to run multiple eFuses in parallel with built-in FETs. Additionally, communication, control, and protection circuitry are included in the package
- **USB0010 dongle:** The interface between the PC and XDP720-001 that communicates via the USB dongle. The commands are sent by the XDP™ Designer GUI to the XDP720-001 device, which are received via PMBus® communication. The USB0010 dongle translates these commands from USB to PMBus®
- **XDP™ Designer GUI:** Software GUI tool for XDP720-001 PMBus® communication that provides commands for configuration and general control

3 XDP72x-001 evaluation platform

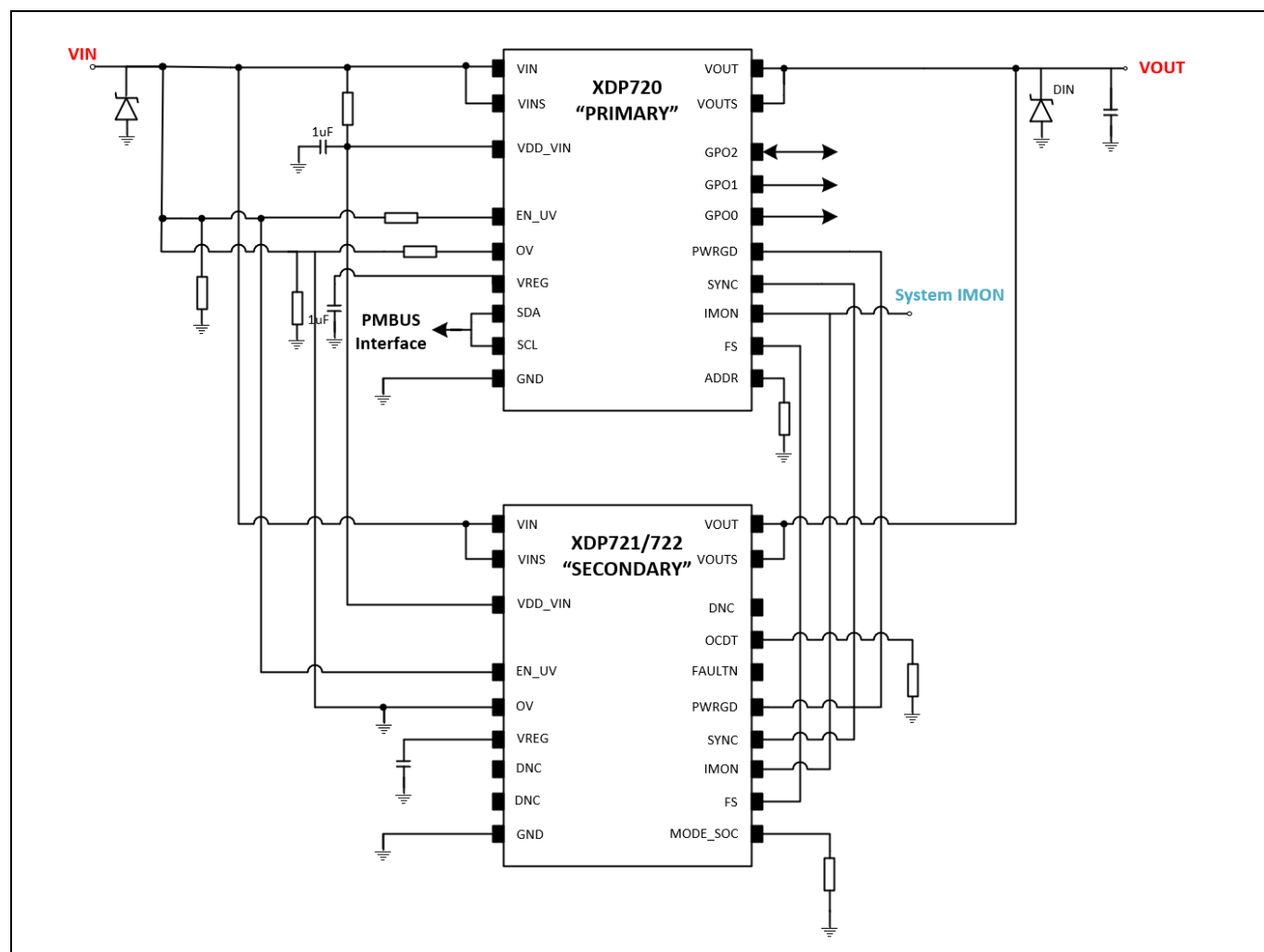


Figure 4 XDP72x-001 evaluation platform

3 XDP72x-001 evaluation platform

3.3 XDP72x-001 Evaluation Board schematics

Figure 5 shows the schematic for the XDP72x-001 Evaluation Board, with one XDP720-001 (with PMBus®) and one XDP721-001 (without PMBus®) in parallel for higher continuous current.

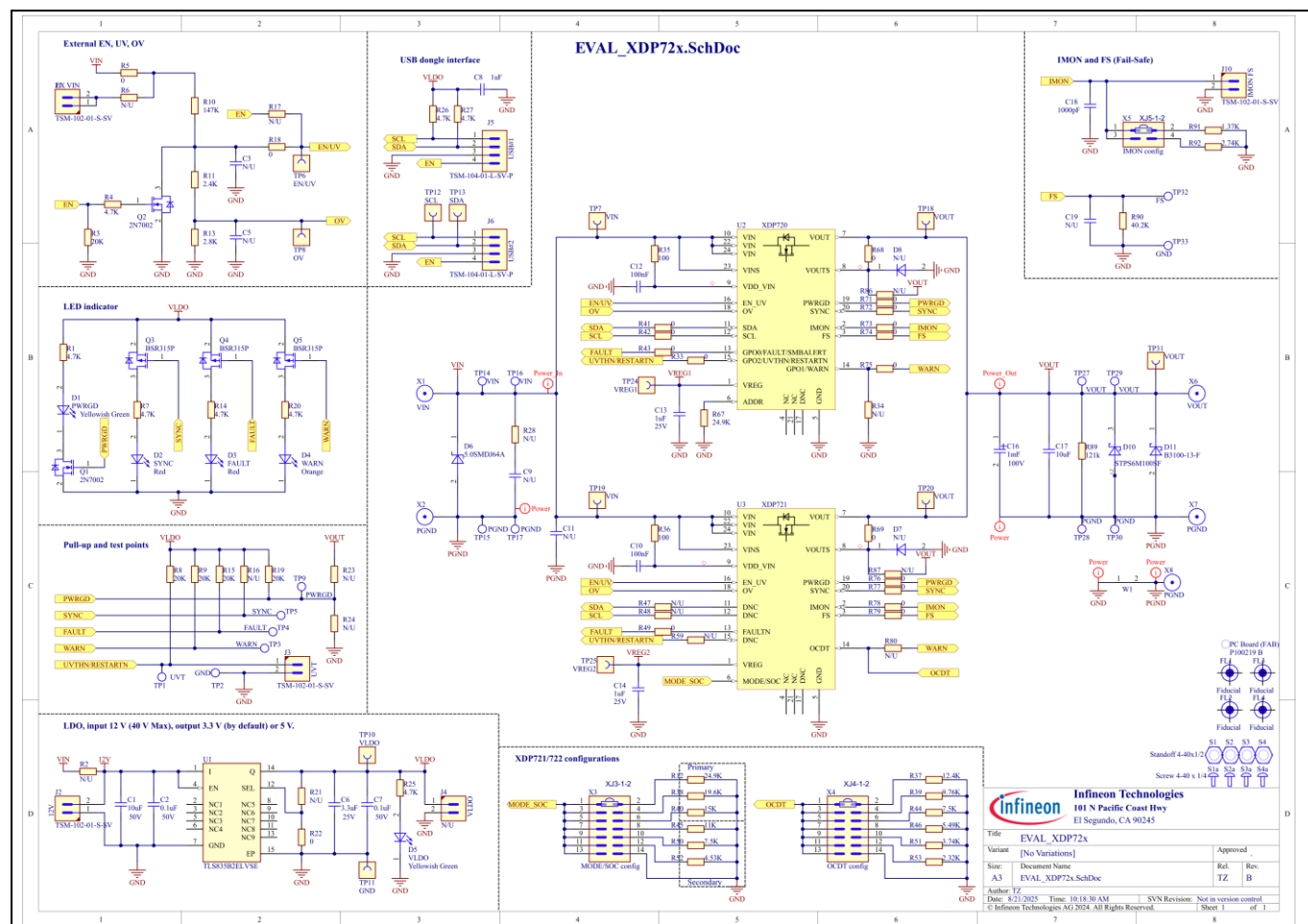


Figure 5 XDP72x-001 Evaluation Board schematics

3 XDP72x-001 evaluation platform

3.4 XDP72x-001 Evaluation Board layout

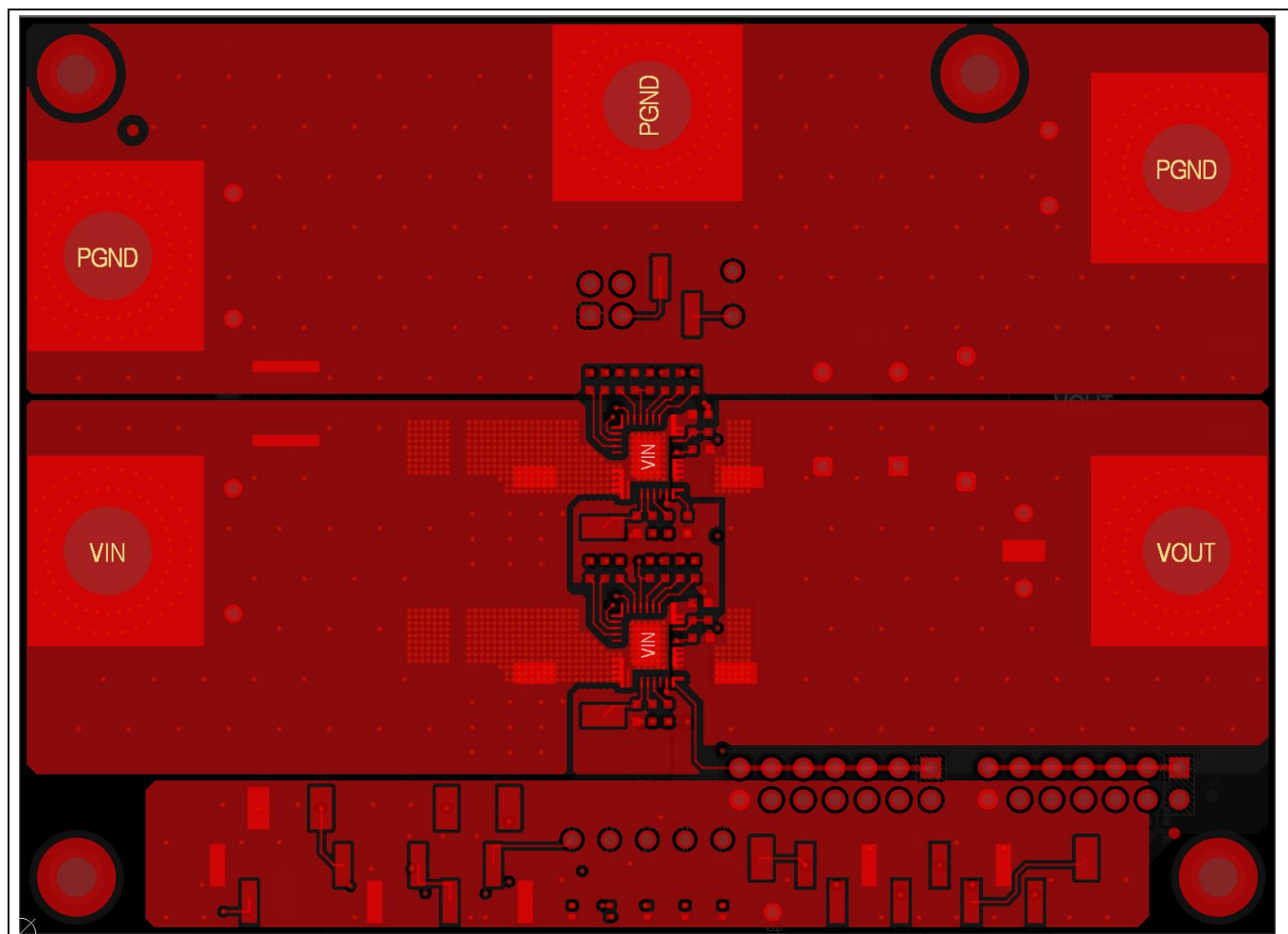


Figure 6 Top layer layout

3 XDP72x-001 evaluation platform

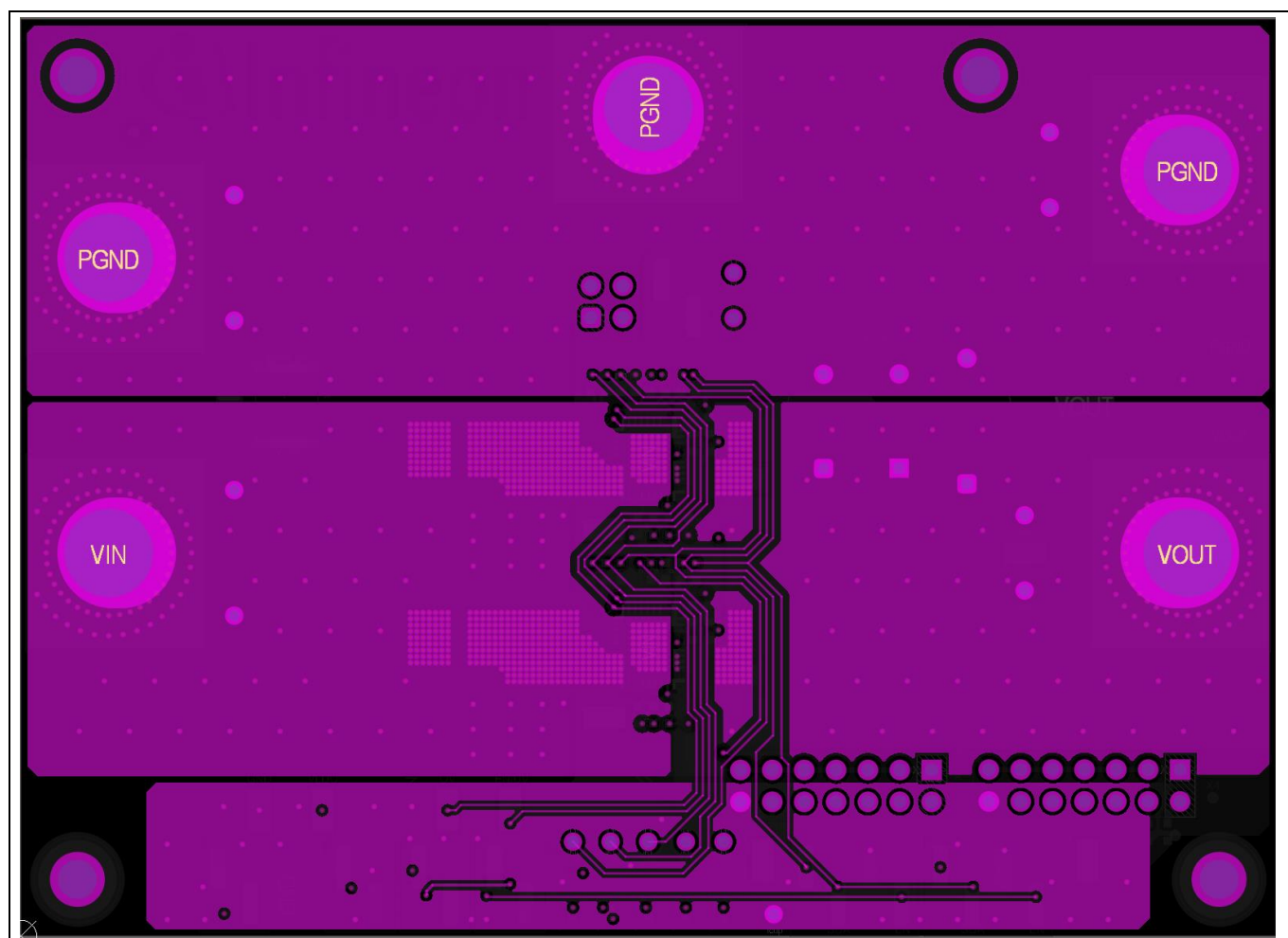


Figure 7 Mid 1 layer layout

3 XDP72x-001 evaluation platform

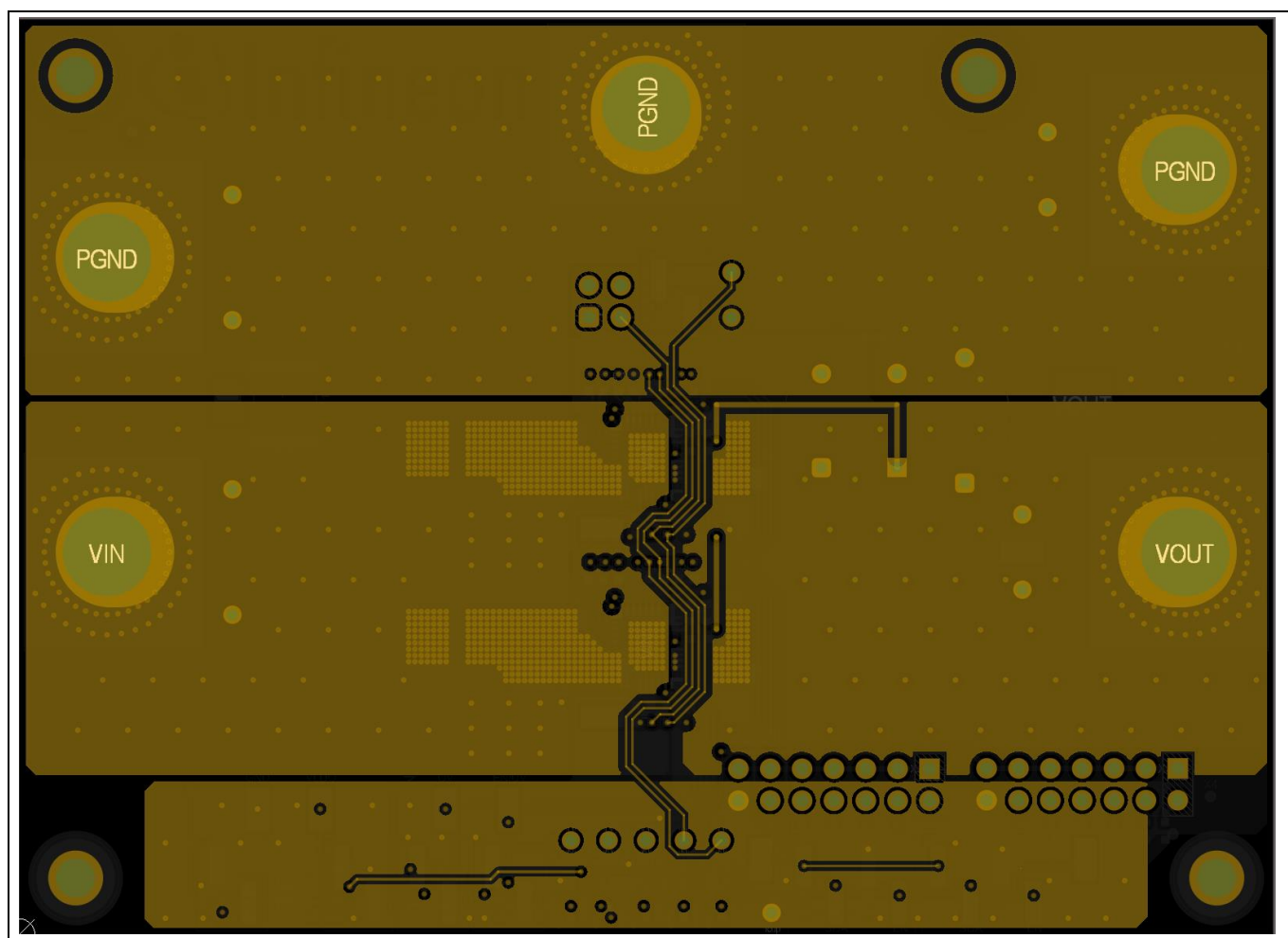


Figure 8 Mid 2 layer layout

3 XDP72x-001 evaluation platform

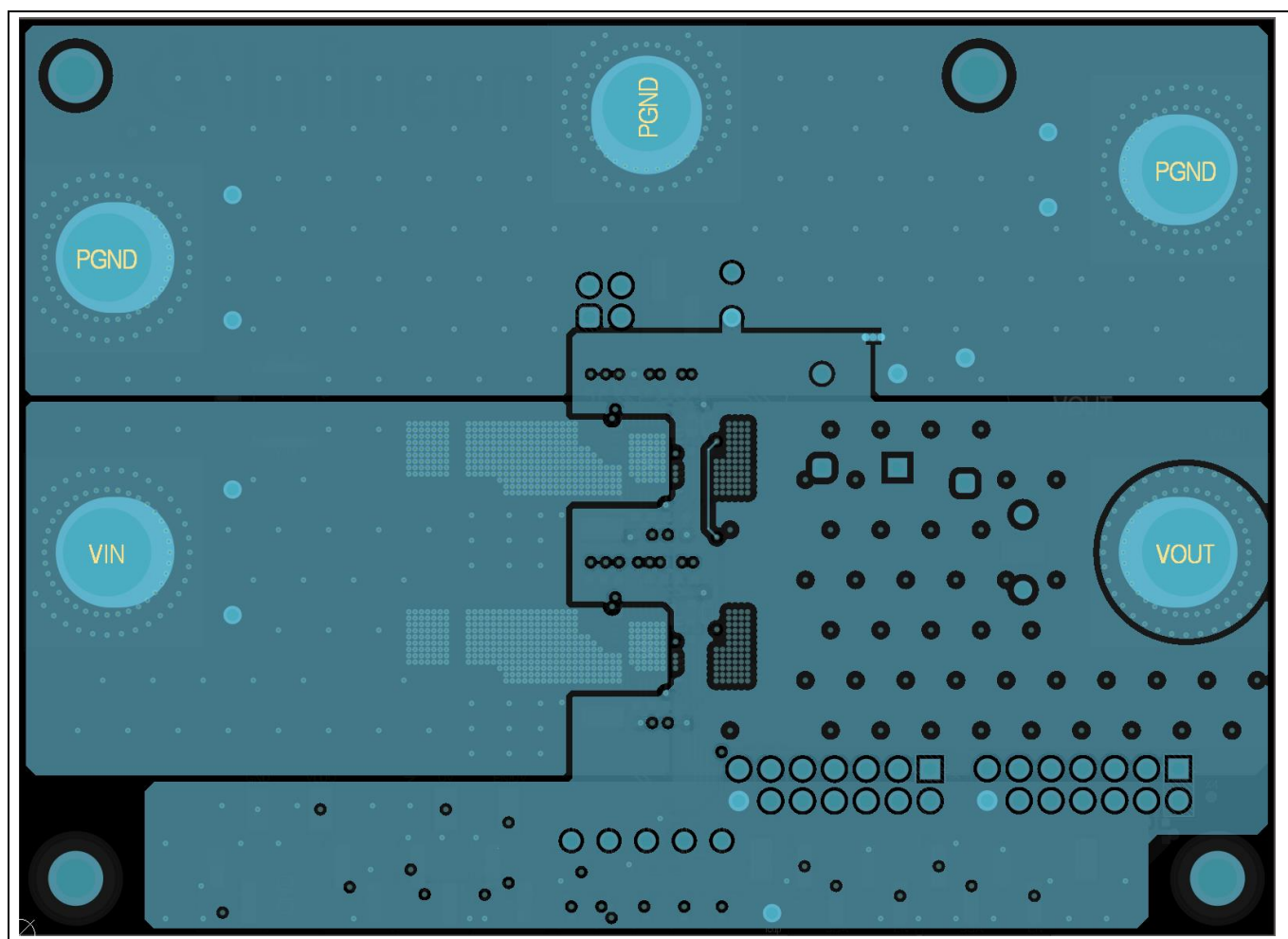


Figure 9 Mid 3 layer layout

3 XDP72x-001 evaluation platform

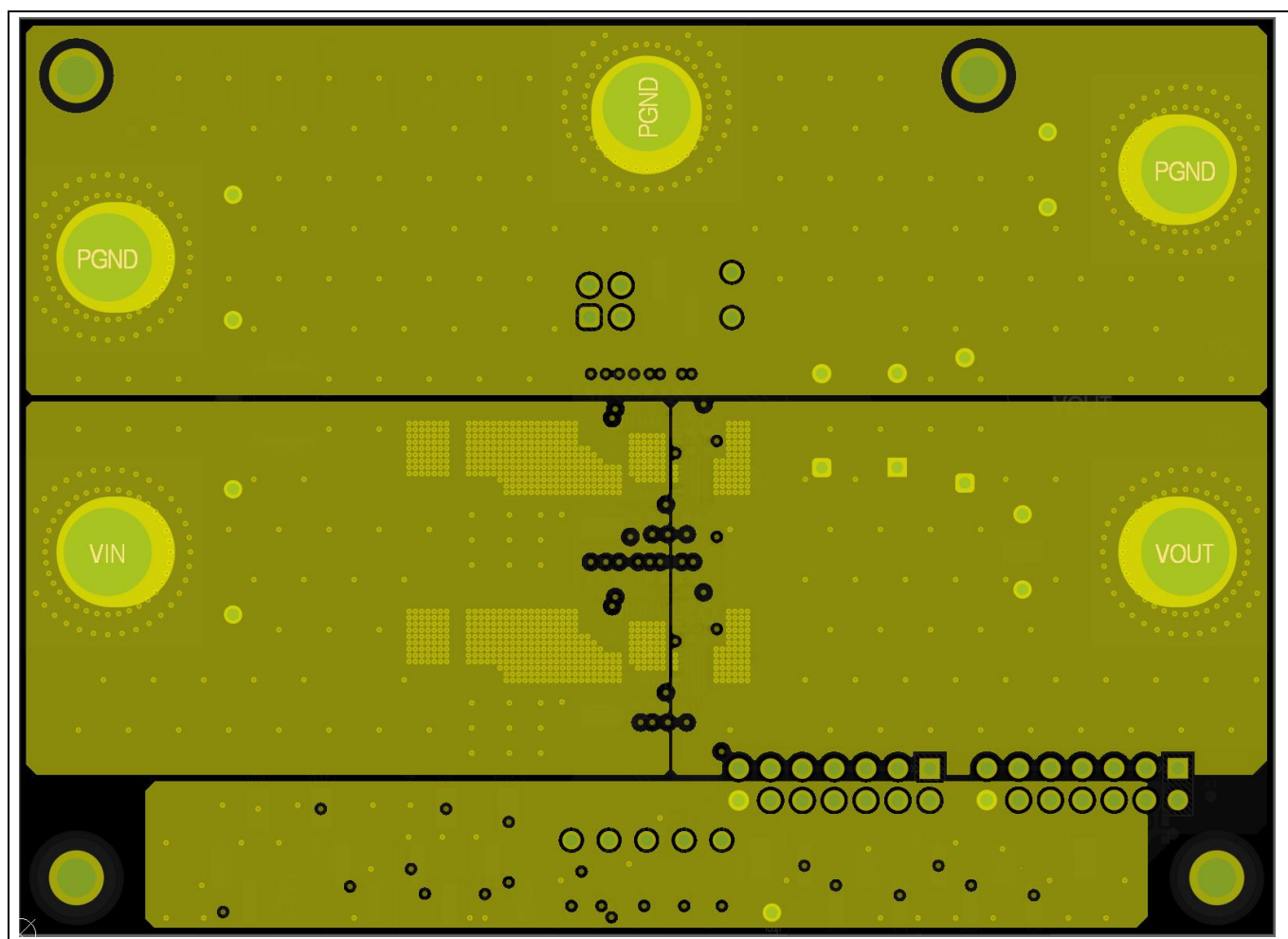


Figure 10 Mid 4 layer layout

3 XDP72x-001 evaluation platform

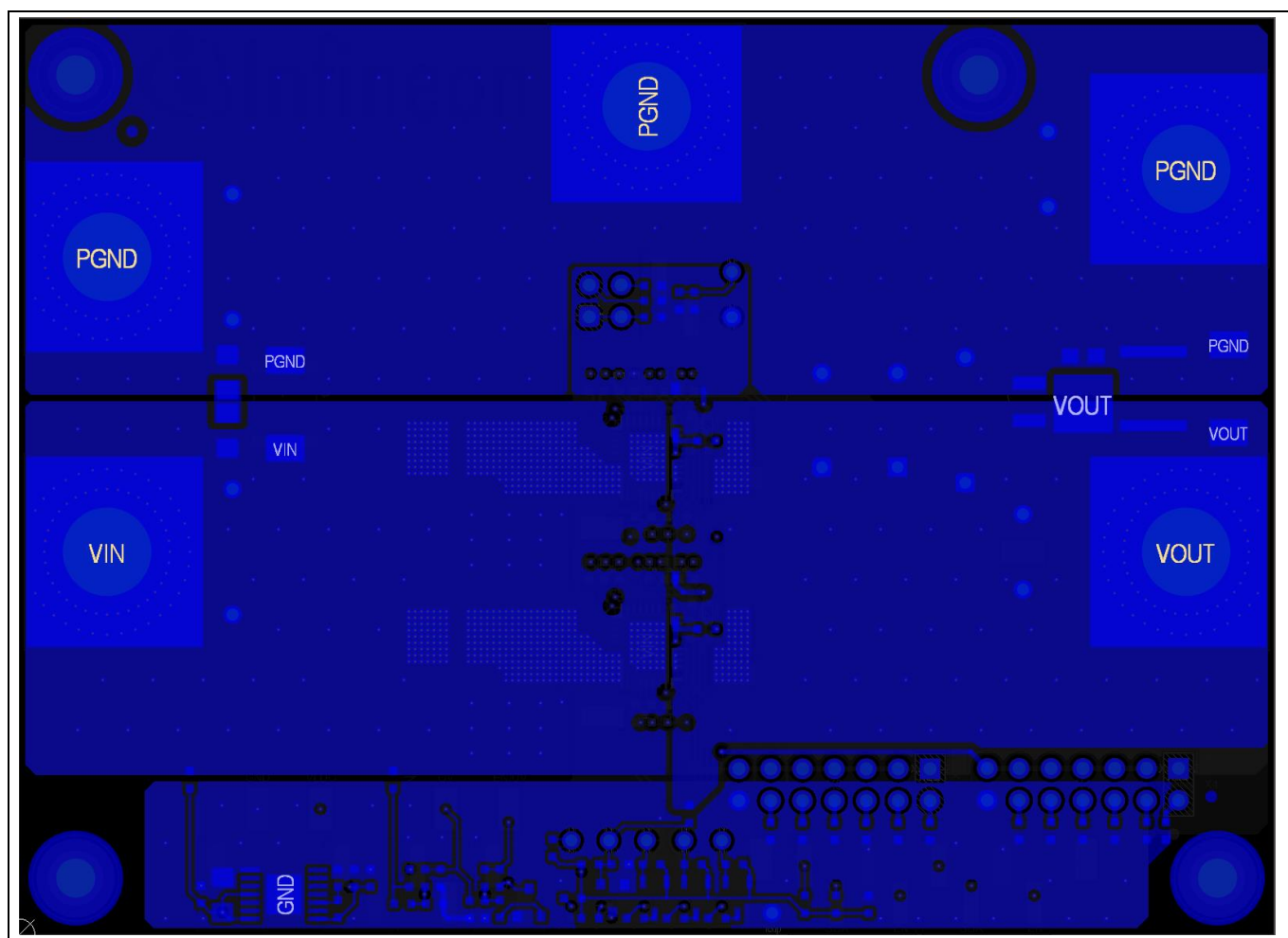


Figure 11 Bottom layer layout

3 XDP72x-001 evaluation platform

3.5 XDP72x-001 Evaluation Board bill of materials

Table 2 XDP72x-001 Evaluation Board bill of materials

Qty	Ref designator	Value	Footprint	Manufacturer	Part number
1	BRD1	PC Board (FAB)	–	–	P100219 B
1	C1	10uF	C1206	Murata	GRM31CD71H106 KE11L
2	C2, C7	0.1uF	C0603	TDK	C1608X7R1H104K 080AA
1	C6	3.3uF	C0603	TDK	C1608X5R1E335M 080AC
3	C8, C13, C14	1uF	C0603	TDK	C1608X7R1E105K 080AB
2	C10, C12	100nF	C0603	Yageo	CC0603KRX7R0BB 104
1	C16	1mF	CAPPRD750W80D 1800H4200B	Nichicon	UHW2A102MHD
1	C17	10uF	CAPC5750X250N	TDK Corporation	C5750X7S2A106K2 30KB
1	C18	1000pF	C0603	TDK	C1608X7R1H102M 080AE
2	D1, D5	Yellowish Green	LED-SMD-SMLP13BC8T	ROHM Semiconductors	SML-P11MTT86R
2	D2, D3	Red	LED-SMD-SMLP13BC8T	ROHM Semiconductors	SML-P11UTT86R
1	D4	Orange	LED-SMD-SMLP13BC8T	ROHM Semiconductors	SML-P11DTT86R
1	D6	5.0SMDJ64A	DIOM7959X262N	Bourns	5.0SMDJ64A
1	D10	STPS6M100SF	V10PL45-M3	STMicroelectronics	STPS6M100SF
1	D11	B3100-13-F	DIOM7959X250N	Diodes Incorporated	B3100-13-F
4	J1, J3, J4, J10	TSM-102-01-S-SV, N/U	CON-M-SMD-TSM-102-01-S-SV	Samtec	TSM-102-01-S-SV
2	J5, J6	TSM-104-01-L-SV-P	CON-M-SMD-TSM-104-01-L-SV-P	Samtec	TSM-104-01-L-SV-P
2	Q1, Q2	2N7002	INF-PG-SOT23_N-0	Infineon Technologies	2N7002
3	Q3, Q4, Q5	BSR315P	SOT95P285X135-3N	Infineon Technologies	BSR315P
8	R1, R4, R7, R14, R20, R25, R26, R27	4.7K	R0603	Panasonic	ERJ-3EKF4701V
5	R3, R8, R9, R15, R19	20K	R0603	Panasonic	ERJ-3EKF2002V
1	R10	147K	R0603	Panasonic	ERJ-3EKF1473V

3 XDP72x-001 evaluation platform

Qty	Ref designator	Value	Footprint	Manufacturer	Part number
1	R11	2.4K	R0603	Panasonic	ERJ-3EKF2401V
1	R37	12.4K	R0603	Panasonic	ERJ-3EKF1242V
2	R12, R67	24.9K	R0603	Panasonic	ERJ-3EKF2492V
1	R13	2.8K	R0603	Panasonic	ERJ-3EKF2801V
18	R18, R22, R33, R41, R42, R43, R49, R68, R69, R71, R72, R73, R74, R75, R76, R77, R78, R79	0	R0603	Panasonic	ERJ-3GEY0R00V
2	R35, R36	100	R0603	Panasonic	ERJ-3EKF1000V
1	R38	19.6K	R0603	Vishay	CRCW060319K6FK EA
1	R39	9.76K	R0603	Panasonic	ERJ-3EKF9761V
1	R40	15K	R0603	Panasonic	ERJ-3EKF1502V
1	R45	11K	R0603	Panasonic	ERJ-3EKF1102V
2	R44, R50	7.5K	R0603	Panasonic	ERJ-3EKF7501V
1	R46	5.49K	R0603	Panasonic	ERJ-3EKF5491V
1	R52	4.53K	R0603	Panasonic	ERJ-3EKF4531V
1	R51	3.74K	R0603	Panasonic	ERJ-3EKF3741V
1	R53	2.32K	R0603	Panasonic	ERJ-3EKF2321V
1	R89	121k	RESC3225X60N	Vishay	CRCW1210121KFK
1	R90	40.2K	R0603	Panasonic	ERJ-3EKF4022V
1	R91	1.37K	R0603	Panasonic	ERA-3AEB1371V
1	R92	2.74K	R0603	Panasonic	ERA-3AEB2741V
4	S1, S2, S3, S4	Standoff 4-40x1/2	mtg_hole_125	Keystone	2203
4	S1a, S2a, S3a, S4a	Screw 4-40 x 1/4		Keystone	9900
16	TP1, TP2, TP3, TP4, TP5, TP9, TP14, TP15, TP16, TP17, TP27, TP28, TP29, TP30, TP32, TP33	loop	TP_5020_loop	Keystone	5020
13	TP6, TP7, TP8, TP10, TP11, TP12, TP13, TP18, TP19, TP20, TP24, TP25, TP31	5015	CON-SMD-TP-5015	Keystone Electronics Corp.	5015
1	U1	TLS835B2ELVSE	SOP65P600X170-15N	Infineon Technologies	TLS835B2ELVSEX UMA1
1	U2	XDP720-001	PG-VQFN-23-1	Infineon Technologies	XDP720-001
1	U3	XDP721-001	PG-VQFN-23-1	Infineon Technologies	XDP721-001

XDP™ XDP72x-001 evaluation PCBA user guide

3 XDP72x-001 evaluation platform

Qty	Ref designator	Value	Footprint	Manufacturer	Part number
5	X1, X2, X6, X7, X8	NUT 8-32	Screw & Nut for JACK1	Penn Eng	KF2-832-ET
2	X3, X4	CON14	CON-M-THT-HTSW-107-07-L-D	Samtec	HTSW-107-07-L-D
3	XJ3-1-2, XJ4-1-2, XJ5-1-2	–	Jumper_SPC02SY AN	Sullins	SPC02SYAN
1	X5	HTSW-102-07-L-D	CON-M-THT-HTSW-102-07-L-D	Samtec	HTSW-102-07-L-D

3.6 USB0010 dongle schematics

Figure 12 shows the schematic for the USB0010 dongle used to connect the evaluation board to the Infineon XDP™ Designer GUI using PMBus®.

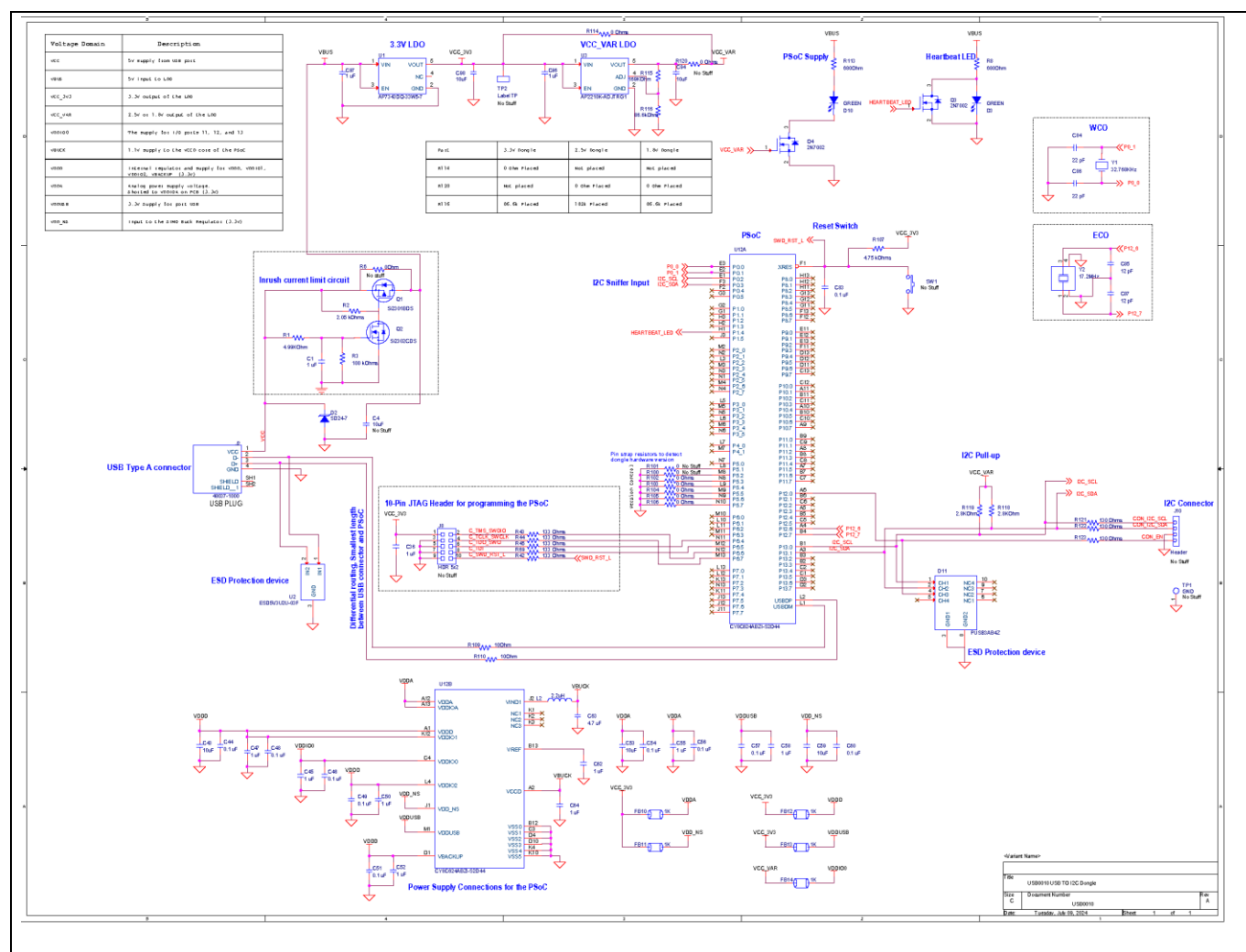


Figure 12 USB0010 dongle schematics

4 Programming, setup, and turn-on instructions

4 Programming, setup, and turn-on instructions

Set up the system as follows:

1. Connect the USB0010 dongle to the XDP72x-001 Evaluation Board as shown in [Figure 13](#)
2. Connect the USB0010 dongle to a PC USB port
3. Ensure that the jumpers are connected properly
4. Connect 40 V to 60 V, 48 V typical from VIN to the PGND on the left side of the board

XDP72x-001 powers up as soon as VIN is equal to or greater than 7 V. At this point, communication and programming is possible, but the integrated FET will be off. To turn on the integrated FET, a minimum of 9 V is required.

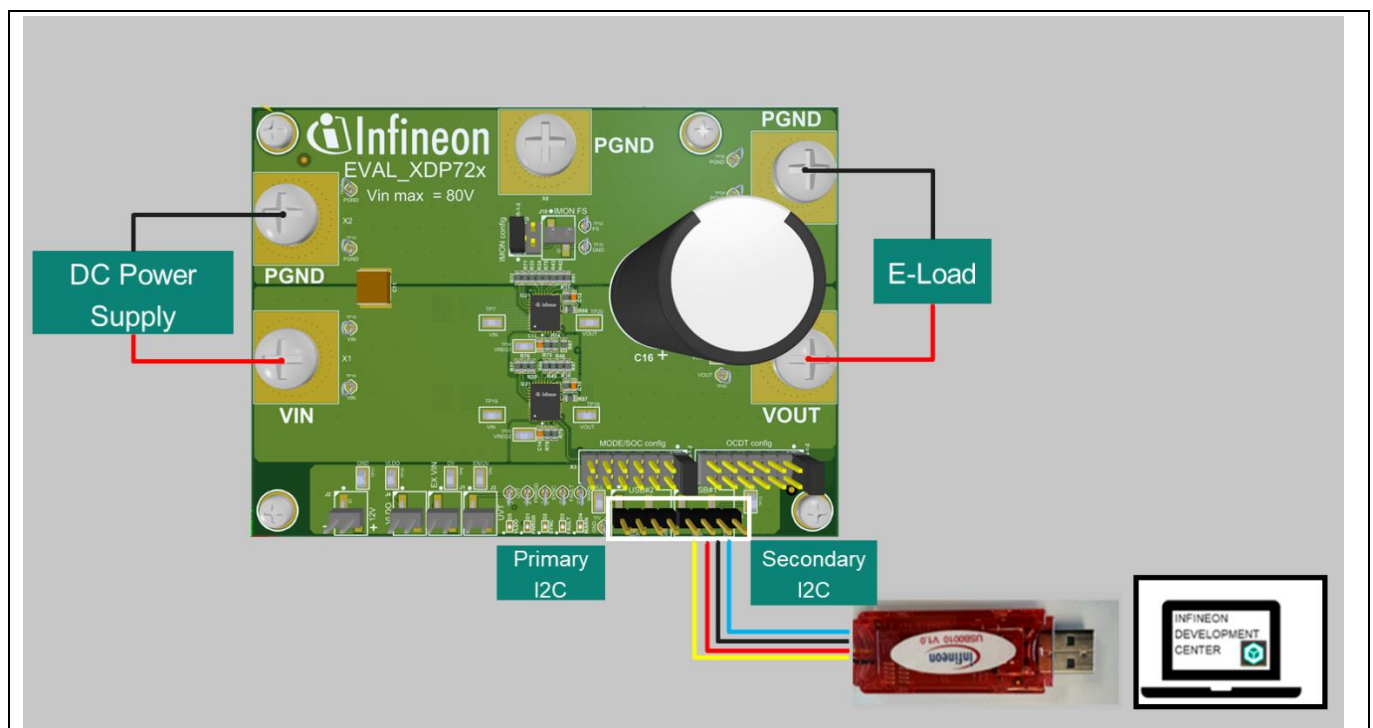


Figure 13 XDP72x-001 Evaluation Board and dongle setup

4.1 XDP™ Designer communication setup

Install the XDP™ Designer software from the [Infineon Development Center](#).

The following sections explain how to configure and test the evaluation board and dongle using the XDP™ Designer software.

4.1.1 Dongle connection in XDP™ Designer

1. Open the XDP™ Designer GUI
2. Wait for a few seconds and check the bottom status bar for the dongle connection
If the highlighted area, as shown in [Figure 14](#), displays **USB010**, the dongle has been successfully detected by the GUI

4 Programming, setup, and turn-on instructions

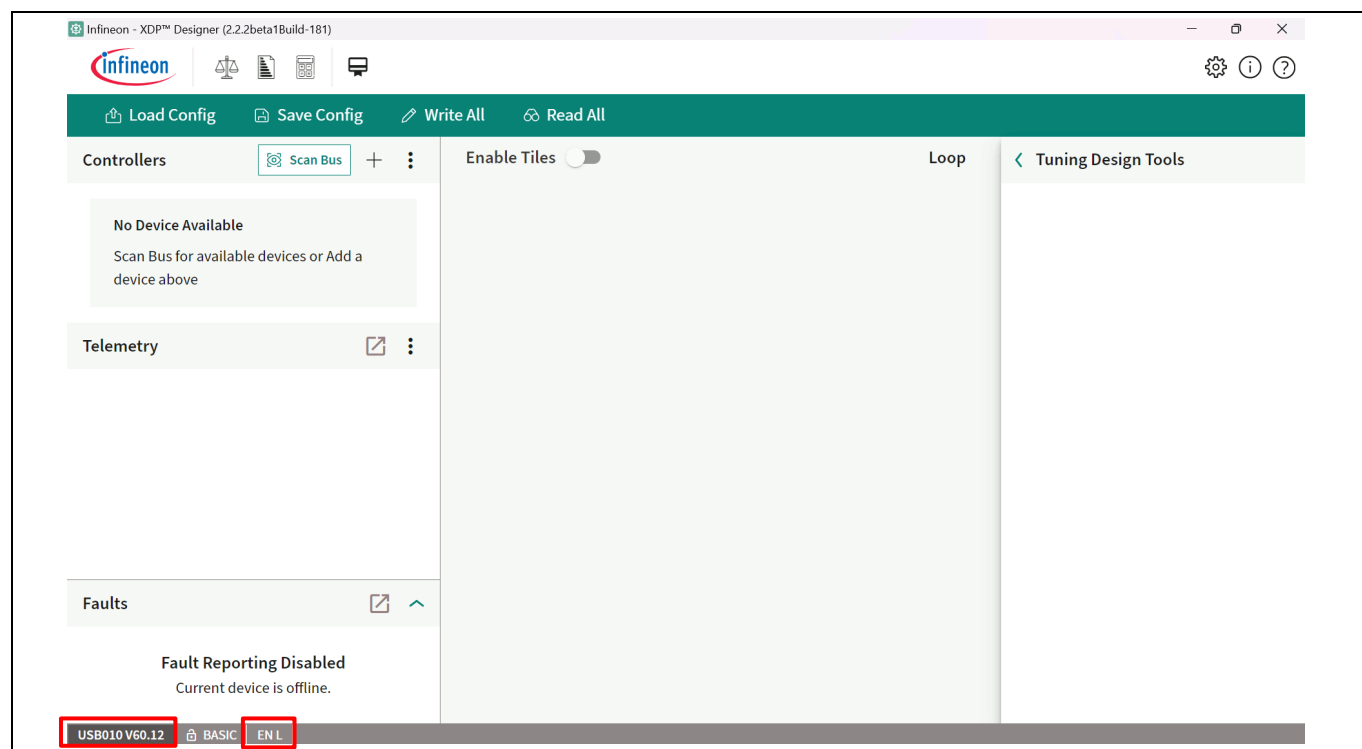


Figure 14 USB0010 detection on XDP™ Designer

4.1.2 Detecting XDP720-001

1. Click Scan Bus, as shown in [Figure 15](#)
2. Wait for a few seconds for the device to be detected by the GUI automatically. If the device is not detected automatically, click **Scan Bus** again

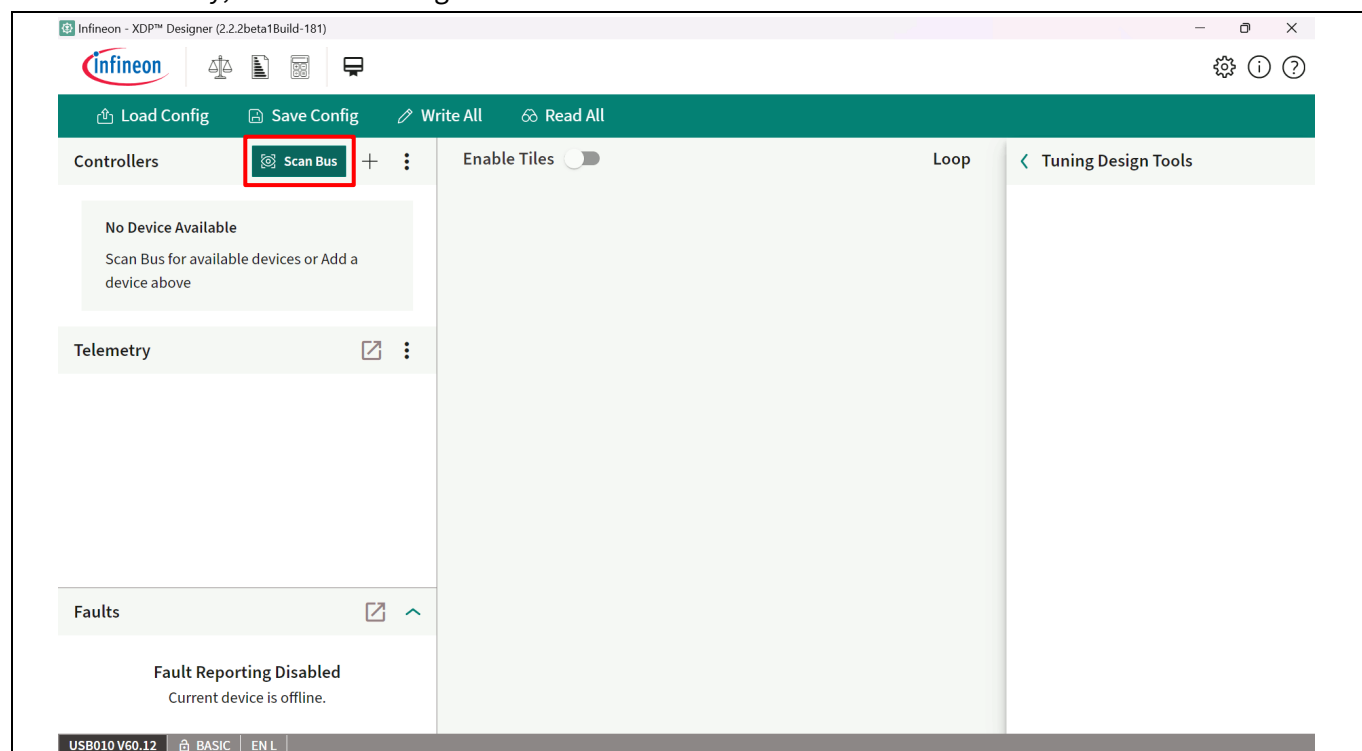


Figure 15 XDP720-001 detection

4 Programming, setup, and turn-on instructions

The detected device is XDP720-001, with the **Telemetry** displayed on the left as shown below:

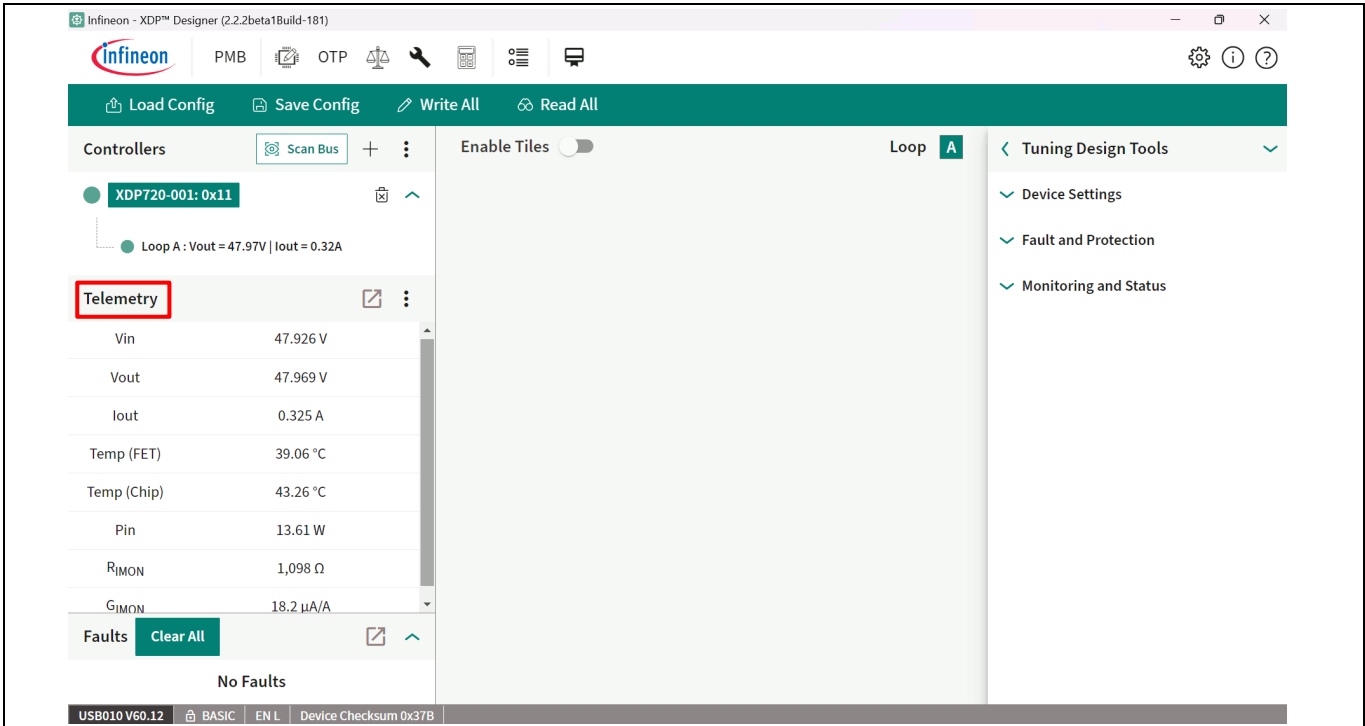


Figure 16 Live telemetry of the connected XDP720-001

3. Click **PMB** to view the PMBus® registers and the values stored in them

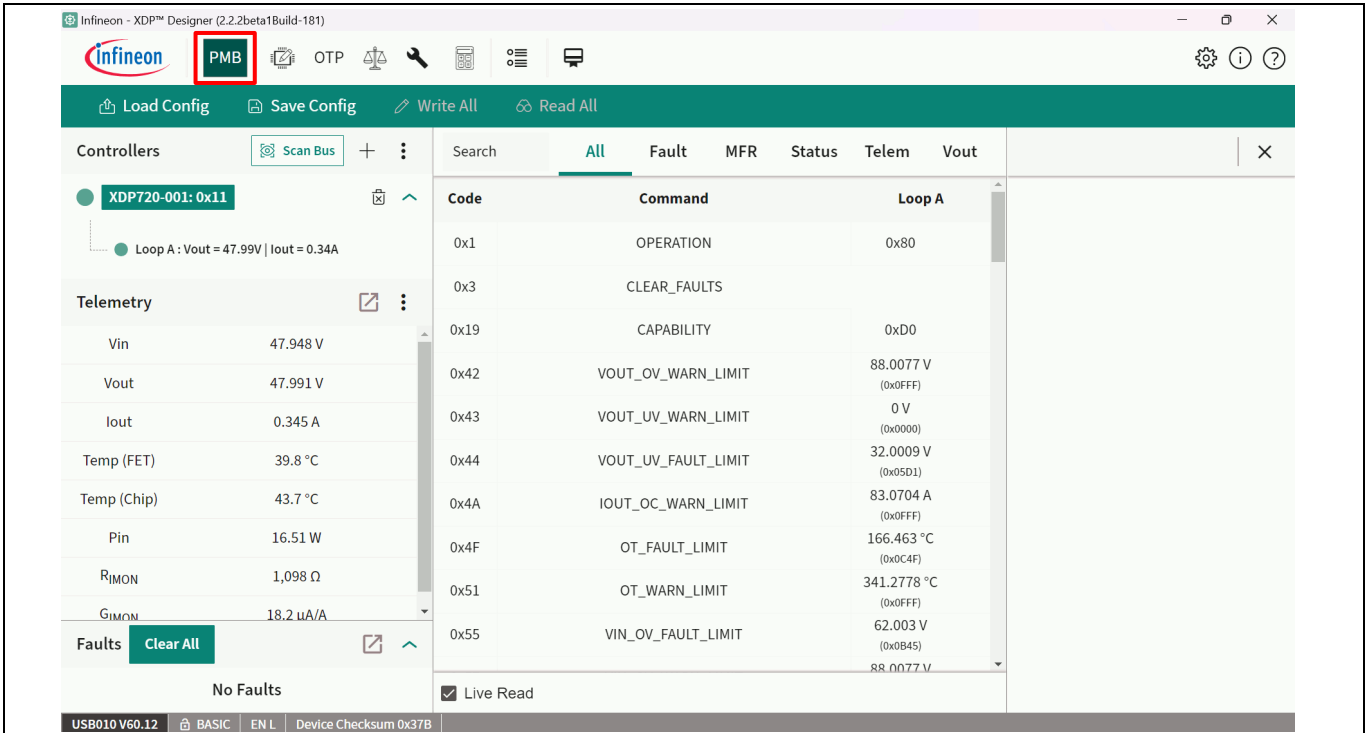


Figure 17 XDP™ Designer displaying all the PMBus® registers of the connected XDP720-001

4 Programming, setup, and turn-on instructions

4.1.3 Reading and writing registers

1. To edit a register individually, click on the corresponding PMBus® register, make the necessary changes, and then click **Write**

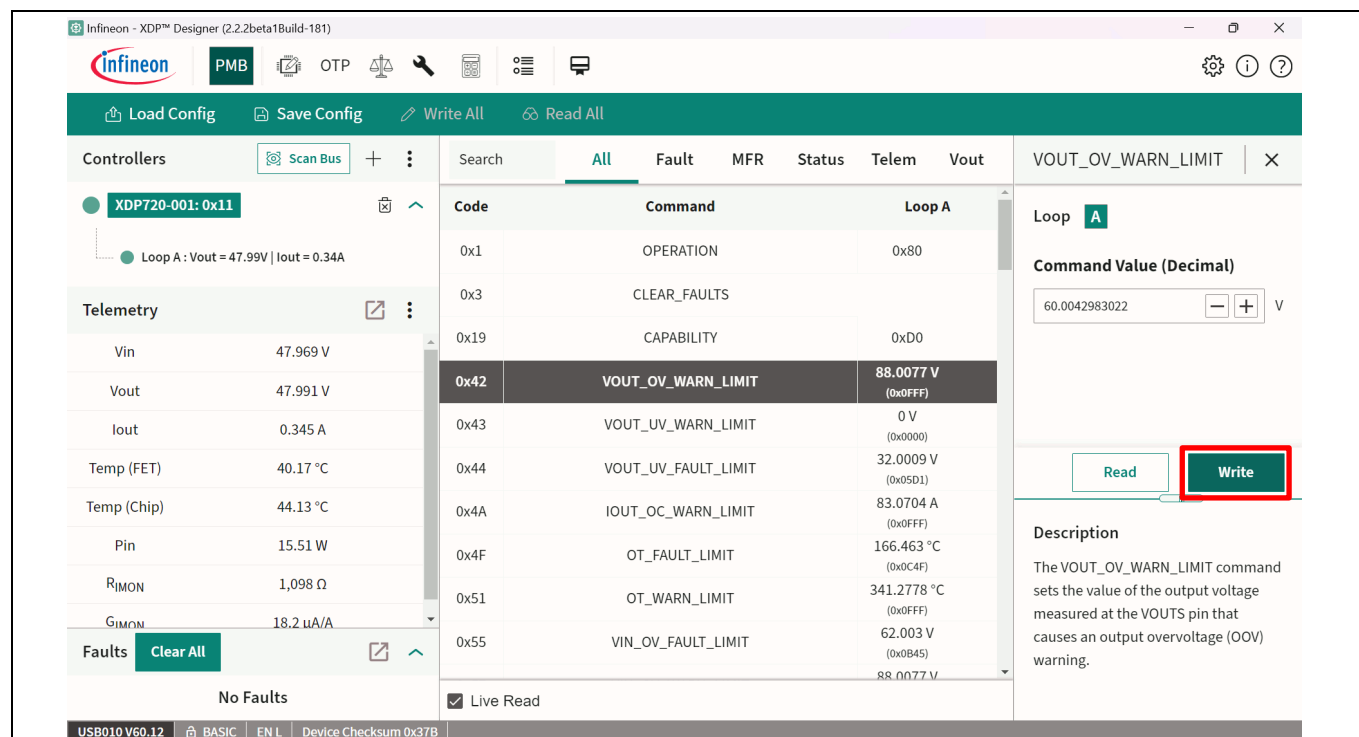


Figure 18 Editing VOUT_OV_WARN_LIMIT

2. Most of the registers are updated automatically. Click **Read** to read the corresponding register values

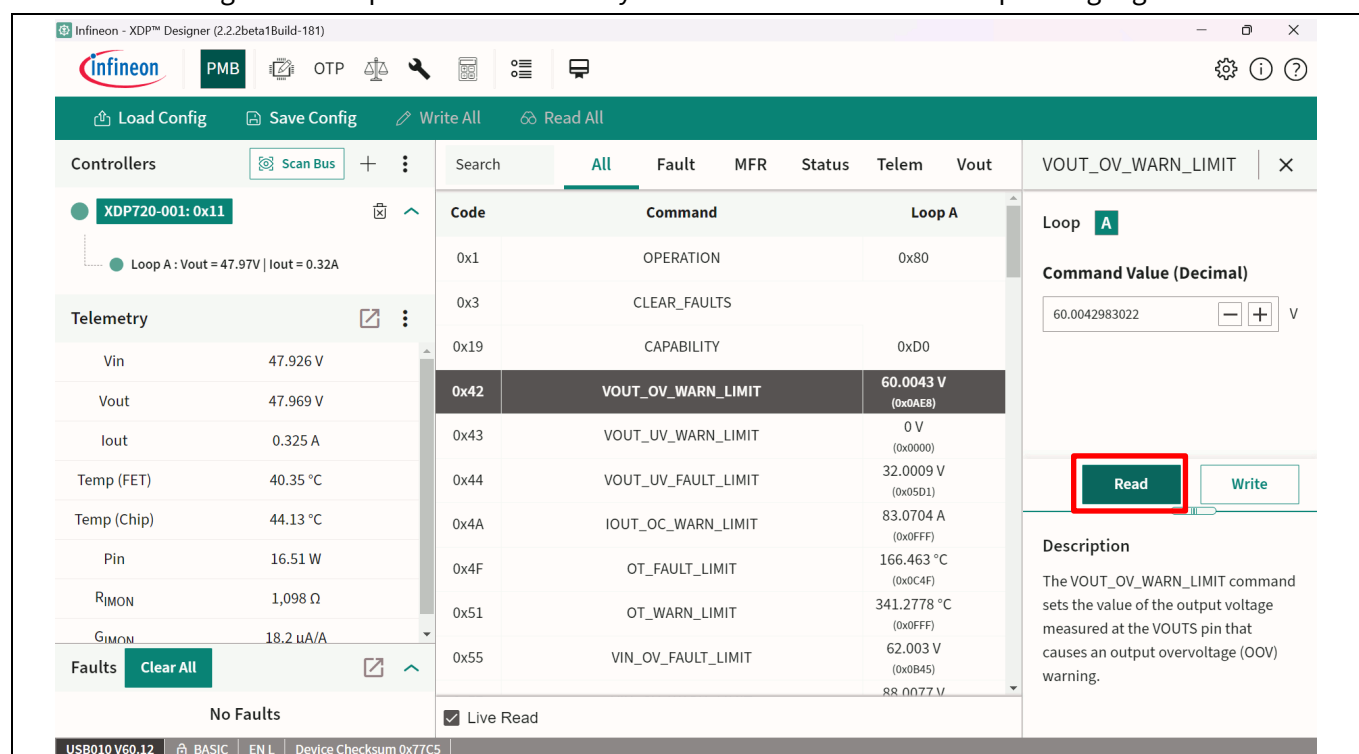


Figure 19 Reading VOUT_OV_WARN_LIMIT

4 Programming, setup, and turn-on instructions

4.1.4 Programming the IMON resistor value

1. Click PMB one more time
2. Select the System Current Fault under Tuning Design Tools on the right
3. Modify the R_{IMON} value to 1370 Ω and then click **Set**. See [Figure 20](#)

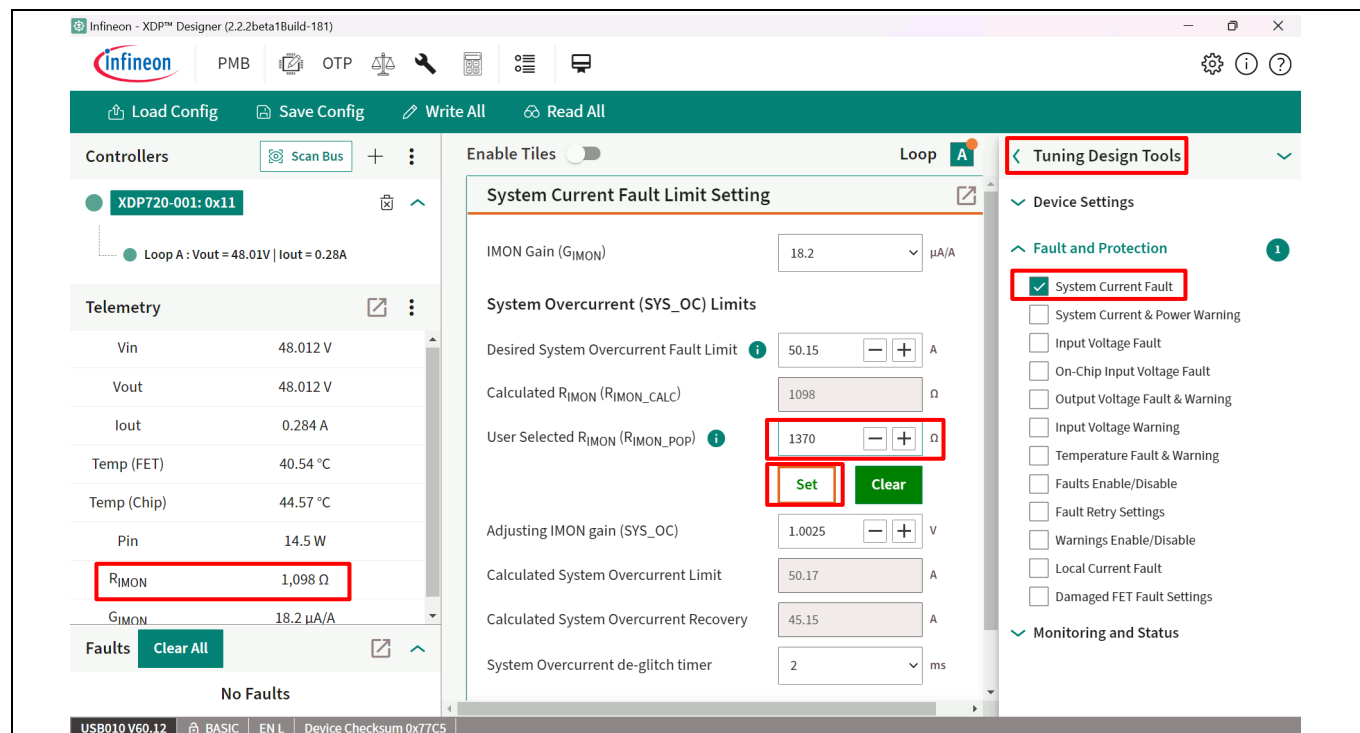


Figure 20 Program IMON resistor value

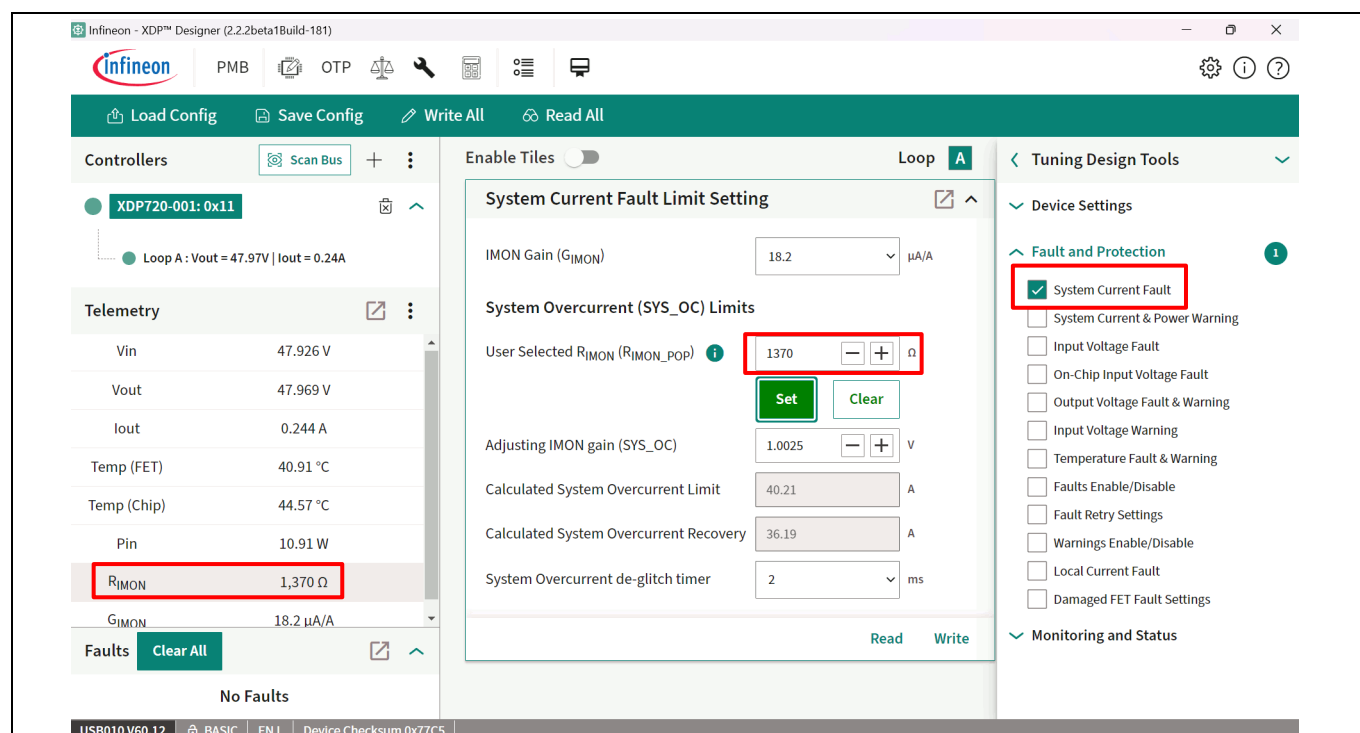


Figure 21 Program IMON resistor value done

4 Programming, setup, and turn-on instructions

4.2 Loading the configuration file

This section describes how to load the configuration file directly into the device, which eliminates the need to manually modify the required register. Do the following to load the configuration file into the device:

1. Click **Load Config**, as shown in [Figure 22](#)

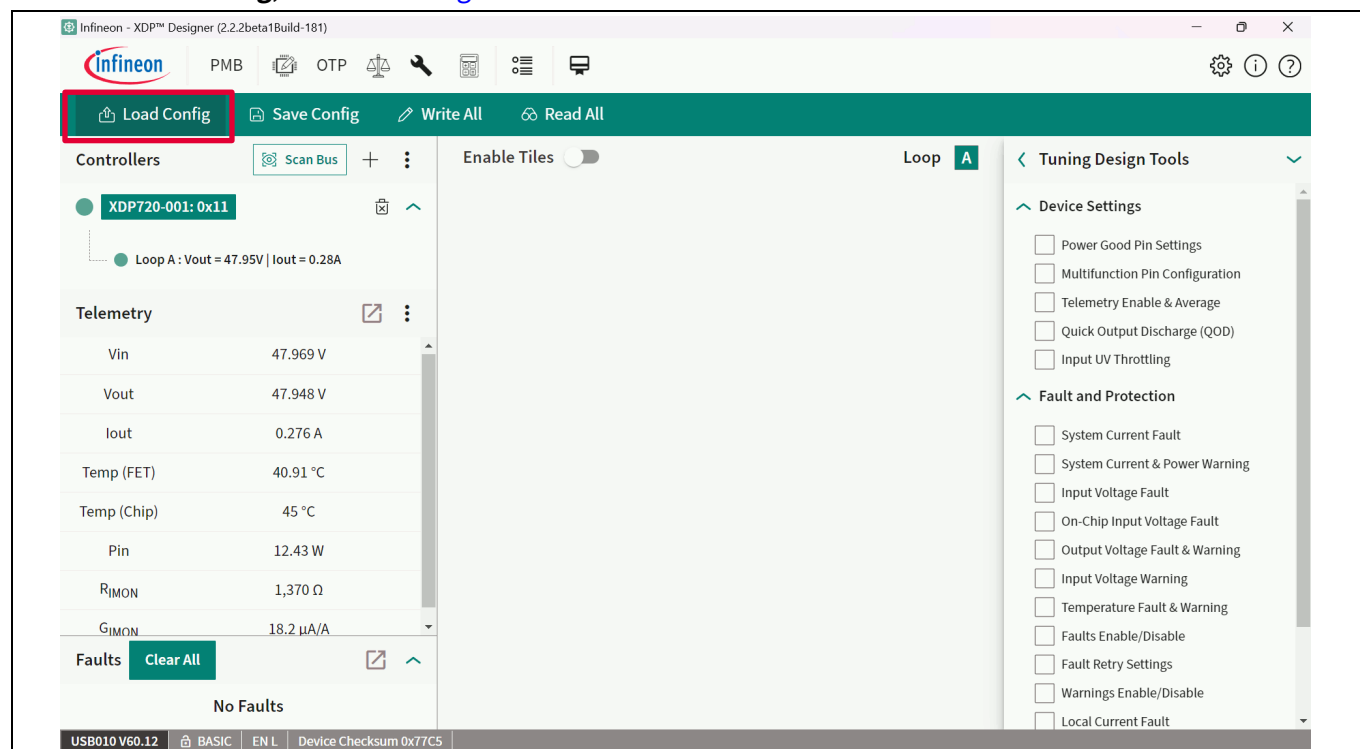


Figure 22 Select Load Config option

2. Click **Browse** and select the .xdp file that needs to be loaded onto the device, as shown in [Figure 23](#)

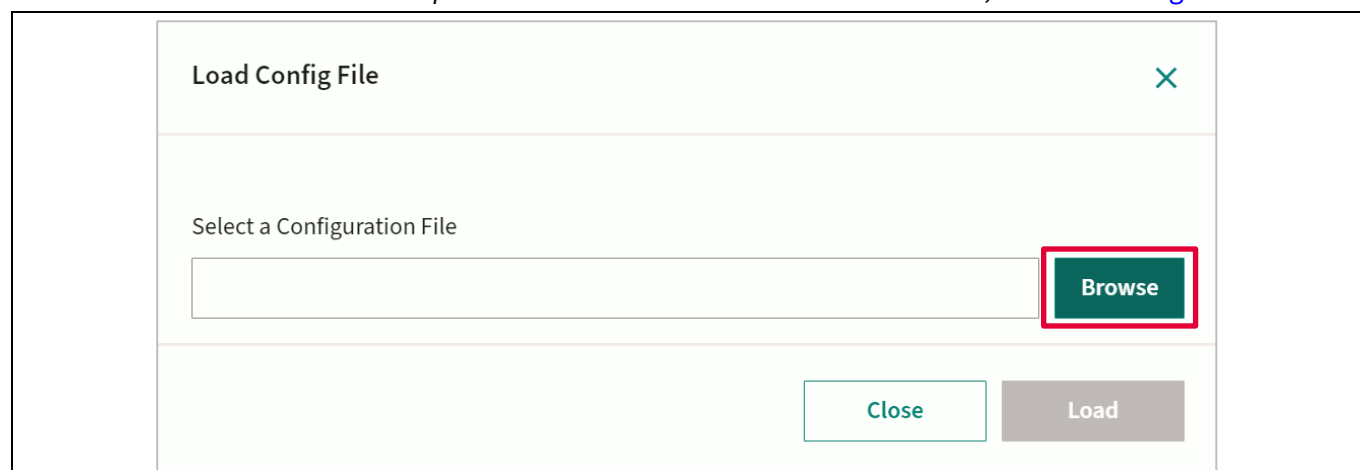


Figure 23 Browse to select the necessary configuration file

4 Programming, setup, and turn-on instructions

3. Click **Load** to load the necessary configuration onto the device, as shown in [Figure 24](#)

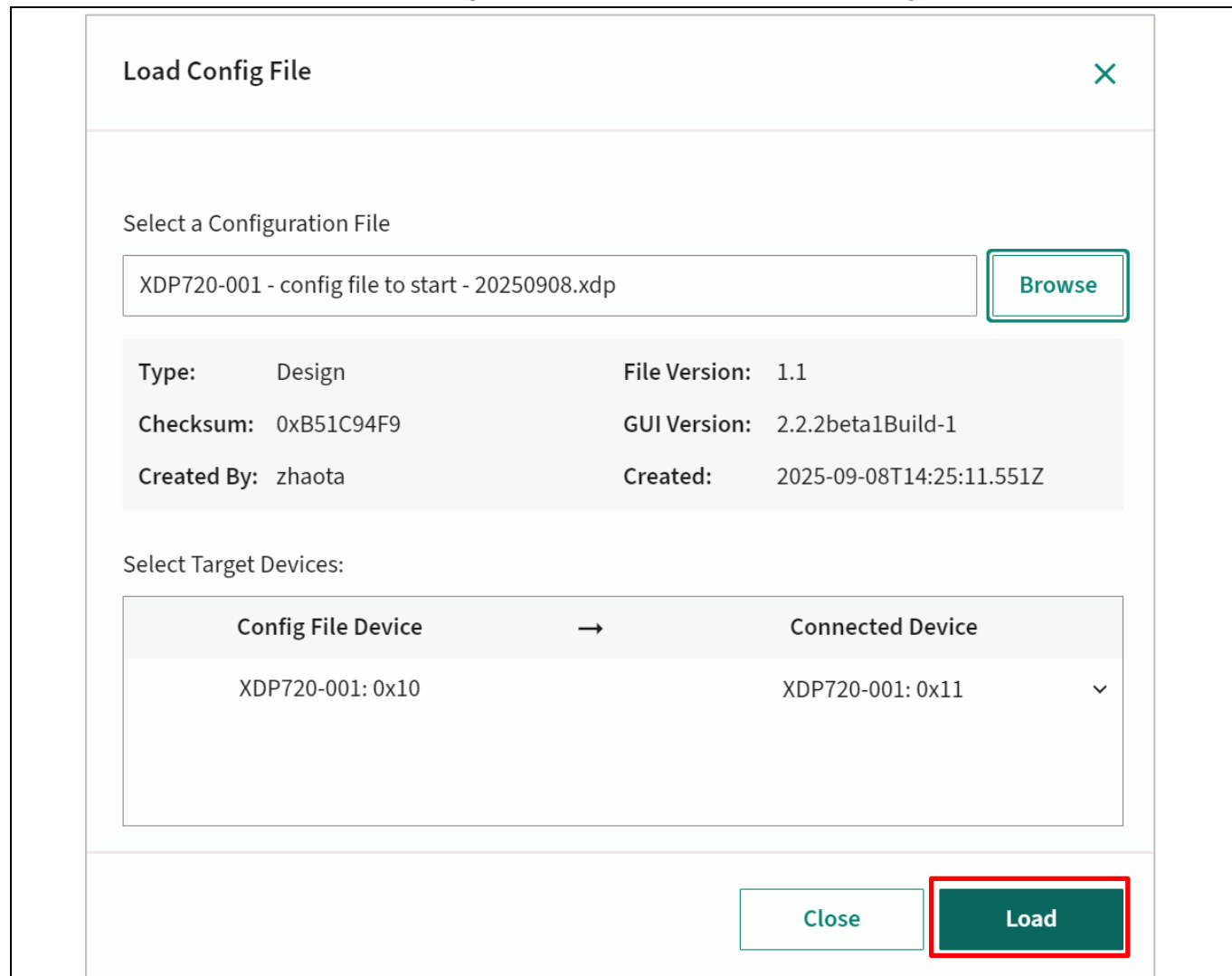


Figure 24 Load the selected configuration file

5 Programming OTP

5 Programming OTP

As specified in the XDP72x-001 datasheet [1], to program the desired settings in internal commands or OTP at power-up, follow these steps:

1. Apply a voltage at the VDD_VIN:
 - At least 9 V to program commands into volatile memory
 - At least 20 V to program OTP
2. Keep the UV/EN pin at chip GND potential
 - Communication via PMBus® is possible as soon as STANDBY state is entered. At this point, commands and OTP can be programmed
3. To ensure successful programming, ensure that the internal temperature of the device stays below 125°C

To program the OTP section:

1. Program the commands in volatile memory as required
2. Click the button highlighted as shown in [Figure 25](#)

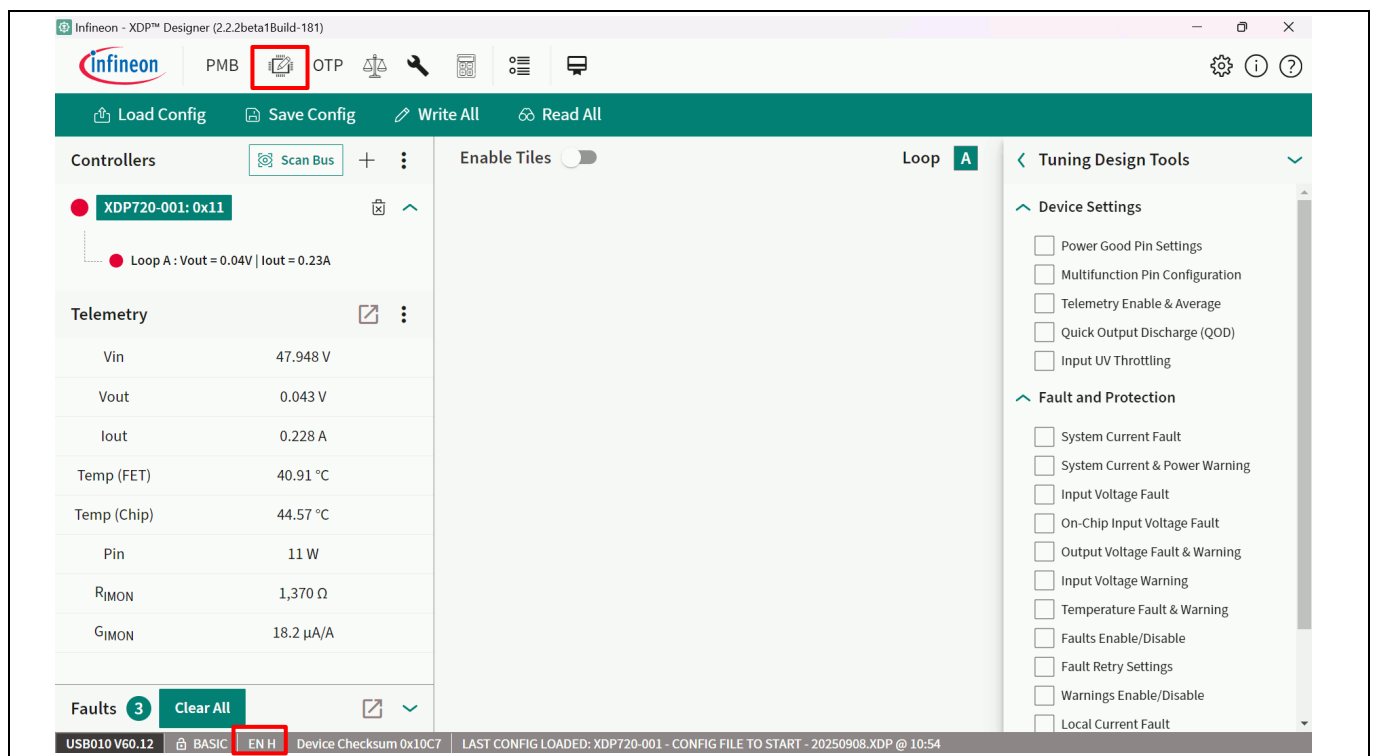
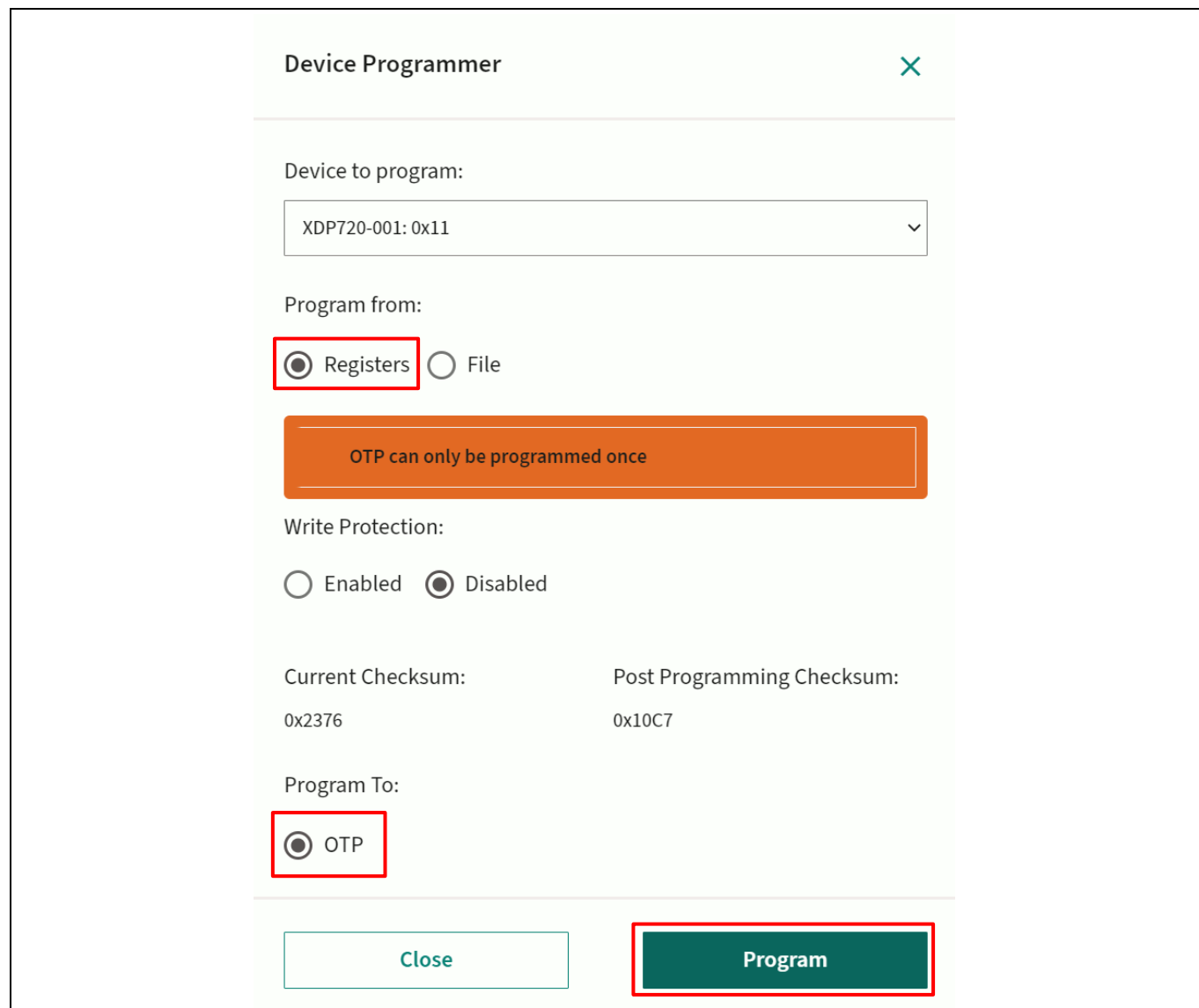


Figure 25 Programming tab

5 Programming OTP

- Set the program from **Registers**, select the memory section Program To **OTP** that needs to be programmed and then click **Program**, as shown in [Figure 26](#)



The screenshot shows the 'Device Programmer' window with the following configuration:

- Device to program:** XDP720-001: 0x11
- Program from:** ☒ Registers ☐ File
- OTP can only be programmed once** (warning message)
- Write Protection:** ☐ Enabled ☒ Disabled
- Current Checksum:** 0x2376
- Post Programming Checksum:** 0x10C7
- Program To:** ☒ OTP
- Buttons:** Close and Program (highlighted with a red box)

Figure 26 OTP programming

The command configuration will be automatically copied to the selected memory section.

6 Board features

6 Board features

6.1 Overcurrent deglitch (OCDT)

The board's overcurrent deglitch (OCDT) time is user-selectable via the 14-pin configuration header X4. Install one 2-pin jumper across a pin pair to route a specific timing resistor to the protection IC's timing pin; this sets how long the controller waits after an overcurrent condition is detected before declaring a fault. See the IC datasheet for the timing equation and tolerances.

Note: Always power down the board before changing the jumper.

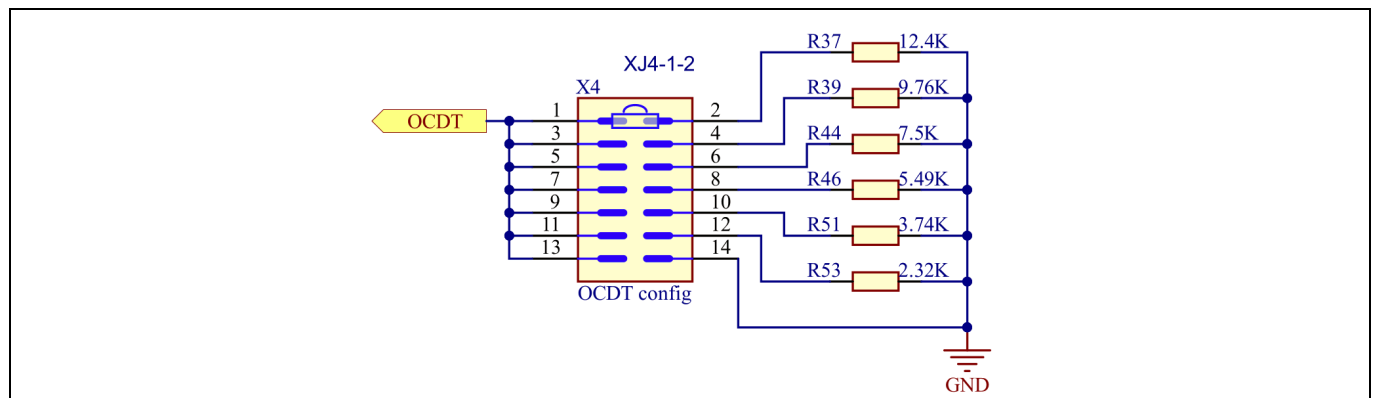


Figure 27 OCDT

6.2 MODE_SOC

This connector configures the “Mode” and “severe overcurrent” (SOC) trip point. When the measured current exceeds the selected SOC threshold, the controller turns the output off immediately (no deglitch/blanking by default).

The 14-pin header presents a set of discrete options that program MODE_SOC by choosing the desirable resistor. The first six pins of the header are used to set the device to “Primary” mode and the rest of them are used to set the IC to “Secondary” mode. The effective current threshold is determined by the SOC sense voltage setting and the current sense element. See the IC datasheet for the timing equation and tolerances.

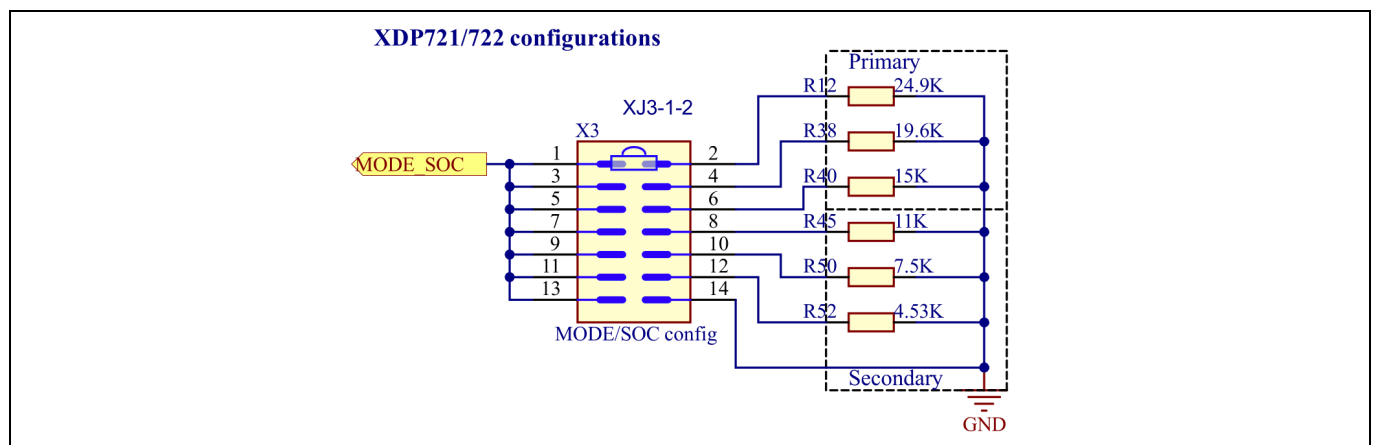


Figure 28 MODE_SOC

6 Board features

6.3 I²C connections

The board provides two independent 4-pin I²C headers. This connector is for: SCL (clock), SDA (data), EN (enable), and GND (ground). SCL and SDA are open-drain signals and require pull-up resistors to the onboard I/O supply (VLDO).

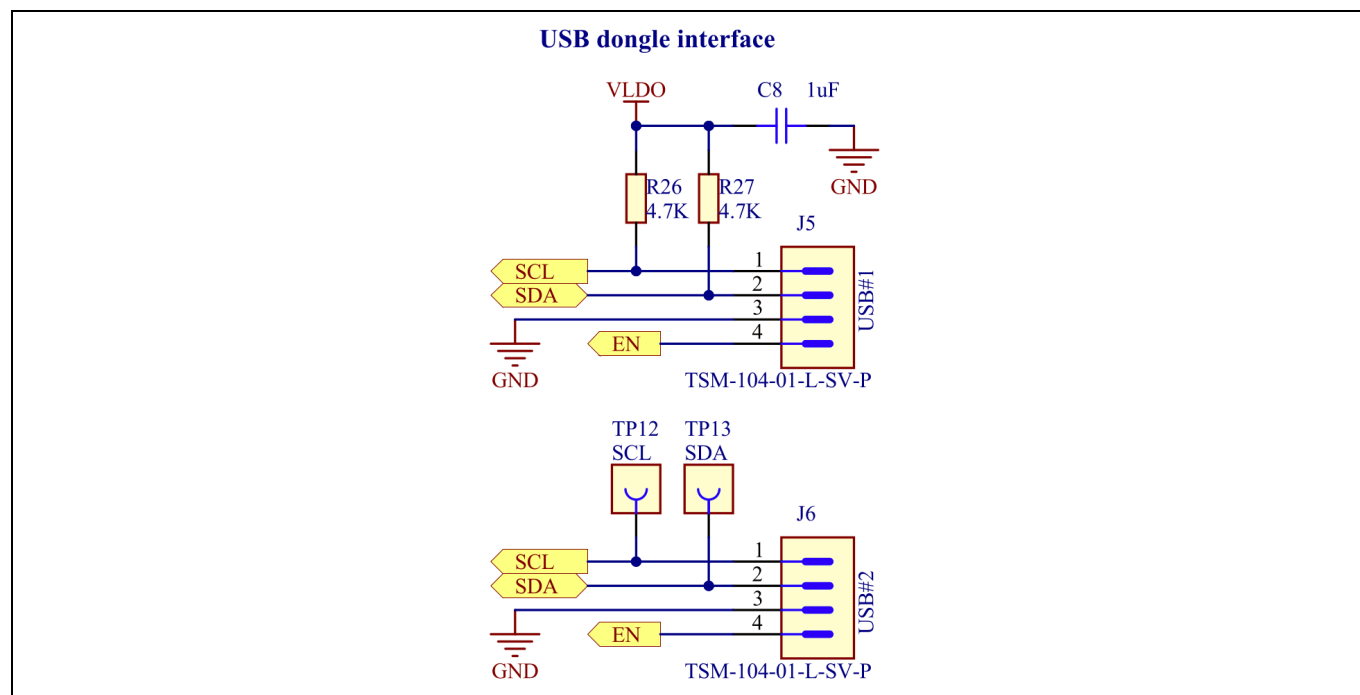


Figure 29 I²C connections

6.4 External power supply

VLDO is generated by an onboard LDO regulator from one of two inputs:

- **VIN to 3.3 V:** When VIN is the active source, the LDO regulates VIN down to 3.3 V
- **12 V input header to 3.3 V or 5 V:** When the 12 V header is the active source, the LDO regulates down to 3.3 V, selectable by a jumper resistor R22 (3.3 V) and R21 (5 V)

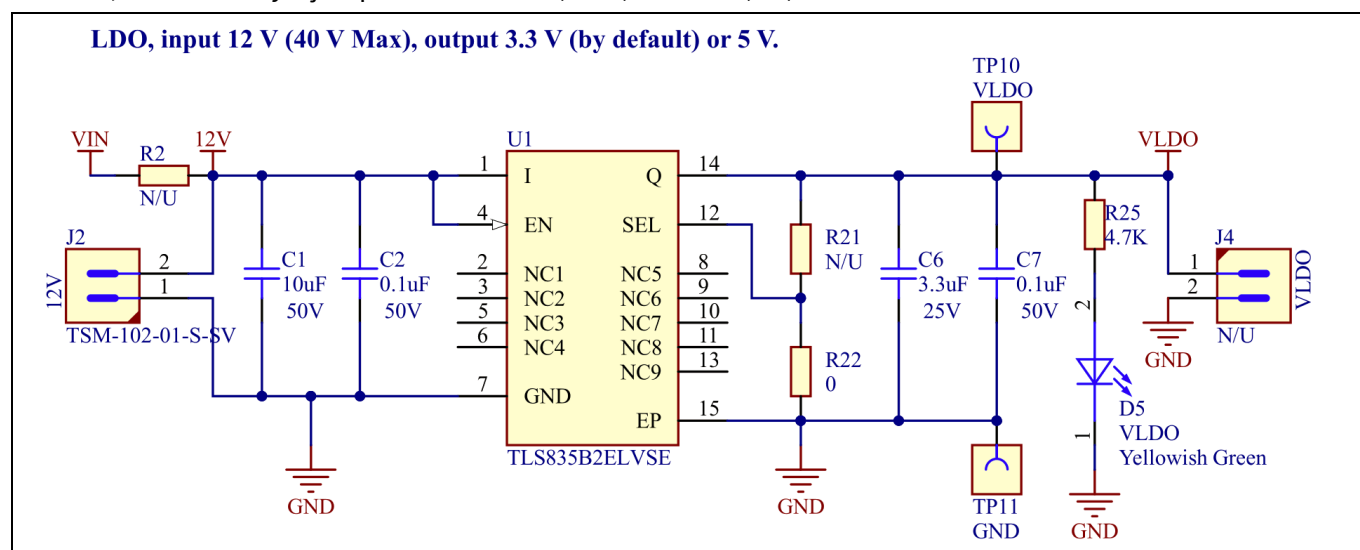


Figure 30 LDO and external power supply

6 Board features

6.5 IMON and fail-safe

The header X5 is used to choose and set the IMON resistor value which sets the system “Overcurrent” level. The IMON voltage can be measured using the J10 pin. The “fail-safe” resistor R90 is present to make sure that Primary of the board is functioning by showing minimum of V_{FS_TH} voltage (0.3 V typical) across the FS pin.

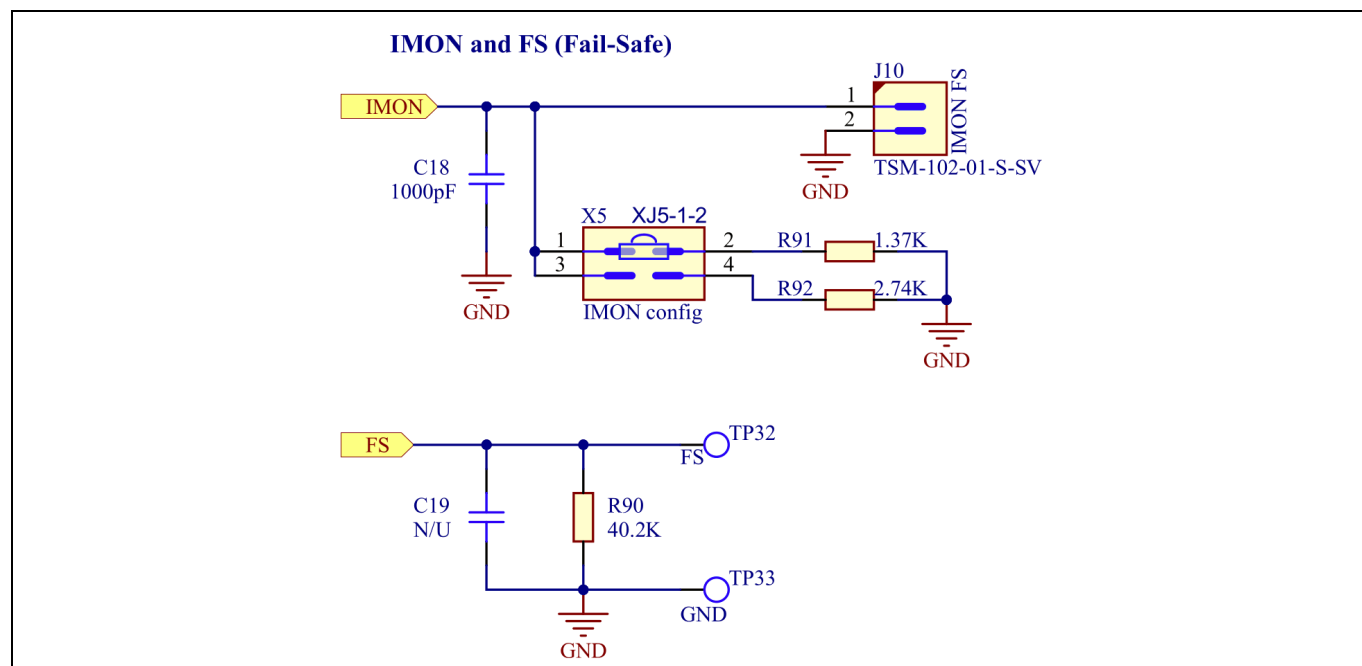


Figure 31 IMON and fail-safe

6.6 LED indicators

The board provides four status LEDs driven from the VLDO rail: PWRGD, SYNC, WARN, and FAULT.

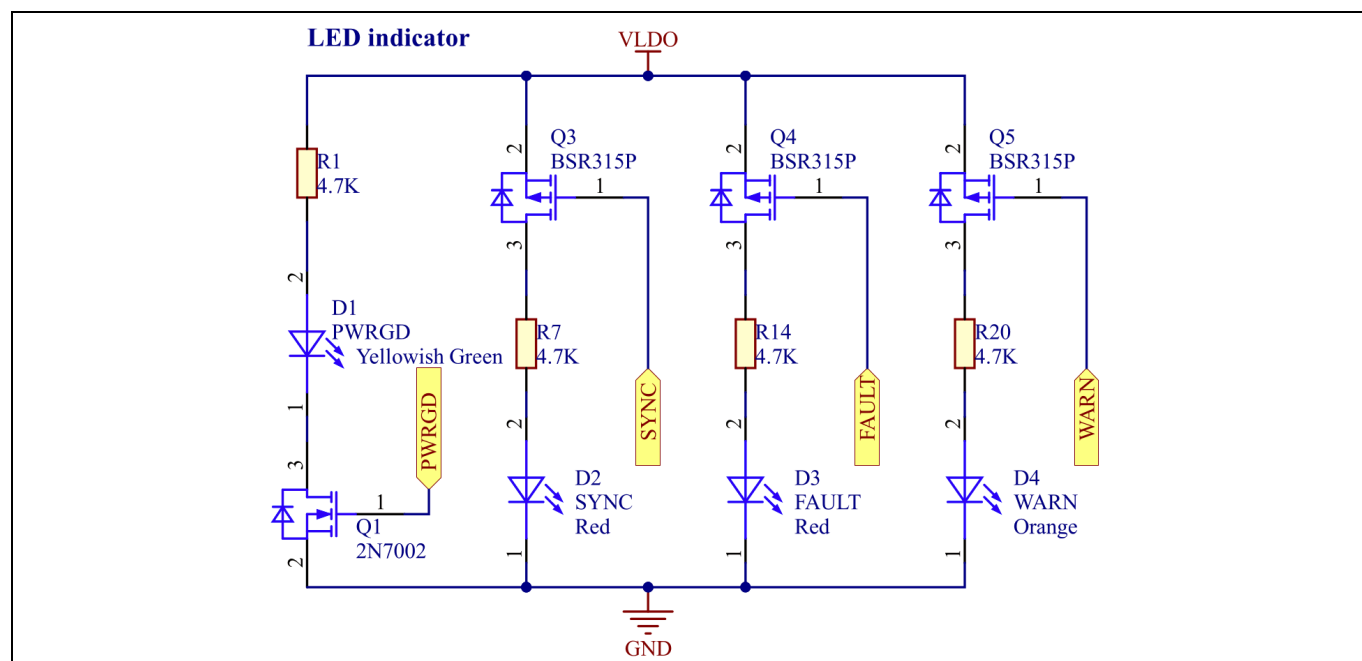


Figure 32 LED indicators

6 Board features

6.7 EN/UV and OV

The board provides an external EN pin to pull the EN pin HIGH or LOW as well as an built-in function to switch using the EN button on the GUI shown in [Figure 33](#). In addition, the board also provides voltage sensing through a resistor divider for overvoltage protection and undervoltage protection using integrated analog comparators.

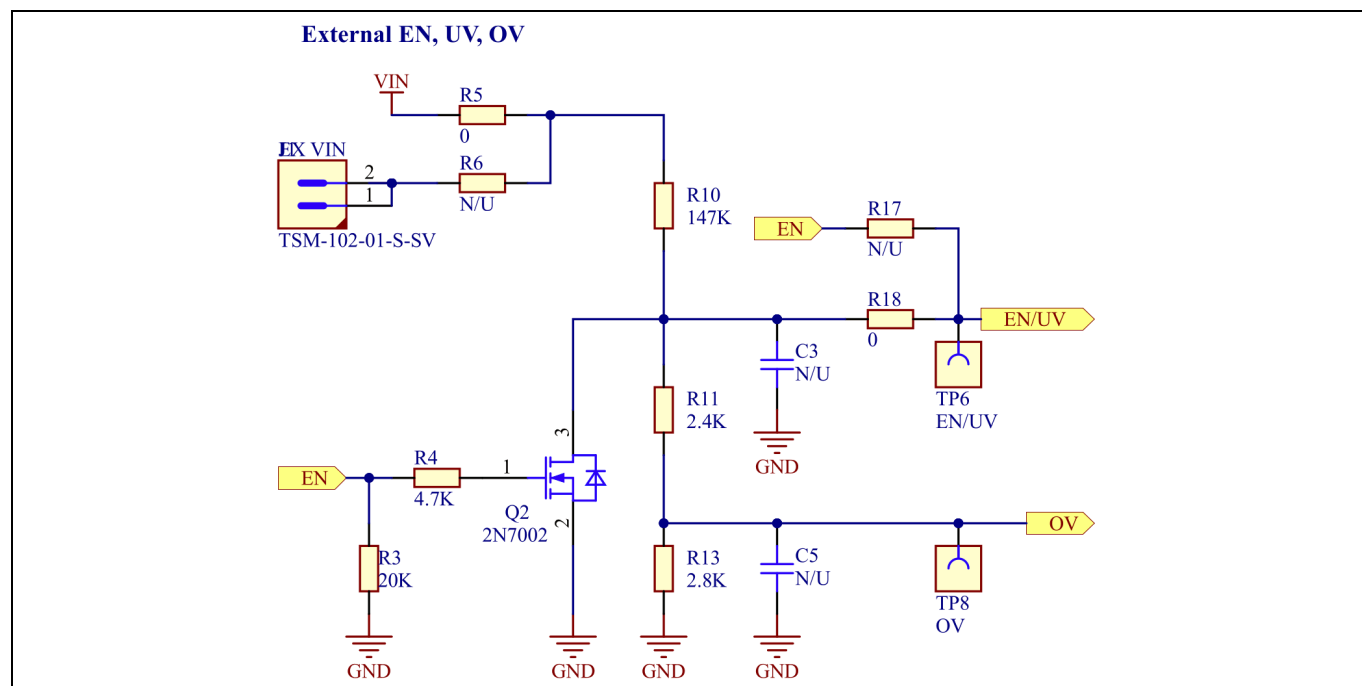


Figure 33 External EN, UV, and OV

7 Test results

7 Test results

7.1 Test setup

Figure 34 shows the test setup connections. The connectors on the left are input while those on the right are output connections. The header marked white is for I²C communication and programming of the XDP720-001 eFuse. The red wires on the left represent input positive terminals and, on the right, represents output positive terminals. The black wires represent the ground connections.

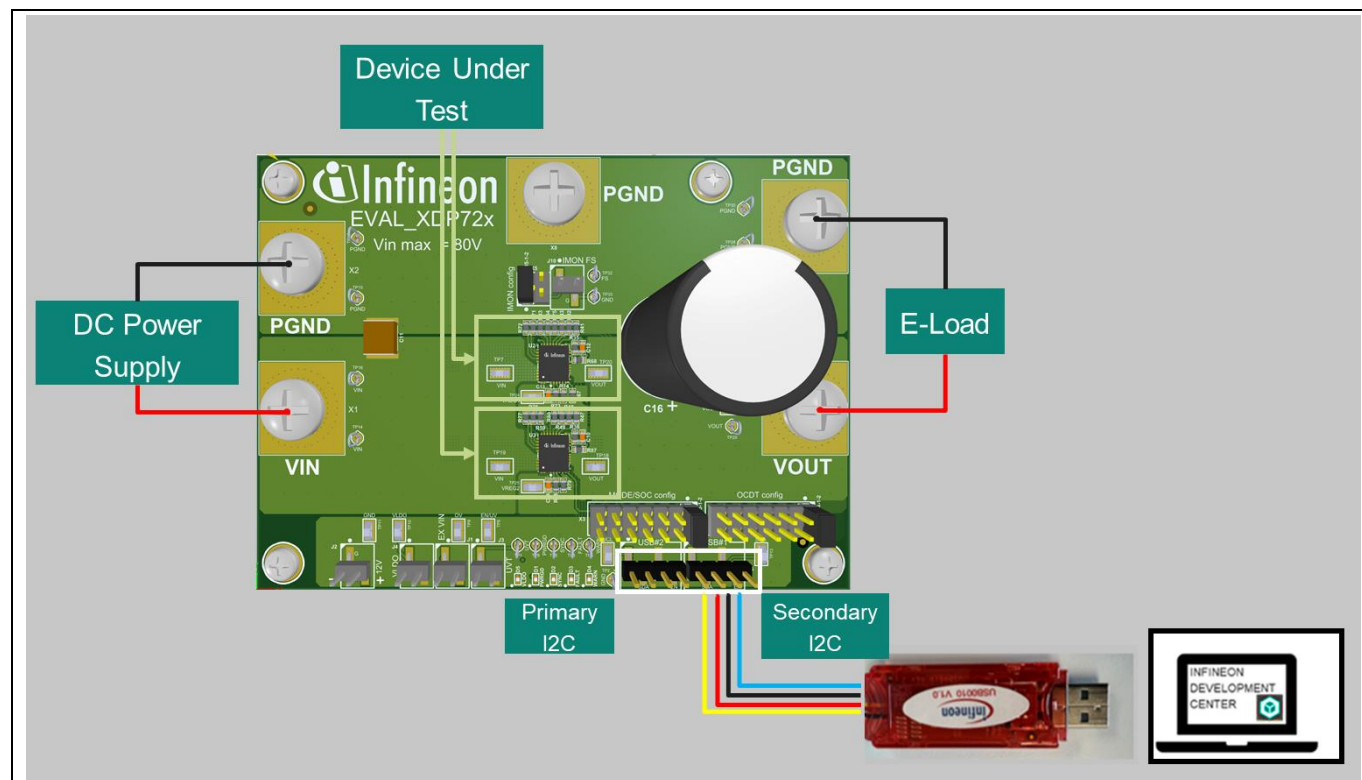


Figure 34 Test setup

7 Test results

7.2 Start up/down by EN cycling (VIN steady state)

Figure 35 shows startup and shutdown waveforms done by cycling the EN pin either on the GUI or with an external supply.

Test condition: Ambient $T_A = 25^\circ\text{C}$, $V_{IN} = 54\text{ V}$, Load 0 A .

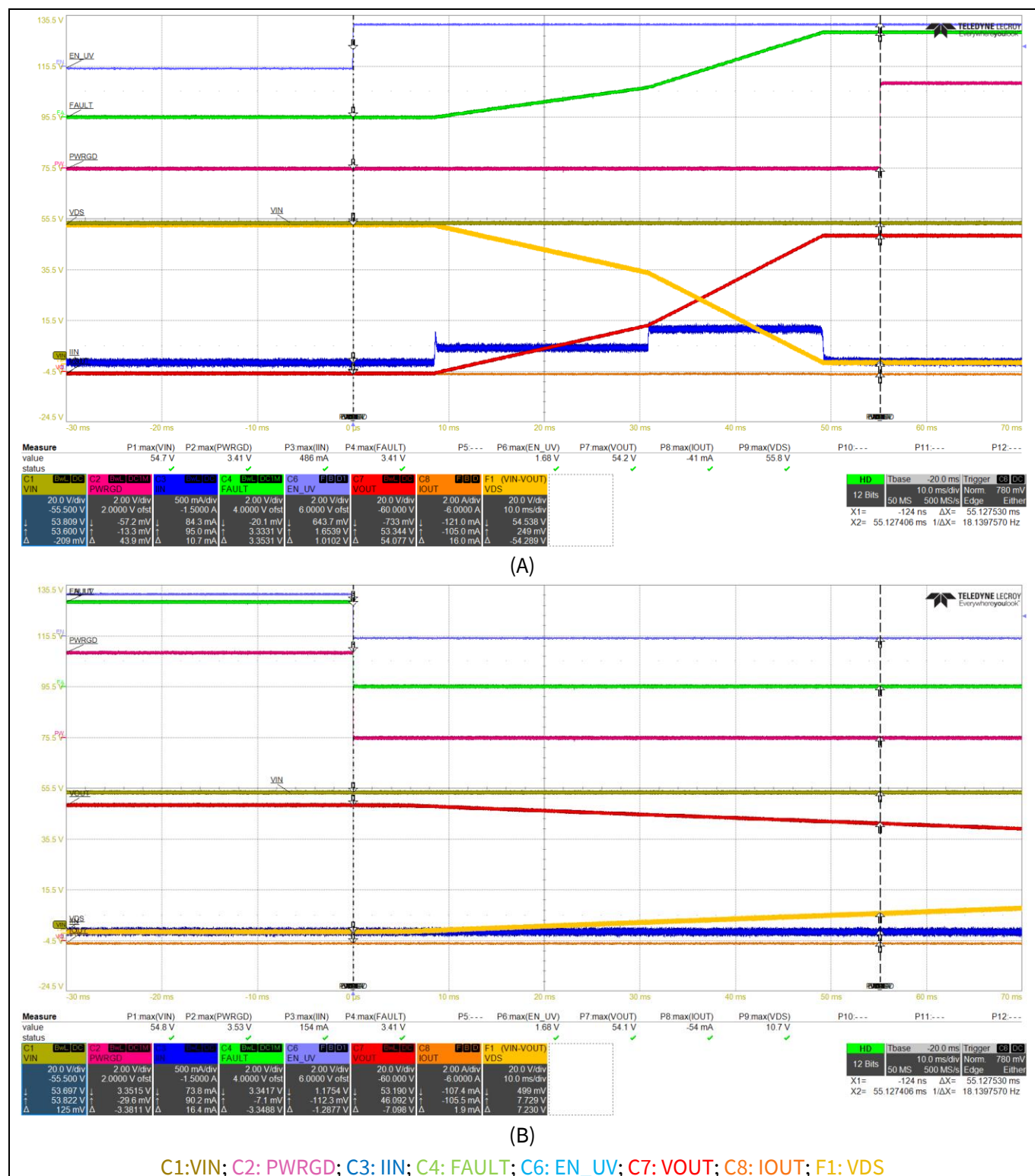


Figure 35 EN cycling (A) turn on; (B) turn off

7 Test results

7.3 Start up/down by VIN cycling (EN tie to divided VIN)

Figure 36 shows startup and shutdown waveforms done by cycling VIN.

Test condition: Ambient $T_A = 25^\circ\text{C}$, VIN = 54 V, Load 0 A.

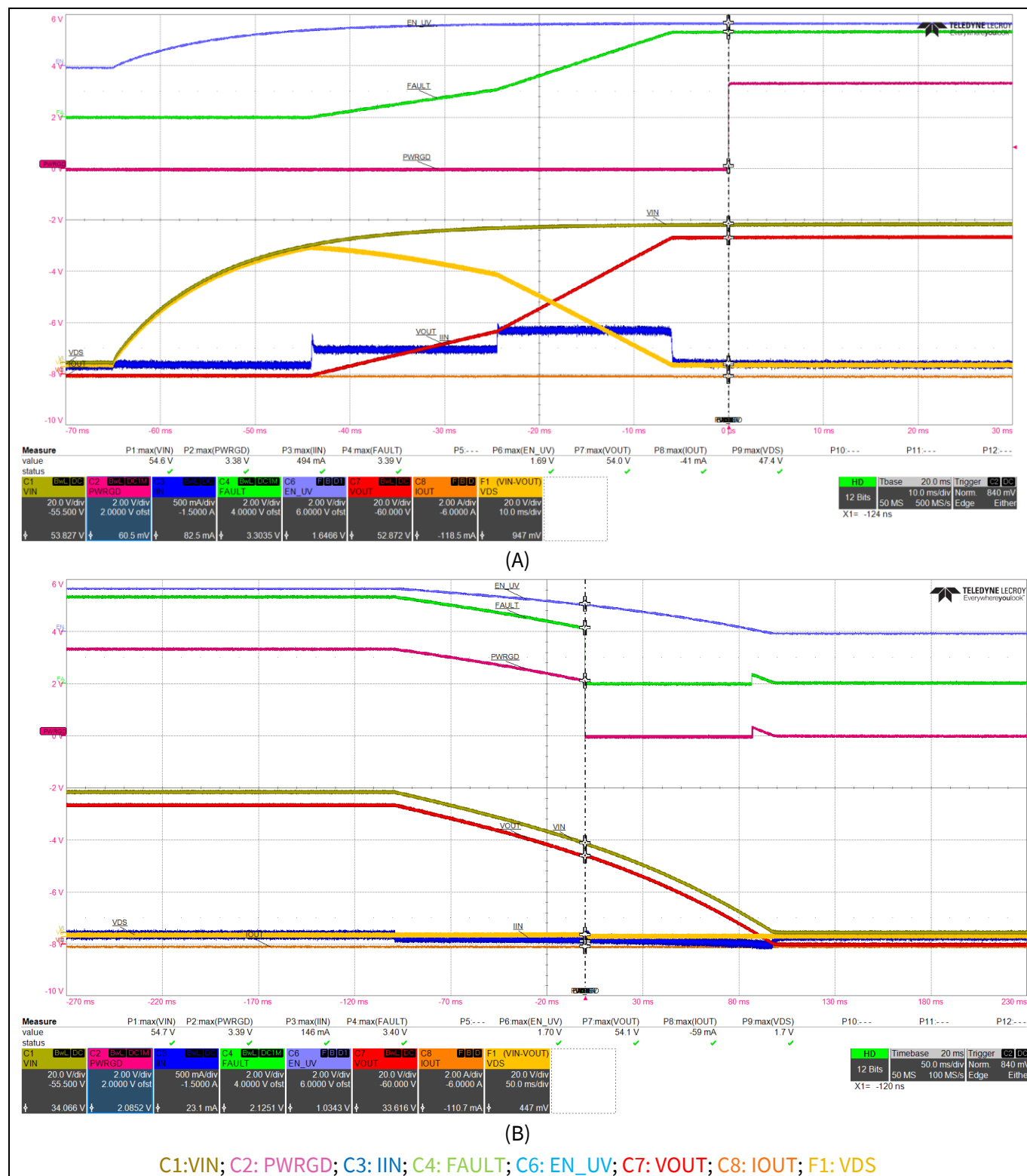


Figure 36 VIN cycling (A) turn on; (B) turn off

7 Test results

7.4 VIN swing test (turn on eFuse)

Figure 37 shows input voltage swing waveforms done by giving input voltage transient from DC power supply.

Test condition: Ambient $T_A = 25^\circ\text{C}$, VIN = 54 V, Load 0 A.

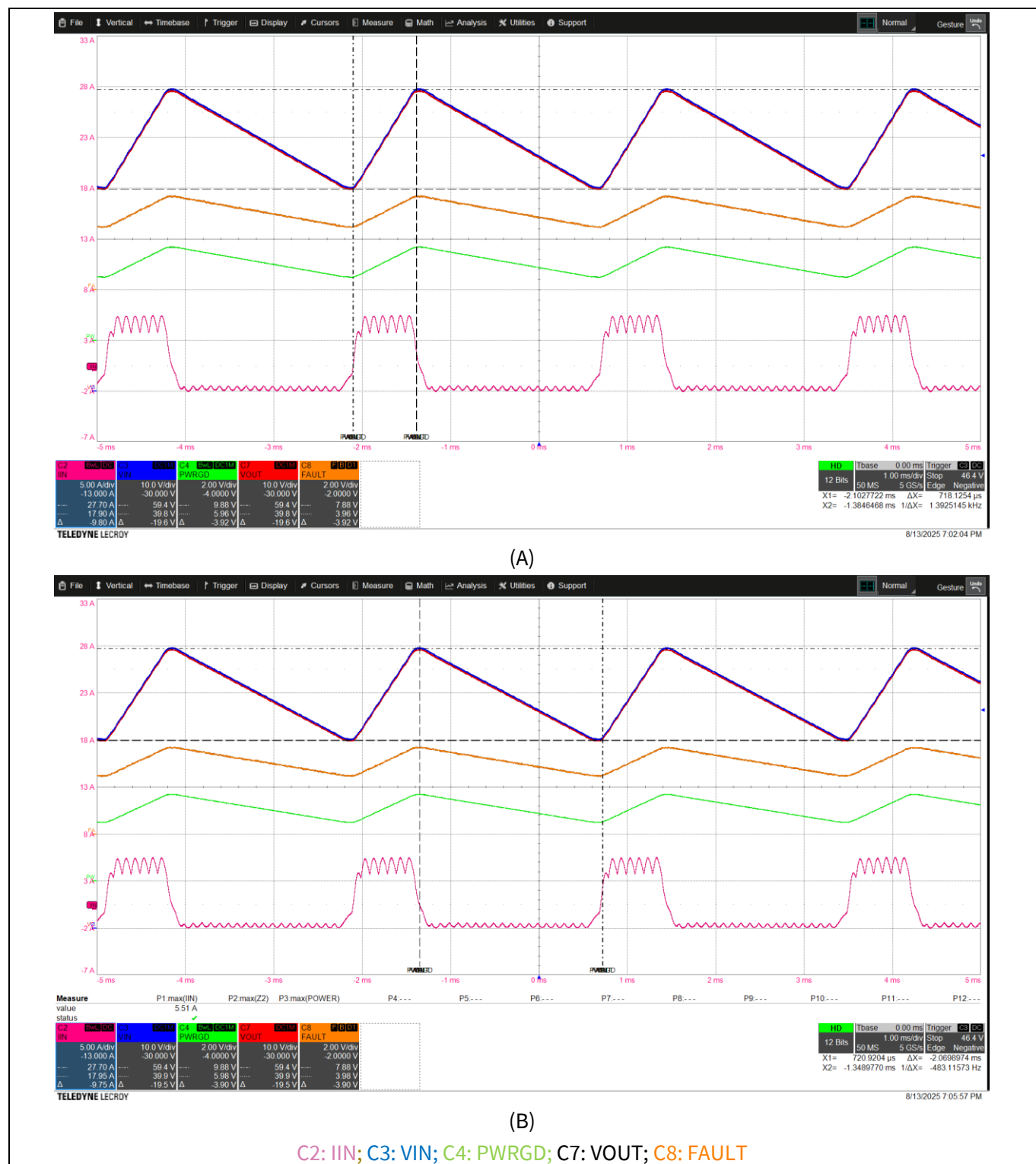


Figure 37 VIN swing test

7 Test results

7.6 Pre-bias output voltage during startup

Figure 39 shows startup waveforms done when the output is pre-biased to a certain voltage.

Test condition: Ambient $T_A = 25^\circ\text{C}$, $V_{IN} = 54\text{ V}$, Load 0 A prebiased at 50%.

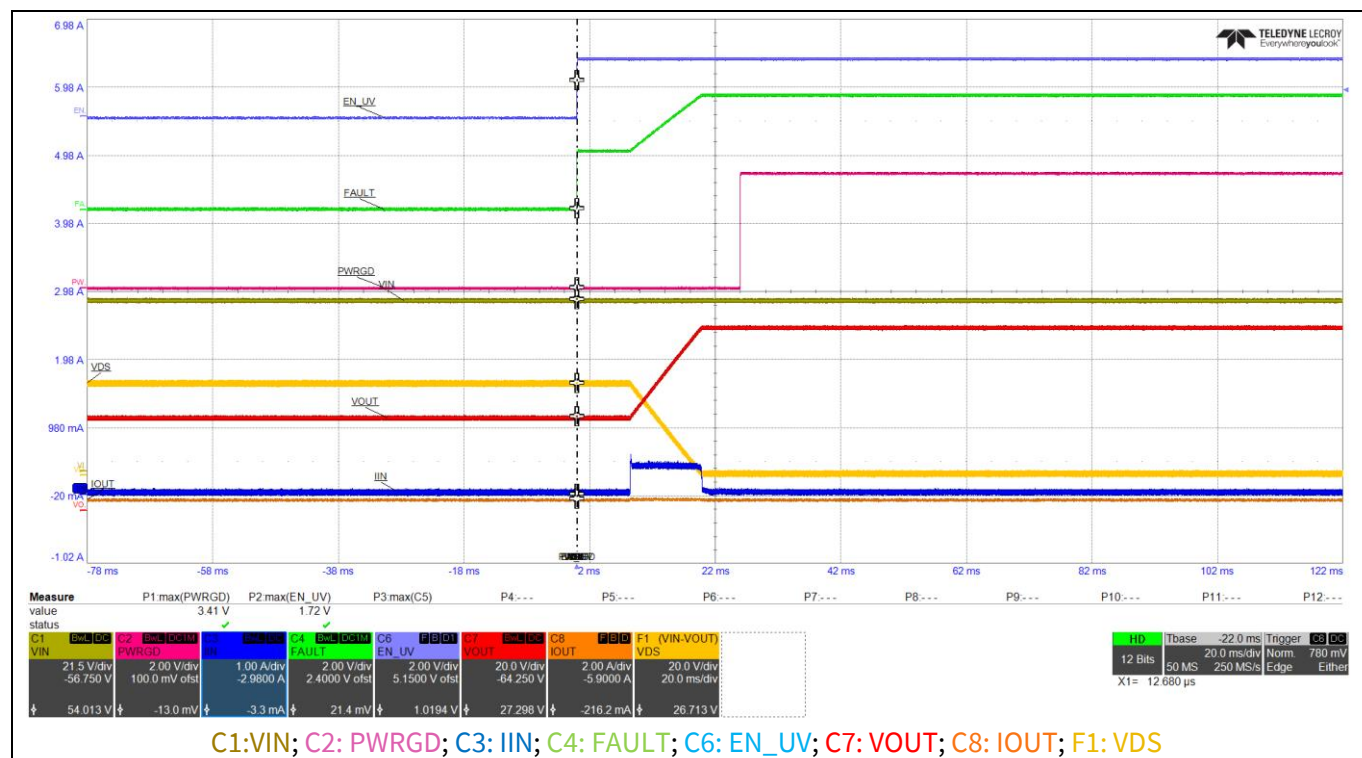


Figure 39 Pre-bias output voltage during startup

7 Test results

7.7 OCP including timer accuracy

Figure 40 shows overcurrent protection waveforms set at 21.8 A of current.

Test condition: Ambient $T_A = 25^\circ\text{C}$, $V_{IN} = 54\text{ V}$, Load 0 A .

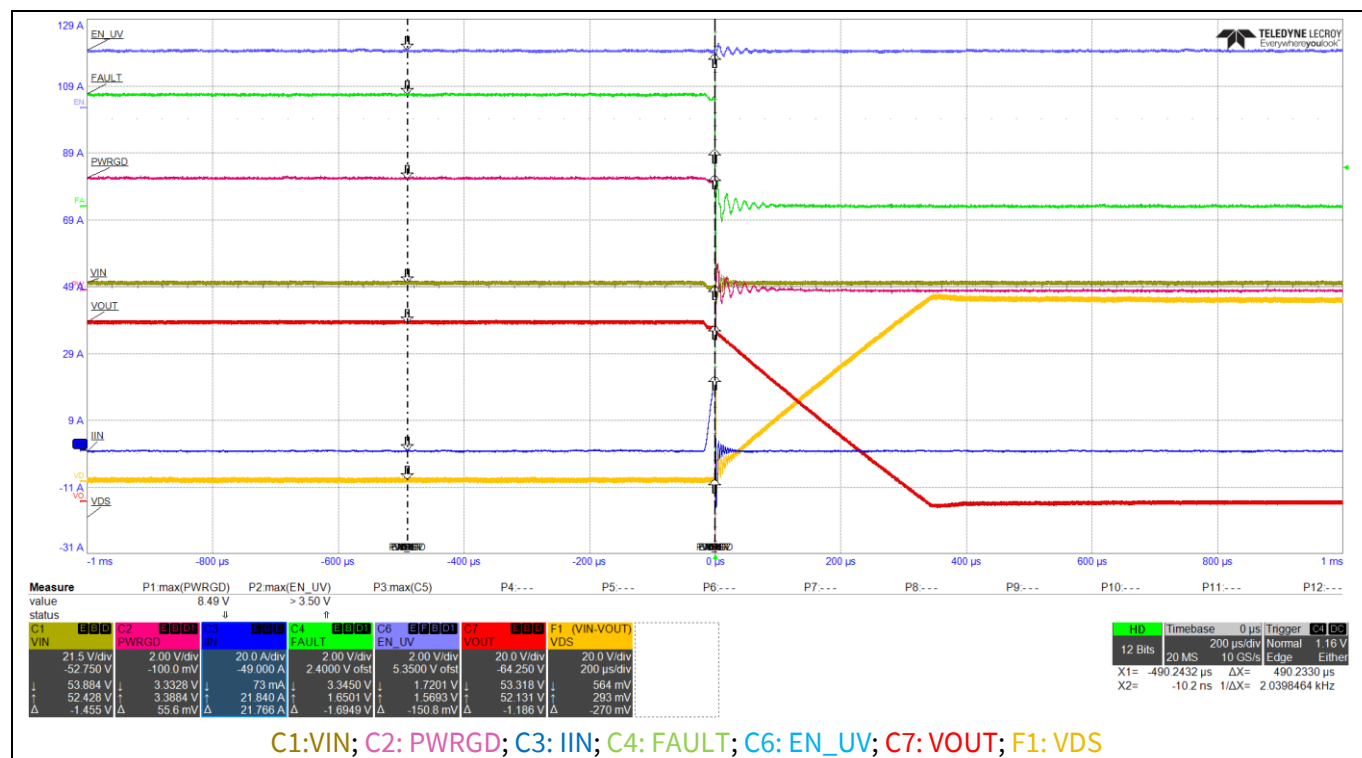


Figure 40 Overcurrent protection

7 Test results

7.8 OVP function

Figure 41 shows overvoltage protection waveforms which is set at 62 V on VOUT.

Test condition: Ambient $T_A = 25^\circ\text{C}$, $V_{IN} = 54\text{ V}$, Load 0 A .

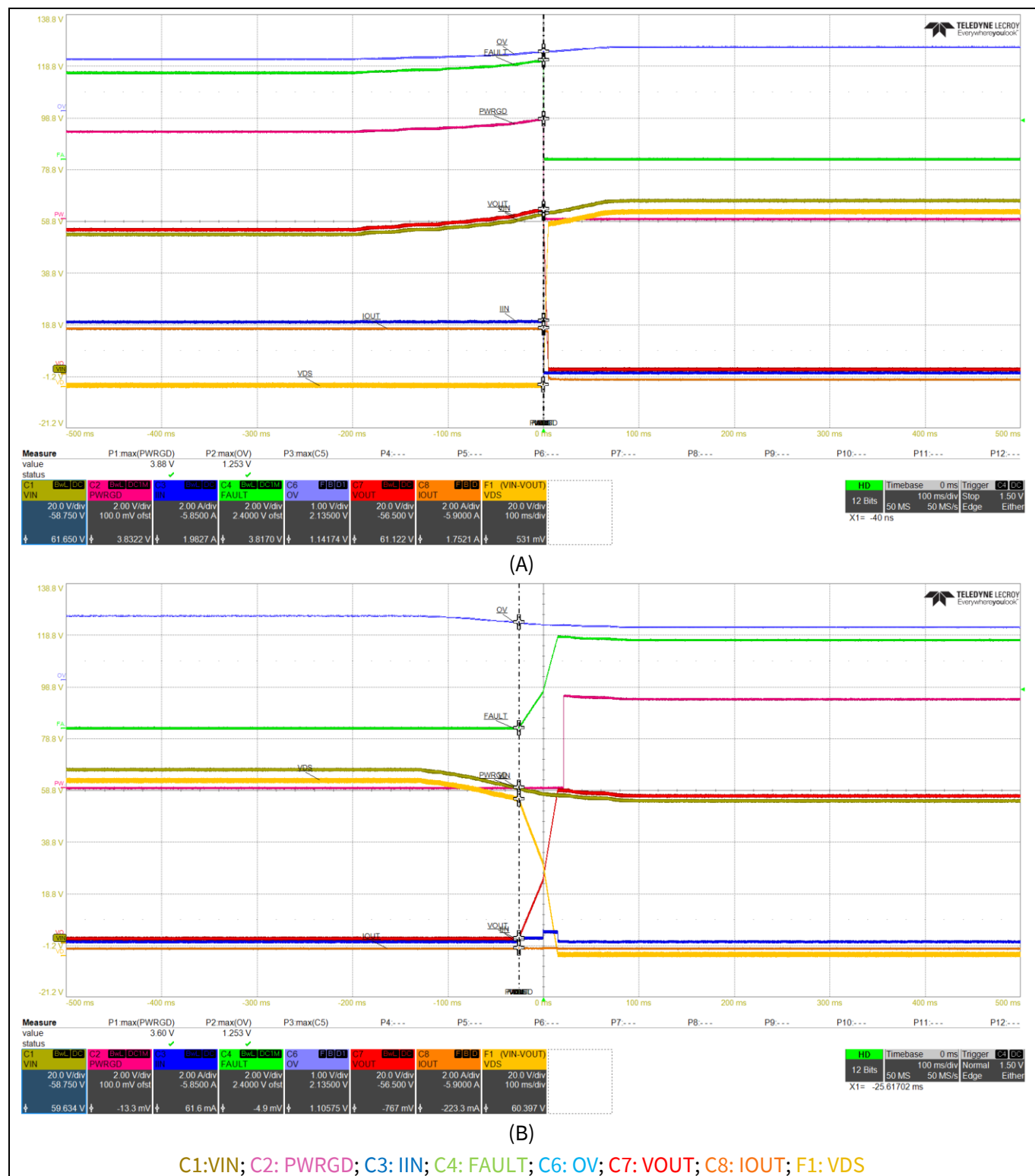


Figure 41 OVP protection (A) turn off at OV limit; (B) OV recovery

7 Test results

7.9 UVLO by VIN cycle

Figure 42 shows undervoltage protection waveforms set at 34.1 V.

Test condition: Ambient $T_A = 25^\circ\text{C}$, $V_{IN} = 54\text{ V}$, Load 0 A .

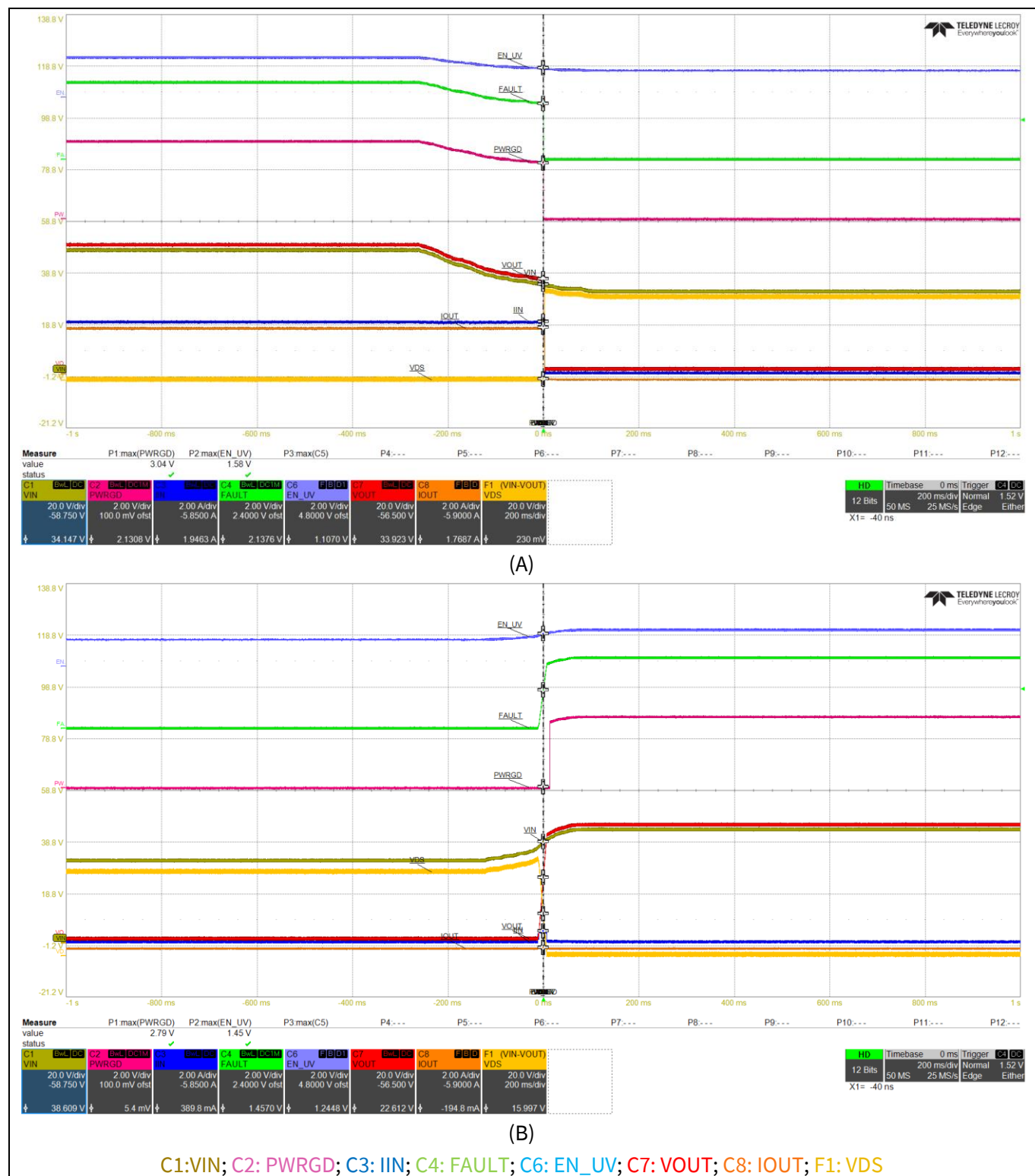


Figure 42 UVLO by VIN cycle (A) turn off at UV limit; (B) UV recovery

8 Related resources

8 Related resources

- [XDP™ protection and monitoring ICs](#) webpage
- EVAL_XDP72x_P100219B kit
- [Power Management ICs](#) forum from Infineon Developer Community

References

References

- [1] Infineon Technologies AG: *XDP720 20A digital eFuse datasheet*
- [2] Infineon Technologies AG: *XDP72x 20A digital eFuse datasheet*
- [3] Infineon Technologies AG: *XDP72x-001 Evaluation Board webpage*
- [4] Infineon Technologies AG: *XDP720-001 PMBus® commands user guide*

Note: Contact [Infineon Support](#) to obtain these documents.

Revision history

Revision history

Document revision	Date	Description of changes
V 1.0	2025-09-24	Initial release

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Customer shall not touch the Evaluation Board during operation and keep a safe distance.

Customer shall not touch the Evaluation Board after disconnecting the power supply, several components may still store electrical voltage and can discharge through physical contact. Several parts, like heat sinks and transformers, may still be very hot. Allow the components to cool before touching or servicing.

The electrical installation must be completed in accordance with the appropriate safety requirements.