The SupIR-SMD

A new IR HiRel surface mount device package

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About this document

Scope and purpose

This application note describes the improvements inherent in International Rectifier HiRel (IR HiRel)'s new SupIR-SMD package (patent #9,559,026).

Intended audience

This document is intended for applications engineers and designers looking for radiation-hardened (rad hard) power MOSFET solutions for Space and other harsh environment applications. The goal of this application note is to guide the designer in selecting the right package to suit the needs and constraints of the application.

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1 Introduction

IR HiRel would like to present this document to describe the improvements inherent in our new SupIR-SMD package [1] (patent #9,559,026). Due to material differences between circuit boards and the large power devices assembled onto those boards, there is a significant challenge to maintain reliable solder joints between the two, and to preserve the sealed integrity of highly reliable, hermetically packaged devices. The new package, as described in this application note, provides a means whereby a more optimal solution can be achieved in a simpler, more cost-effective manner. Direct mounting can now be more easily implemented for high-reliability space missions with severe thermal cycling as part of the mission profile.

Figure 1 SupIR-SMD package

The new package design implements several features to allow for relief of thermally-induced stress in the solder joint between the circuit board and the device package itself. This application note will follow this general outline:

- First, it will briefly describe the general problem of thermal mismatch.
- Second, it will review some of the prior art that allowed for a solution to this problem.
- Third, it will show the new package and describe the mechanical features of interest.
- Fourth, it will describe the environmental qualifications of the new SupIR-SMD package as mounted on a printed circuit board (PCB).
- Fifth and last, it will present feedback from customers and present application guidelines such as the solder pad layout used in our own qualification of the part.

2 A summary of the design challenges

It is an inherent property of materials to change their dimensions by expanding and contracting with temperature changes. It is the difference between materials' expansion that gives rise to the stress and strain that can cause problems in assemblies.

For example, consider only one linear dimension of a material. Metals, ceramics, and printed circuit boards (PCB, such as FR-4 and polyimide) will expand at different rates for incremental positive changes in material temperature. The change in length of a material due to a change in temperature is defined [1] by the equation

$$\Delta l = \alpha \cdot l_0 \cdot \Delta T \qquad [1]$$

where l is the material length, α is the coefficient of linear expansion in units of 10^{-6}/K (or ppm/K) and ΔT is the change in temperature in degrees Kelvin. So, for an α of 100 ppm/K there would be a 0.01% change in the length of a material. This does not seem to be of concern by itself, until one considers this question: when is the expansion too small to cause problems for a highly reliable power connection? Even small deflections result in stress and strain that are a recipe for problems. Coefficients of thermal expansion for various materials as used in IR HiRel analyses are shown below in Table 1.

Table 1 Material properties used in analyses

Material	α (10^{-6}/°C)
Copper [3]	16-17
FR-4 circuit board [4]	13-14
Polyimide circuit board [5]	18

A one-dimensional analysis is an oversimplification for this real world application. Material expansion occurs in all three dimensions, and those relative movements of objects which would ideally remain fixed (and electrically attached) can integrate over area and volume to create a significant problem.

PCBs are not uniformly constructed, they are laminated. The problem complexity increases as the copper traces, reinforcement fiber, and epoxy or polyimide (the resins holding the layers together) are taken into consideration.

The previous discussion only considers uniform thermal expansion, when, in truth, expansion coefficients themselves can be a function of temperature.

IR HiRel power devices are housed in hermetic packages made mostly from a combination of metals, ceramics, and glass. Ceramic and glass have a coefficient of thermal expansion (CTE) around 6 ppm/K, and most PCBs have CTEs in the aforementioned range of 13-14ppm/K (FR-4 board) or 17-18 ppm/K (polyimide board). The large CTE mismatch between ceramic/glass and PCB materials poses major challenges in the design of hermetic packages for power devices.

There is a fundamental difference between metal and ceramic/glass: metal is ductile and ceramic/glass are brittle. When subject to large levels of stress, metal will yield and experience large strain without breaking, whereas ceramic/glass will not yield: it will just crack. This "make-or-break" property of ceramic/glass adds another challenge to the design of hermetic packages.

Furthermore, power devices usually carry large current and dissipate a lot of heat, even with chips that have high efficiency. In order to dissipate heat, some stress relief designs such as a J-lead or a gull-wing lead cannot be used, because they do not carry large amount of heat. In other words, it is hard to satisfy electrical, mechanical, and thermal requirements simultaneously.

Due to the above challenges, it is extremely difficult to make large surface mount hermetic power package compatible with most common PCBs. For years, ceramic cracking has been a problem when surface mount power devices are directly mounted on PCBs. Some examples of fractures in finished circuit card assemblies of power components can be seen in Figure 2 through Figure 4.

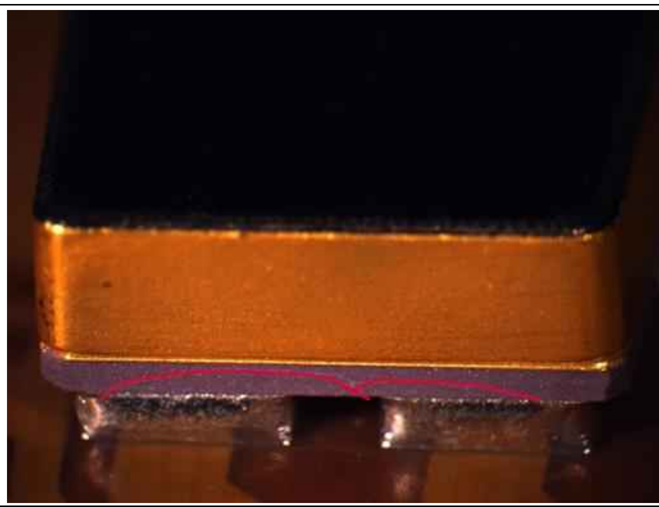

Figure 2 IR HiRel surface mount device on polyimide circuit board (cracks delineated in red)

Figure 3 Stress fracture in a surface mount device on a circuit board

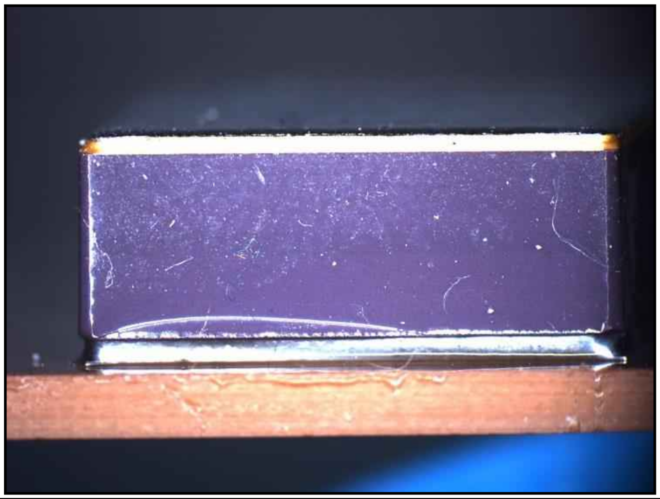

Figure 4 Stress fracture in surface mount device

IR HiRel has produced packaged power devices for decades and depending on the temperature extremes and number of thermal cycles expected those parts have seen use from the ocean's floor to beyond the orbit of Pluto. While the reliability of those packages is very high, these issues of thermal expansion can require some unique solutions for mounting larger devices, depending on the temperature extremes expected in each application.

3 Existing solutions

Different parties involved in packaging of high reliability power devices have tried to solve the problem of cracks in ceramic from different perspectives. For example, system integrators who use power devices have tried to modify the local properties of a PCB by inserting a low CTE material under the power device, and package suppliers, for their part, have tried to develop stronger ceramics. These efforts have had only limited success and have not been widely adopted by the industry.

For many years, IR HiRel has offered package lead or carrier options to its customers to overcome issues of CTE mismatch between the power device and its PCB for those applications where the thermal expansion was deemed risky. As described to some degree in AN-1016 [6], IR HiRel offers various lead options and carriers for larger surface mount devices to enable better assembly when the temperature range of the application's circuit board is large enough to cause concern.

In this section, we shall describe (from smallest to largest) the SMD packages for IR HiRel standard discrete MOSFET and diode power devices. Let us begin with the SMD-0.2 as shown (reference outline drawings can be found on the IR HiRel website [7]) in Figure 5, and state that IR HiRel has, in fact, found very few customers who have concerns with thermal expansion with the SMD-0.2 package, since it is so small.

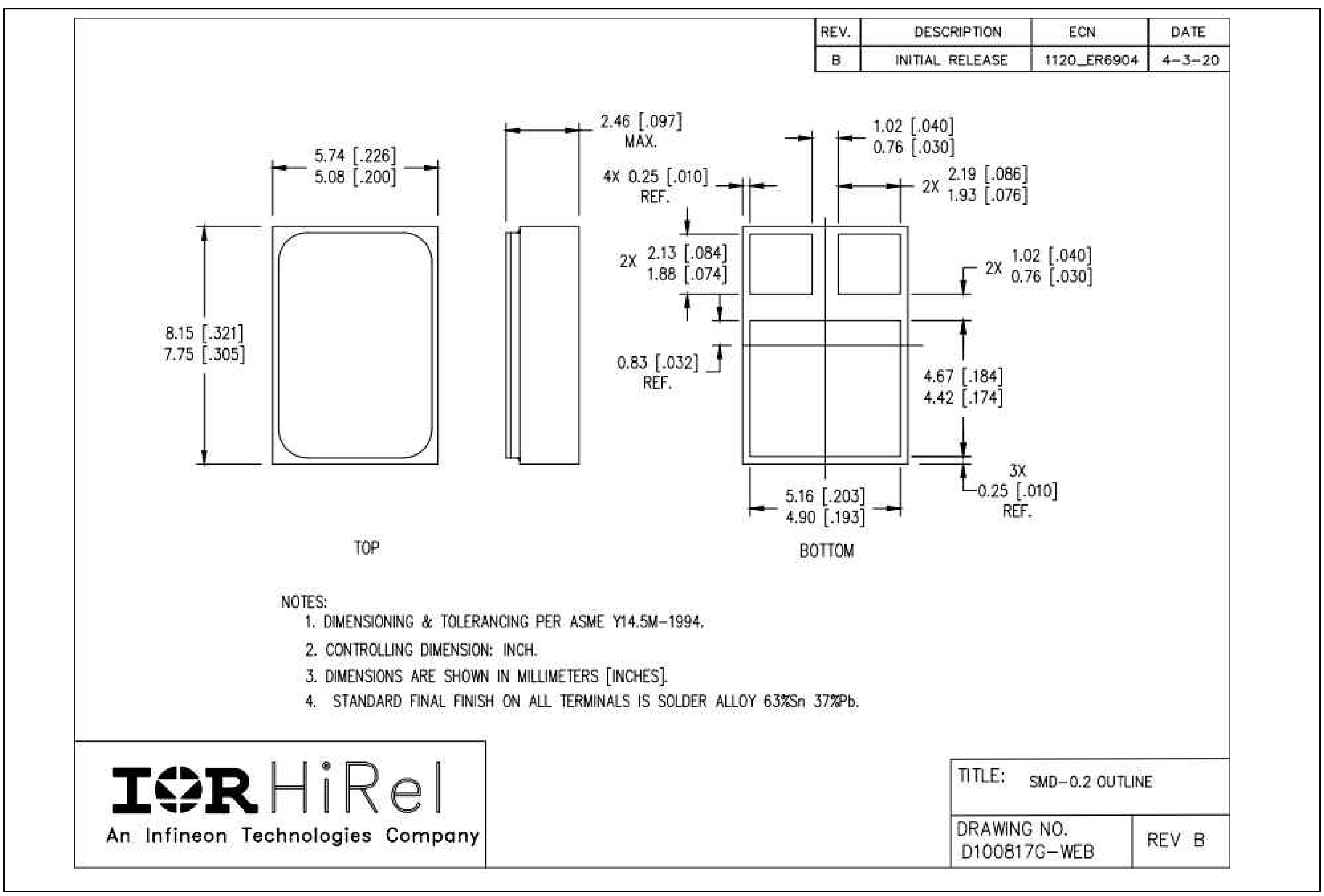

Figure 5 SMD-0.2 outline drawing (See IR HiRel website)

Existing solutions

Since this SMD-0.2 device is rather small, IR HiRel has not seen a need to provide any packaging options other than the standard.

The next size up is the SMD-0.5, as shown [8] in Figure 6.

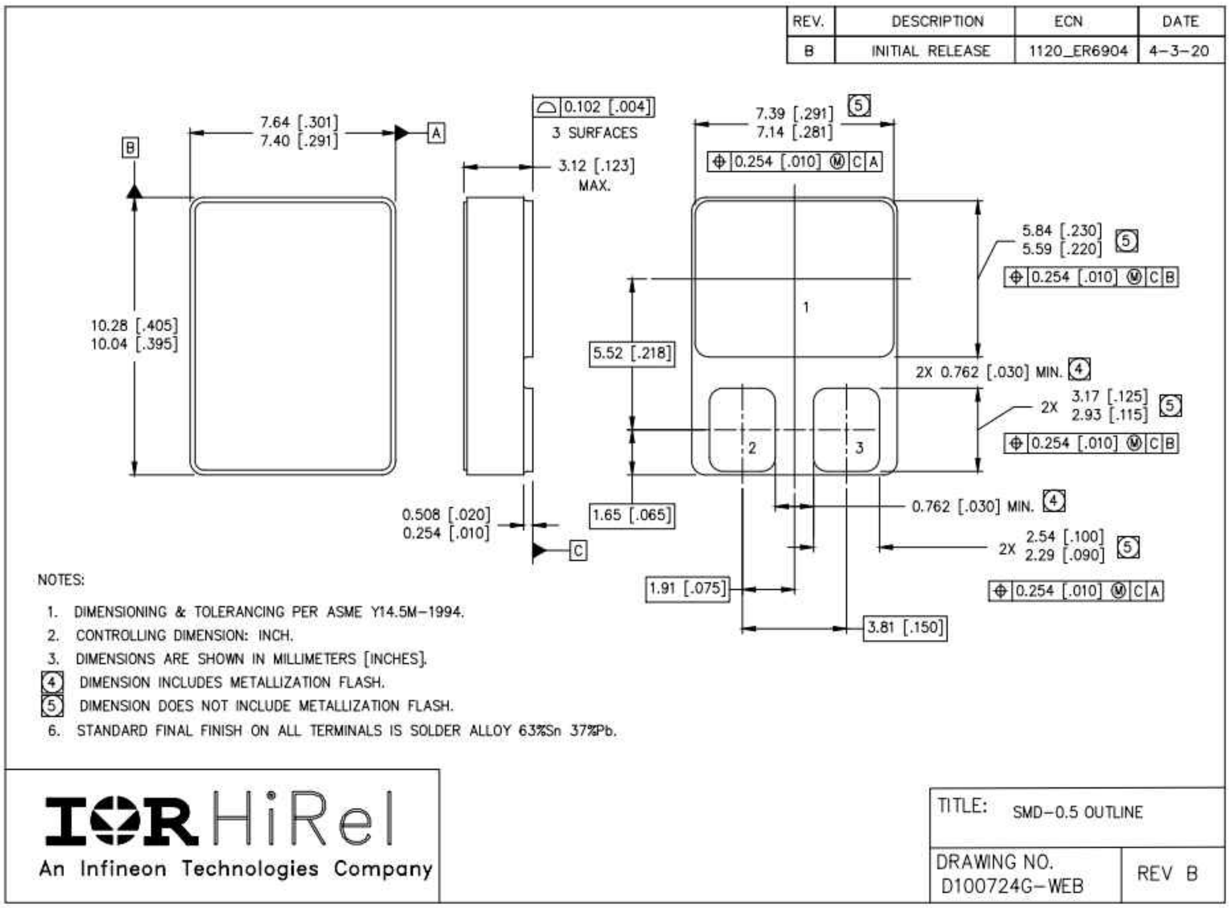

Figure 6 SMD-0.5 outline drawing (See IR HiRel website)

There are options for this package (and one of the subsequent sizes) to provide strain relief in the forms of lead attachment of ribbons of copper to the SMD package. The concept of this is shown in Figure 7 and the dimensions of the lead attach option is shown [8] in Figure 9.

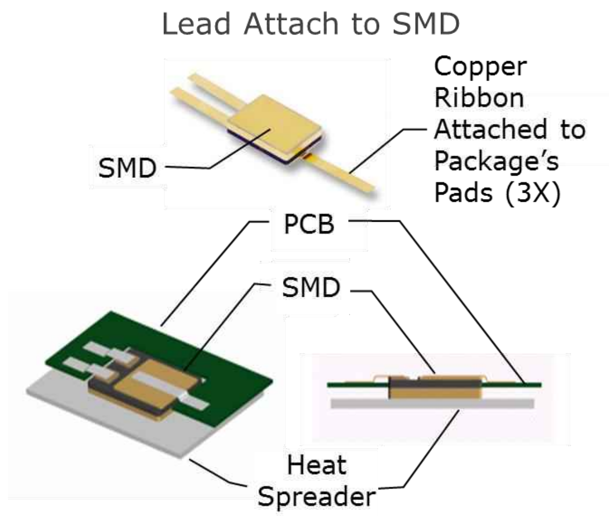

Figure 7 Lead attachment option for SMD to solve assembly thermal expansion concerns

An example of how a standard SMD part would be mounted on a board where the actual application temperature extremes would cause concern regarding thermal expansion is shown in Figure 8. (This assembly is typical of a Space level, satellite board design for a power conversion system as delivered by IR HiRel.)

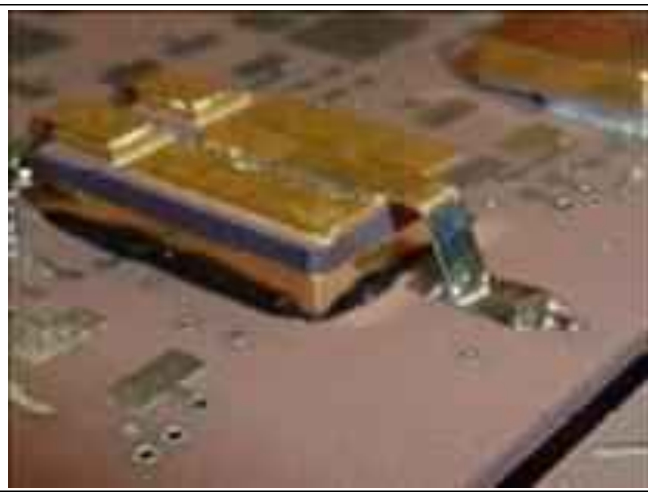

Figure 8 Example assembly with SMD-1 and ribbon leads

It is worth noting that this type of construction, while allowing for proper thermal expansion relief between the rad hard part and its circuit board, does not provide the optimal thermal path for heat removal from the device. The die is mounted on the terminals' side of the package and the heat must flow through the attached leads to the circuit board and/or through the sidewalls to the lid and down to the heat spreader. Also, the leads add parasitic resistance and inductance. Derating for Space grade components alleviates this problem, as the heat that results in a derated application can often be sufficiently conducted in this manner.

Existing solutions

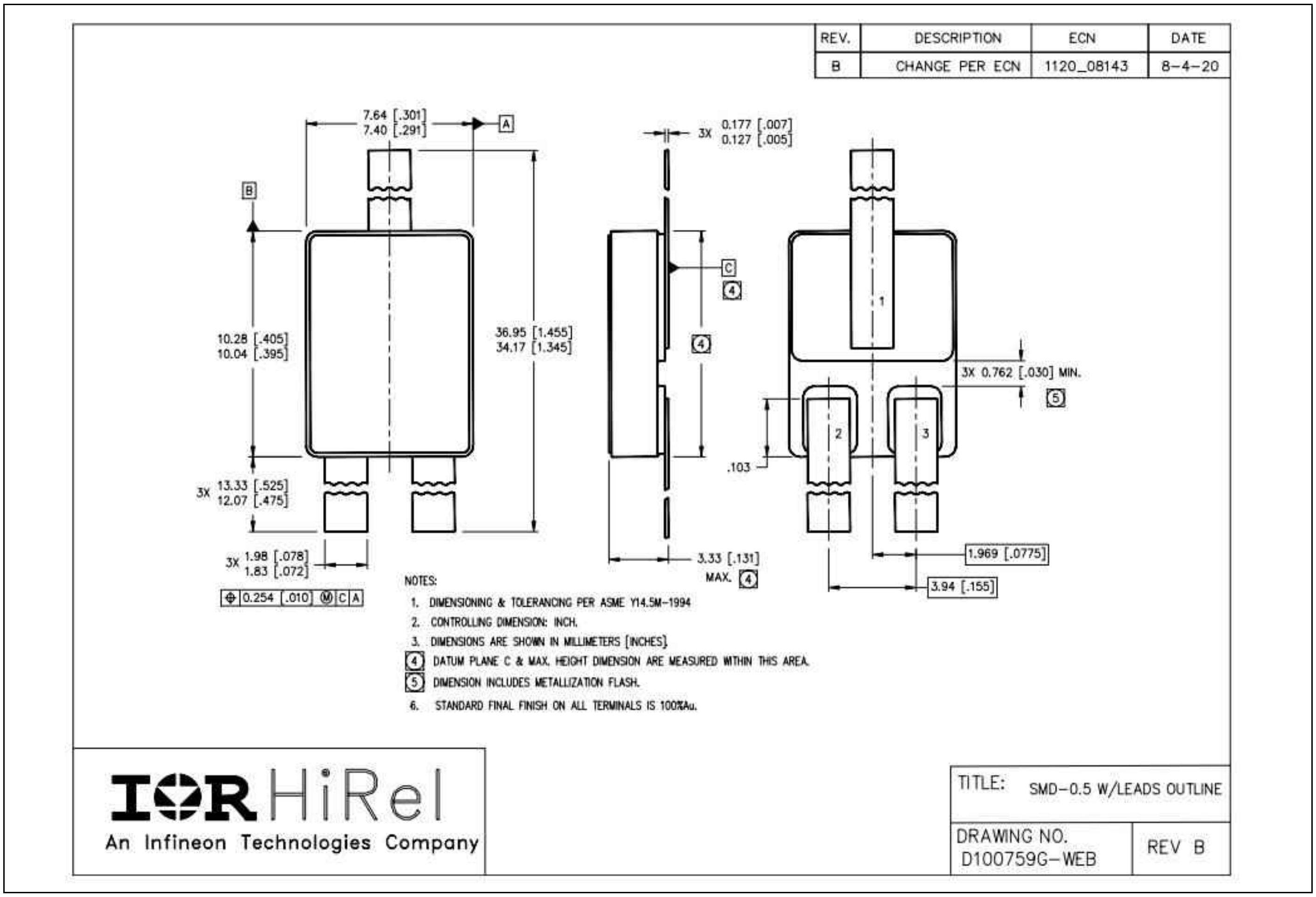

Figure 9 SMD-0.5 with leads, outline drawing (see IR HiRel website)

The next size larger package is the SMD-1 as shown [9] in Figure 10.

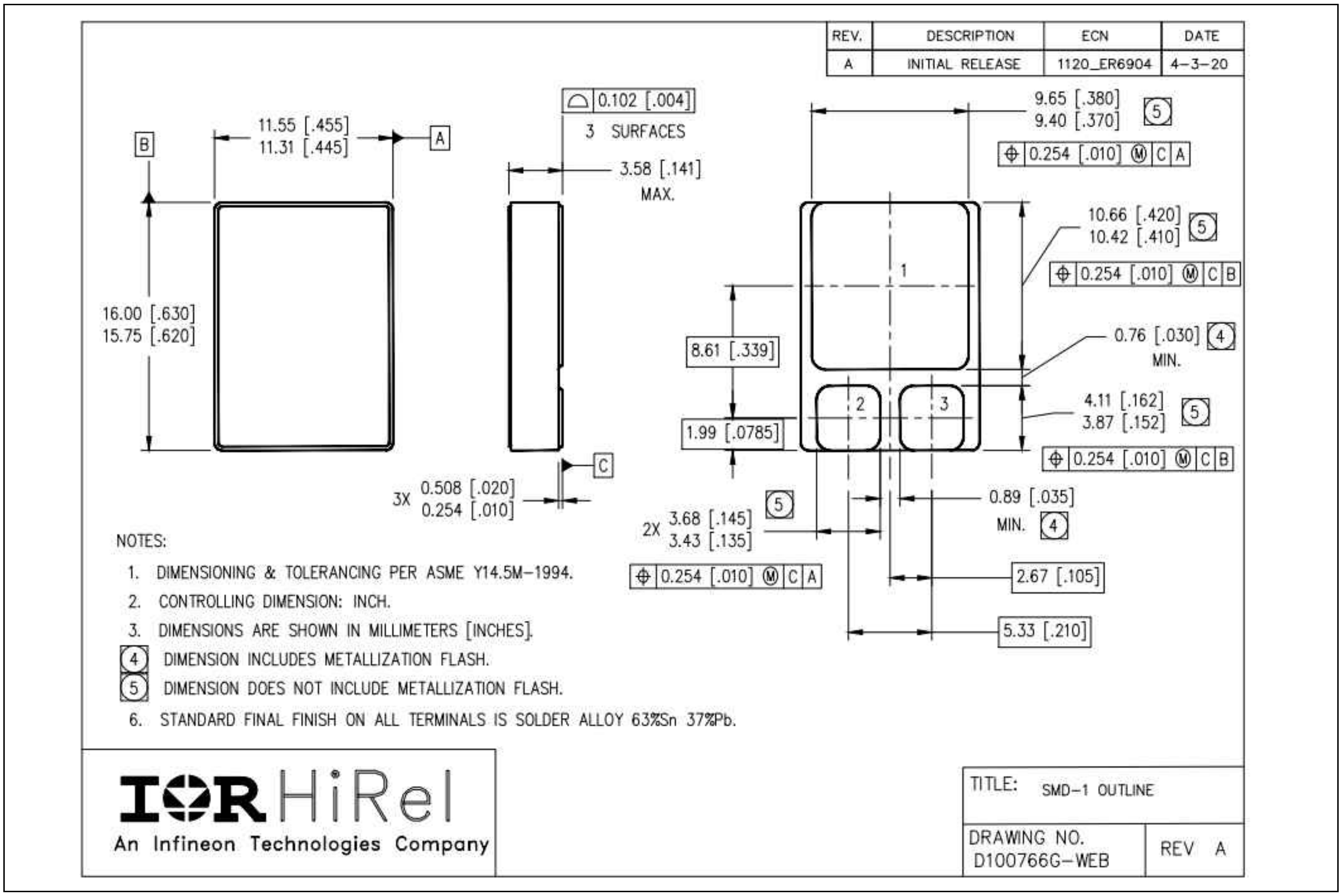

Figure 10 **SMD-1 outline drawing (see IR HiRel website)**

As the reader may begin to imagine, as the size of our packages increases, the concerns regarding thermal expansion (and now heat removal) become more prevalent. In this package style, not only is a lead attachment option available for thermal expansion concerns [9]as shown in Figure 11, but we also have a part carrier so the heat can flow more directly down through the bottom of the device to allow for a better thermal path.

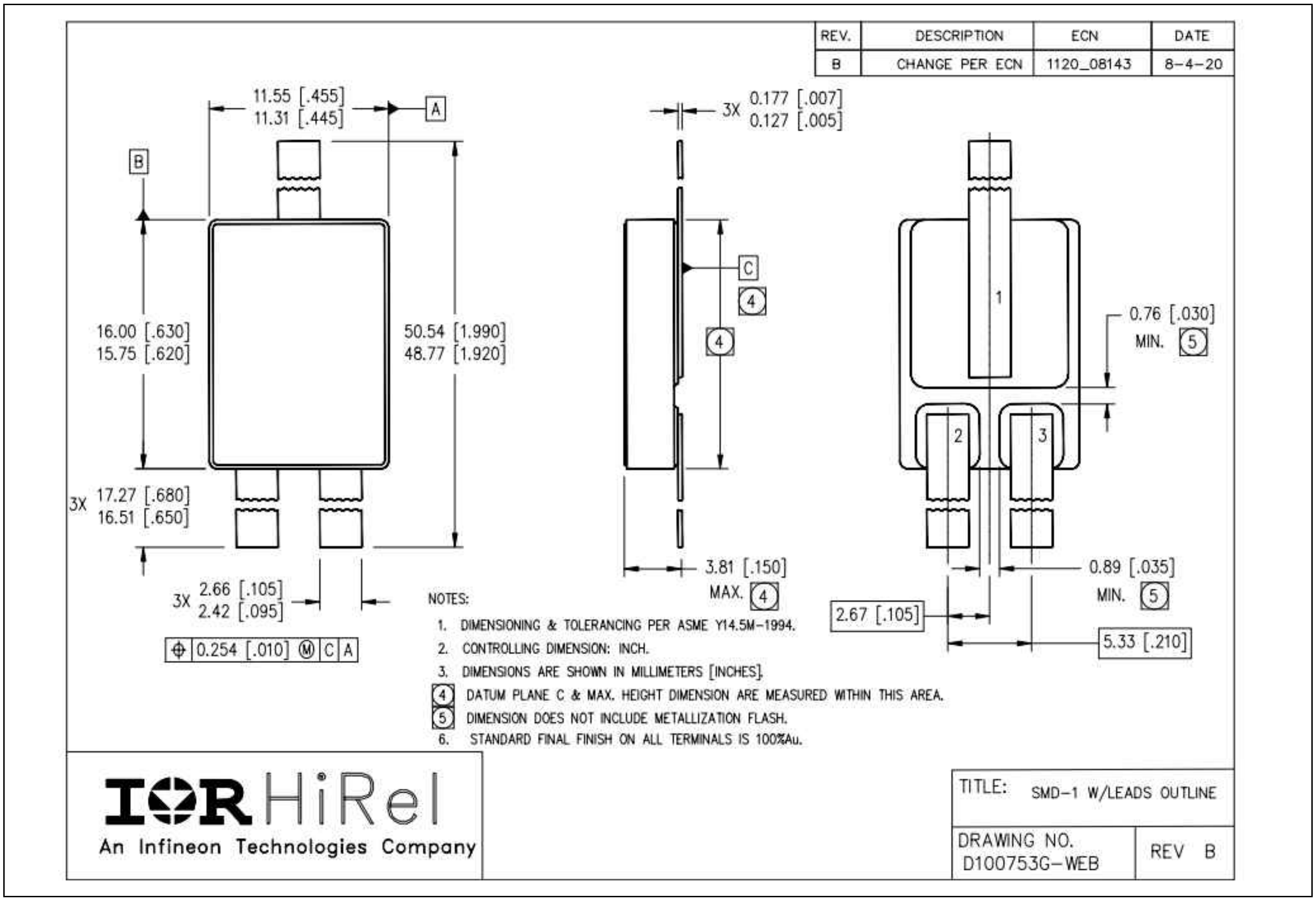

Figure 11 SMD-1 with leads, outline drawing (see IR HiRel website)

The concept of the part carrier is to provide a strain relief in the leads as well as to allow the heat to flow more directly down through the device mounting. The physical construction of the carrier is described in a higher level in Figure 12.

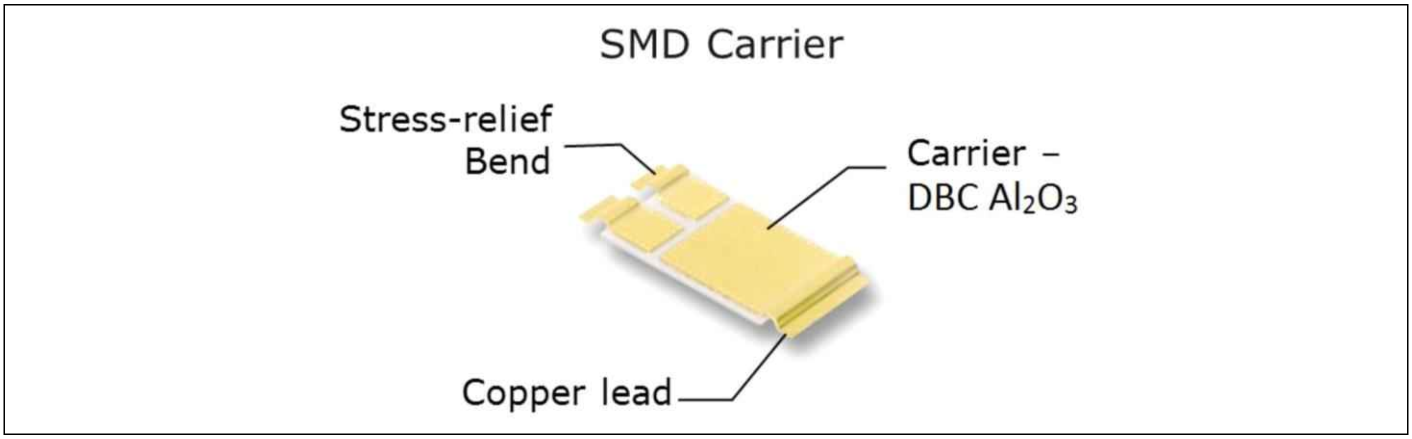

Figure 12 Carrier for SMD

The direct bond copper substrate provides a more direct thermal path down through the carrier. The visual representation of an SMD part on a carrier is shown in Figure 13 using the next size (SMD-2) to give the reader some idea of how large the solution has become, relative to the original package.

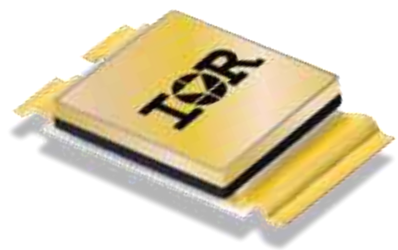

Figure 13 SMD-2 on carrier

The carrier itself for an SMD-1 is described [9] in more detail in Figure 14.

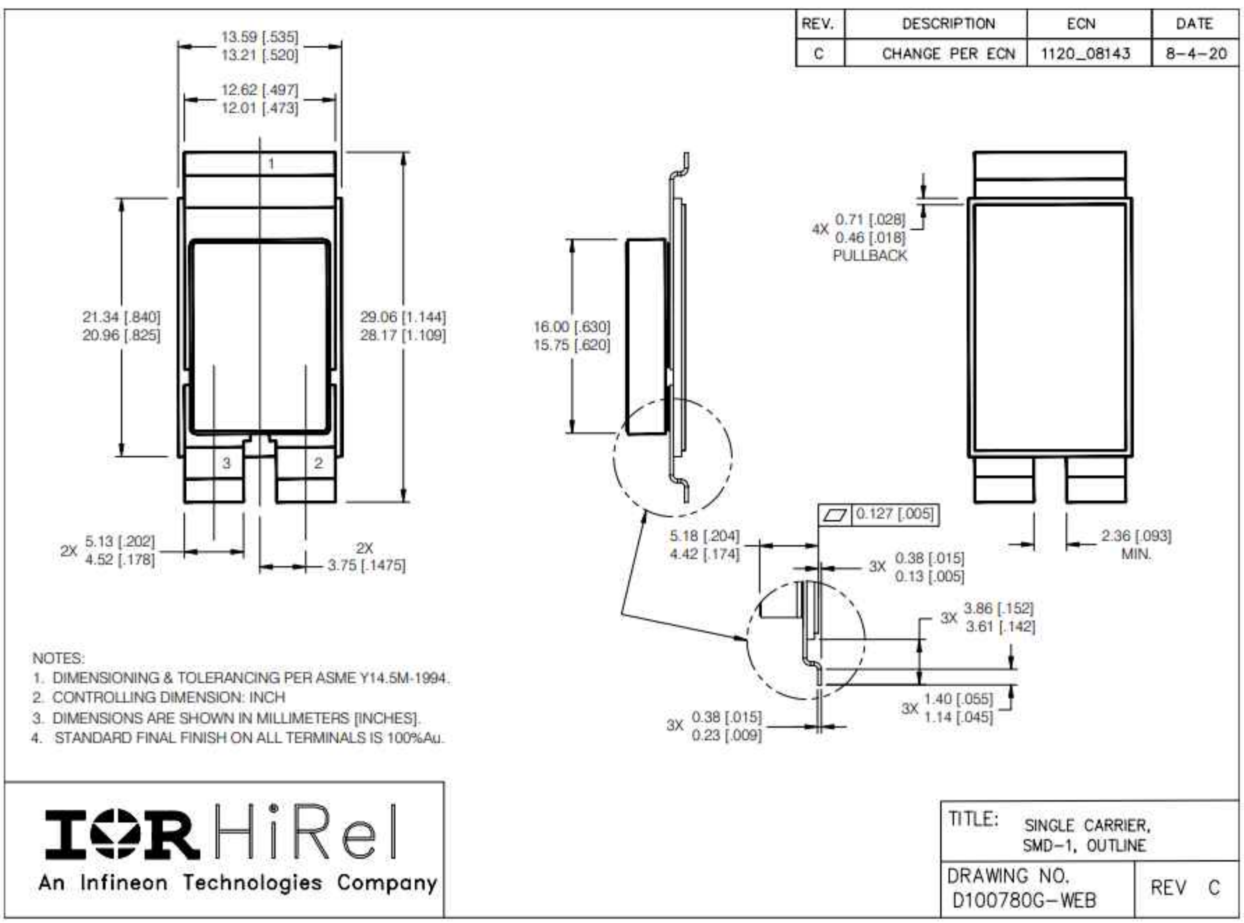

Figure 14 SMD-1 on carrier, outline drawing (See IR HiRel website)

Existing solutions

Finally, the largest legacy SMD discrete device package from IR HiRel is the SMD-2. We have now arrived at the package size which shall be compared to our newest improvement, the SupIR-SMD, which shall be described in more detail in the next section of this document. This device is shown [10] in Figure 15, with the leads and carrier options shown in Figure 16 and Figure 17, respectively.

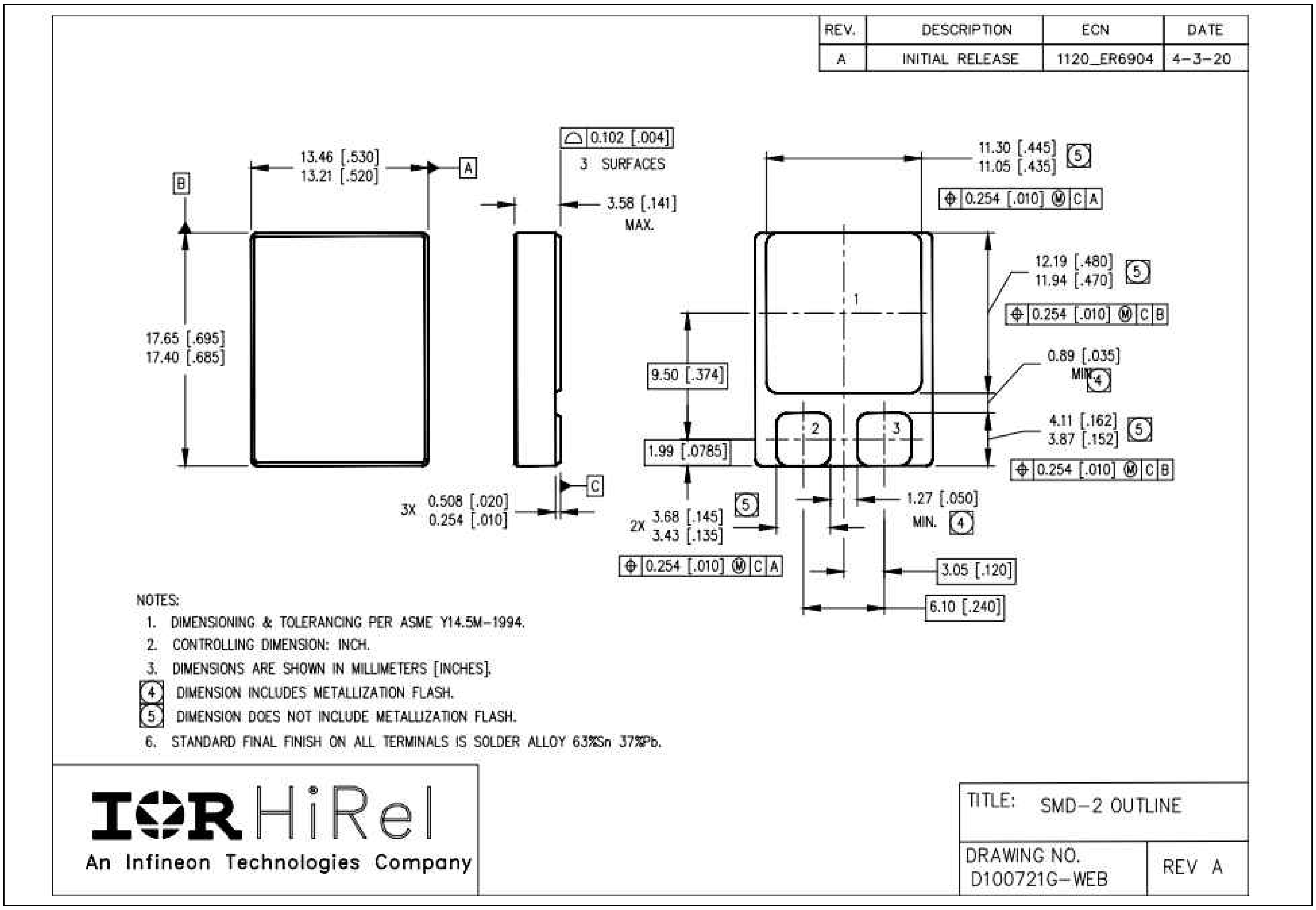

Figure 15 **SMD-2 outline drawing (See IR HiRel website)**

Existing solutions

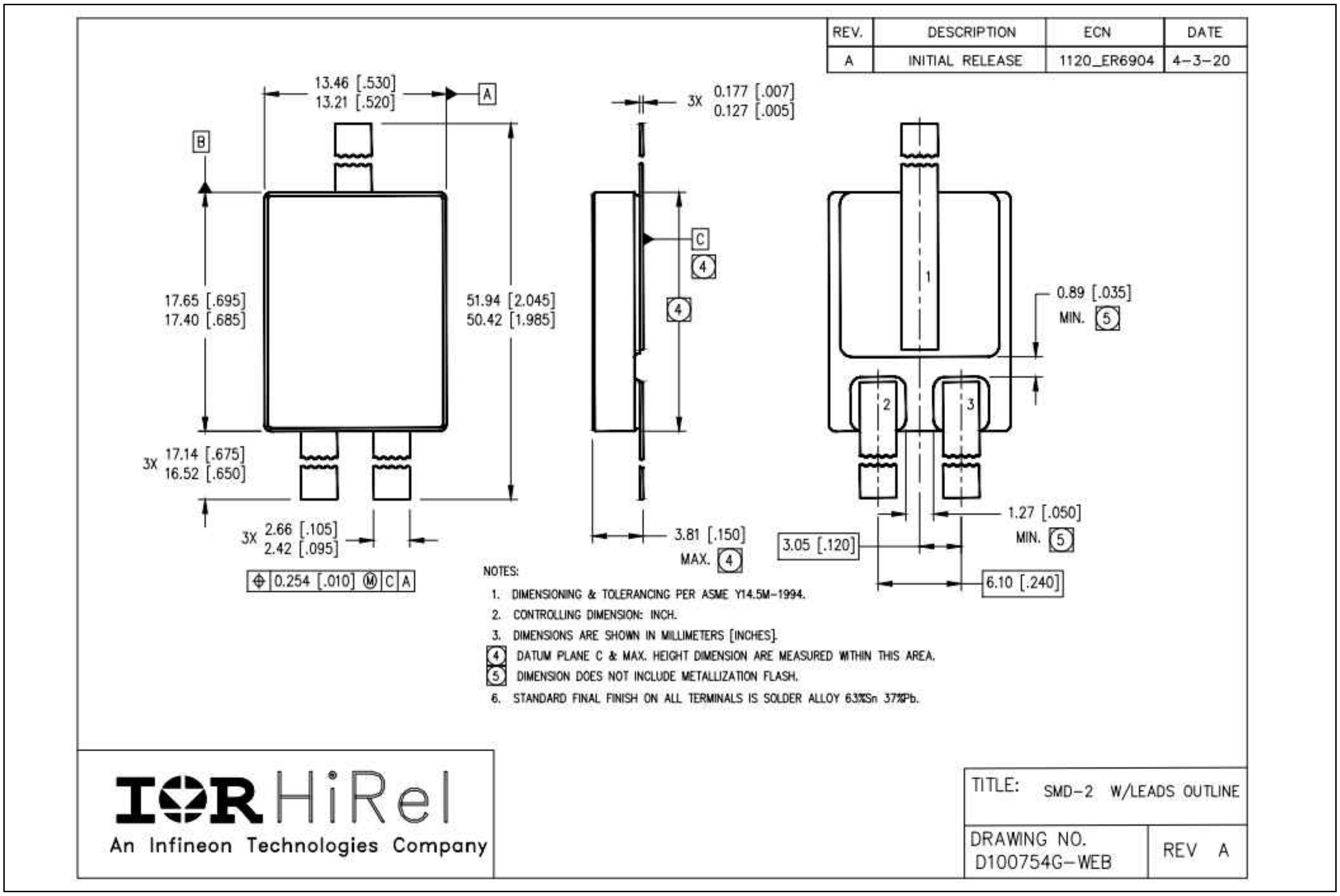

Figure 16 **SMD-2 with leads, outline drawing (See IR HiRel website)**

Existing solutions

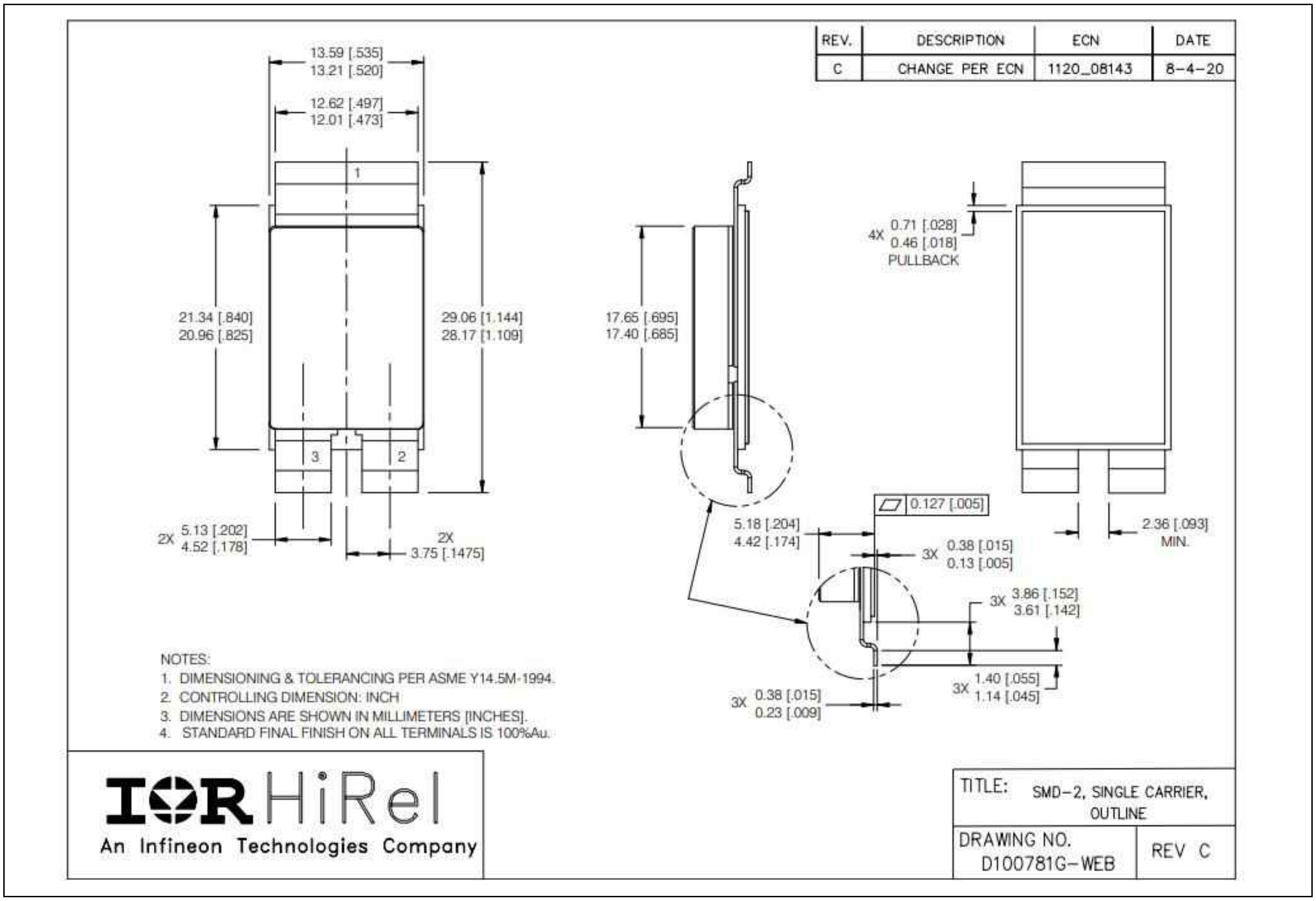

Figure 17 **SMD-2 on carrier, outline drawing (See IR HiRel website)**

4 The SupIR-SMD: a better solution

Adding ribbon leads to the SMD packages and then providing carriers for the larger SMDs allows for solutions to the problem of thermal expansion mismatch, but the inherent problem lies at the terminal interface between the part and the solder pads of the circuit board. IR HiRel has re-designed the package itself in order to achieve a better solution for thermal expansion and for heat transfer.

In order to solve the stress cracking problem caused by the large CTE mismatch between power package and circuit board, and minimize the thermal and electrical resistance as well, IR HiRel adopted a package design with a multiple layer base as shown in Figure 18. In this design, the base has two layers, the layer that connects the ceramic body has a CTE that matches the ceramic CTE, and the layer that connects the circuit board has a CTE value between those of first layer and circuit board. In this way, the CTE changes gradually from ceramic to PCB and thus reduces the stress from a large CTE mismatch. The idea was patented (US patent #9,559,026 [1]) by Infineon Technologies, the parent company of IR HiRel. The new design concept and the dimensioned drawing of the design are shown in Figure 19 and Figure 20, respectively.

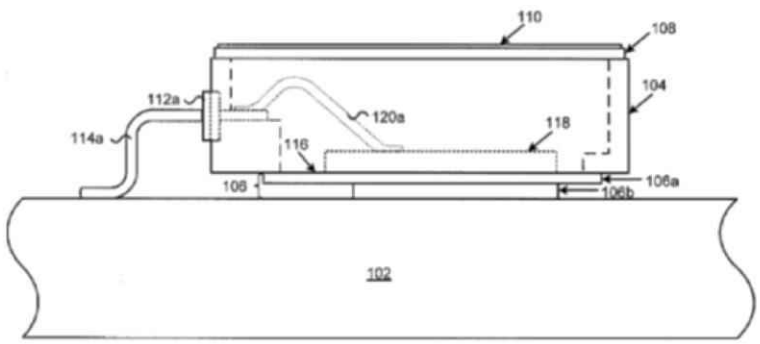

Figure 18 The SupIR-SMD, a new design concept (cutaway view showing chip and wirebond inside)

The new SupIR-SMD incorporates the stress relief of wide, flat leads with a curved structure and the more direct thermal path through the bottom of the part where the die is mounted. A picture of the SupIR-SMD is shown in Figure 19, with a detailed drawing [11] shown in Figure 20.

The SupIR-SMD: a better solution

Figure 19 SupIR-SMD package

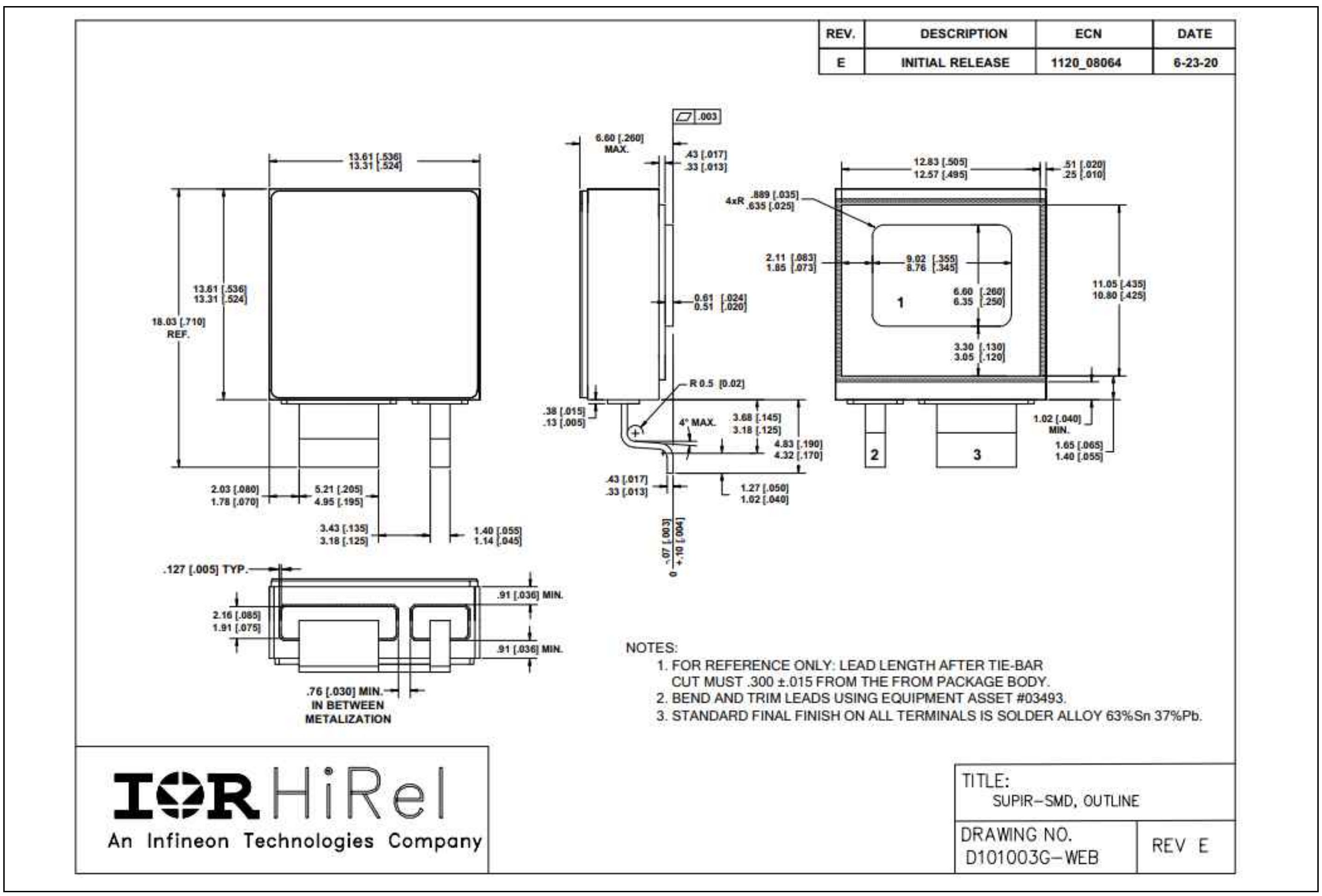

Figure 20 SupIR-SMD, outline drawing (See IR HiRel website)

The SupIR-SMD: a better solution

The reduction in size of the SupIR-SMD to the SMD-2 on carrier is detailed in Figure 21, showing a reduction of about one third in the total footprint of the part on a PCB.

Figure 21 Comparison of SupIR-SMD dimensions to SMD-2 on carrier

This package will hold devices which will be JANS qualified in accordance with MIL-PRF-19500, the quality and reliability level required (in general) for Space applications. The new design offers improved physical performance parameters (thermal expansion performance non-withstanding) compared to the nearest packaging solutions, the IR SMD-2 package with a carrier. The SupIR-SMD is

- 35% smaller: 0.376 in^2 vs. 0.583 in^2,
- 45% lighter: 2.8 g vs. 5.1 g, and
- lower in thermal resistance by 0.25°C/W

In point of fact, the new package also offers features that are often desired in highly reliable circuit applications: the structure of the device allows for visual inspect on the side of the solder joint, and the flux residual can be more easily removed than in the standard SMD package. An example of the successful implementation of the SupIR-SMD is pictured in Figure 22, which shows the parts as used on the IR HiRel ZAN-series converter, in this particular instance a 28V input, 5V output, operating at 92% efficiency through the use of synchronous rectification (SupIR-SMD and SMD-0.2 shown).

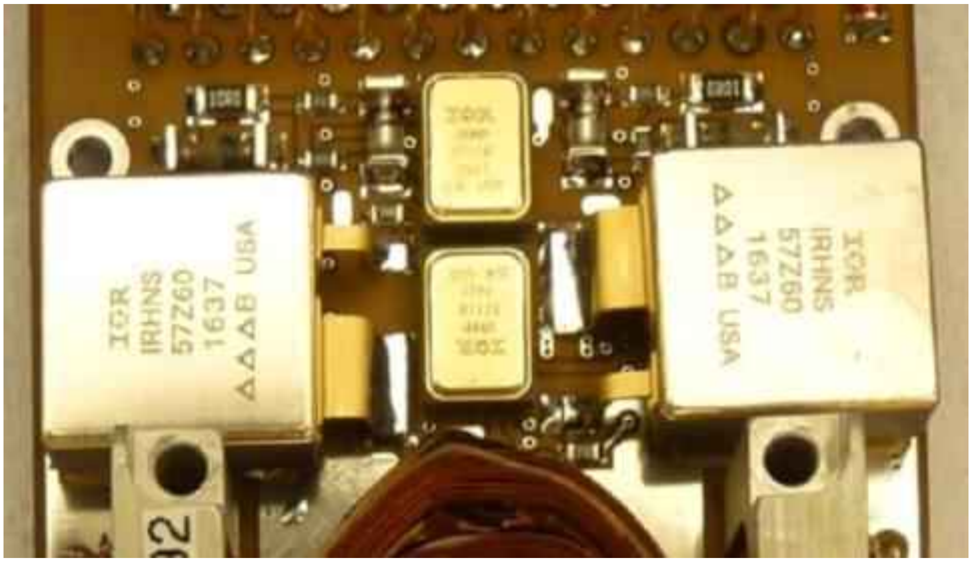

Figure 22 SupIR_SMD as used on IR HiRel ZAN-series converters

Finite Element Analysis was used to create and evaluate different designs and finalize the new design. The key figure of merit is the ceramic stress, which was calculated to be at a maximum level in the package of 104 MPa when mounted on a PCB, which is much lower than the stress limit for tensile strength of the material at ~220 MPa. Stress levels in the FEA correlated very well with package performance in the board level test assemblies during the design iteration phase of the SupIR-SMD. An example of the FEA is shown in Figure 23.

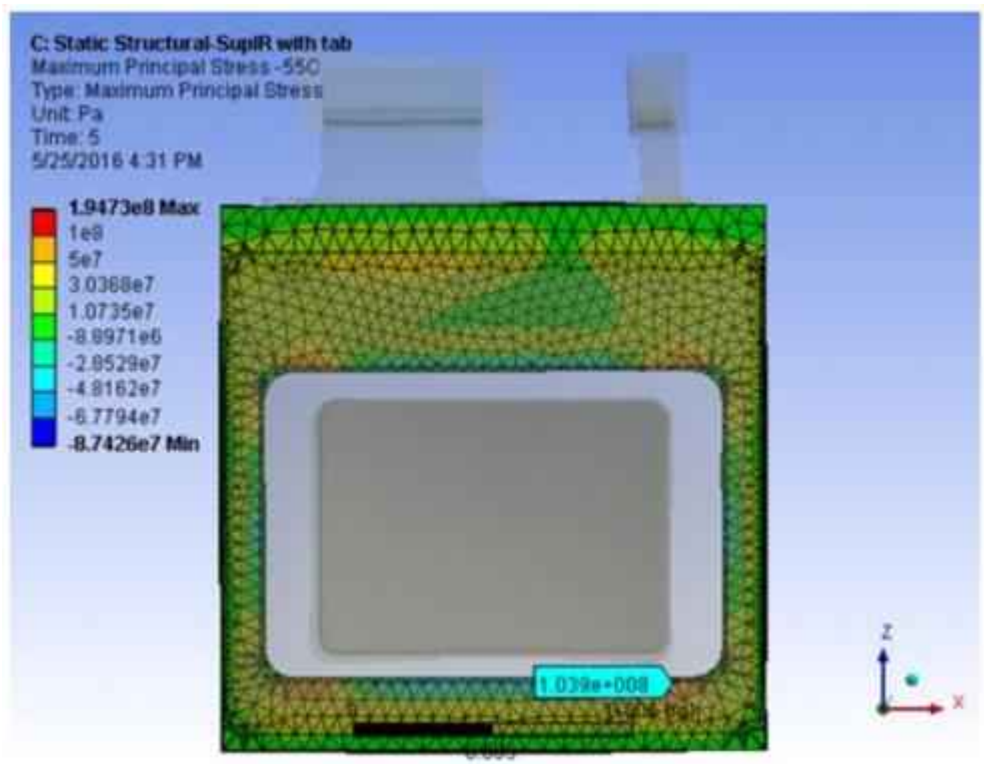

Figure 23 SupIR-SMD FEA model results

5 Qualification testing

To qualify the new package on a representative PCB, the SupIR-SMD was mounted in various orientations and positions on a printed circuit board. This board was then subjected to thermal cycling, random vibration, and mechanical shock. To verify the efficacy of the FEA analysis and package design, some parts were then removed from the PCB for fine and gross leak, and the others were cross sectioned for detailed examination of the solder joints and package integrity. The combination of the leak tests and the cross sections were to establish conclusive suitability of the SupIR-SMD to remain free of any cracks formed under these demanding thermal and mechanical conditions.

The details of the test are as follows. First, the board-level assemblies were subjected to thermal cycling. Temperature cycling was performed in according with MIL-STD-750F, Method 1051 [12], with some additional constraints. This test applied 500 temperature cycles from -55°C to 100°C with a minimum 10°C/minute ramp and a 15 minute dwell time. Checks were performed after these thermal cycles and the qualification continued without any failure through the next stage of mechanical stresses.

The next step in qualification was to take these board assemblies and test them with respect to Random Vibration in accordance with MIL-STD-883J with Change 5 [13], Method 2026, Condition 1J. Figure 24 shows a picture of the setup (Z-axis example shown) for the random vibration test with multiple SupIR-SMD's on the board. As per the standard, the SupIR-SMD assemblies were vibrated in three dimensions, to a level of 36.6 rms G's for 15 minutes (each dimension). The package was also tested for Mechanical Shock to 1500 G's, in accordance with Method 2002.5, Condition B of the same standard. That means that the assemblies saw (at least) 1500 G's peak for half a millisecond, and this was done five times in each axis.

Figure 24 Z-axis random vibration setup

The measured profile of the random vibration forces is shown in Figure 25 (Z-axis example given). All three axis were tested, but only one is shown for the sake of clarity.

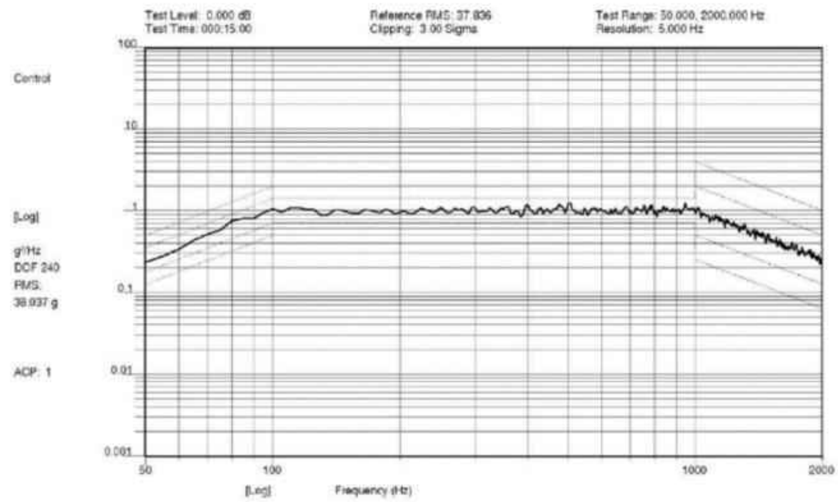

Figure 25 Measured vibration profile for z-axis

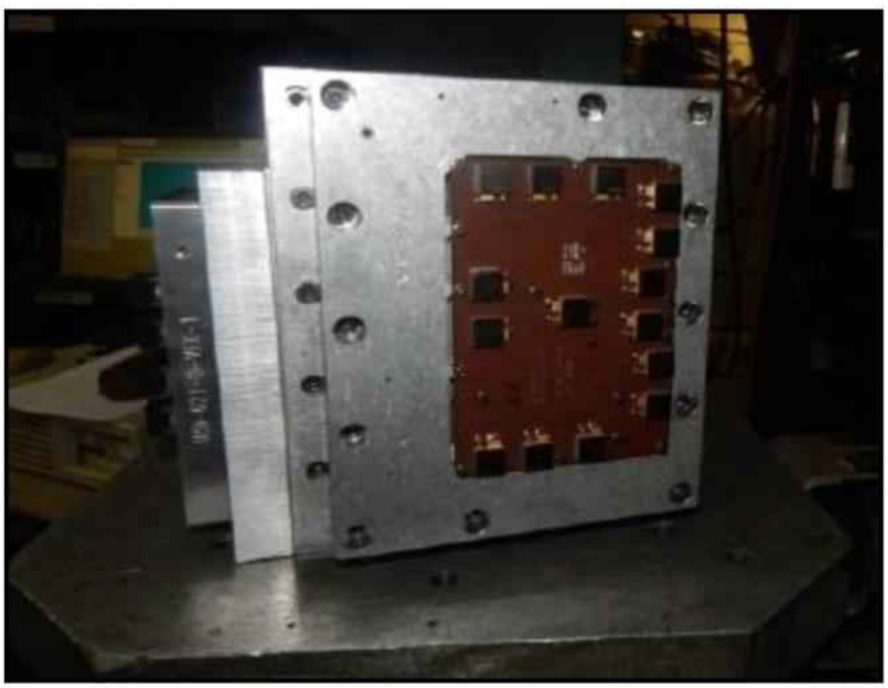

Figure 26 Y-axis mechanical shock setup

For the example Y-axis setup shown in Figure 25, the measured mechanical shock is shown in Figure 27. All axes and orientations were tested and measured.

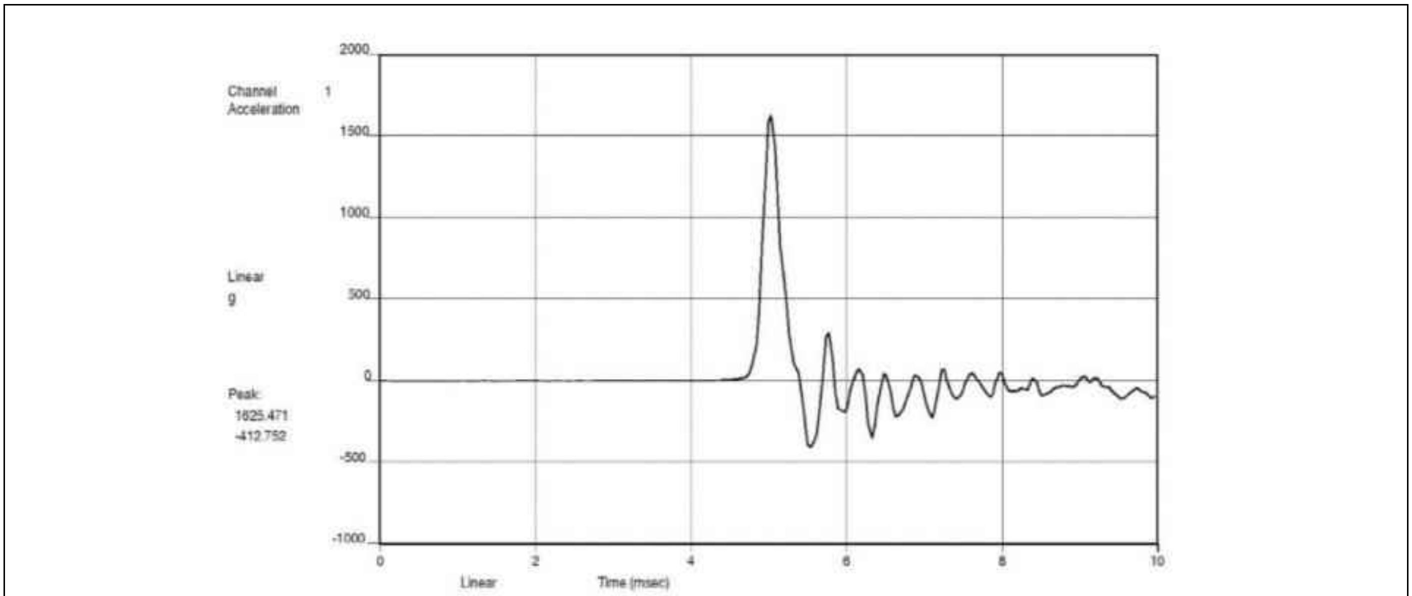

Figure 27 Measured y-axis mechanical shock

6 Results of qualification

The end results of these sequential qualification test results are described in this section. First, fine and gross leak measurements were made in accordance with MIL-STD-750F, Method 1071 [9]. These measurements were taken on SupIR-SMD parts that had been removed from the board, and all of these parts passed the test, whose purpose is to verify the integrity of the package itself.

Sample parts (still soldered to the test board) were then cross sectioned to be inspected under higher optical magnification. Those parts and cross sections are shown in Figure 28 through Figure 37.

Figure 28 SupIR-SMD, front view

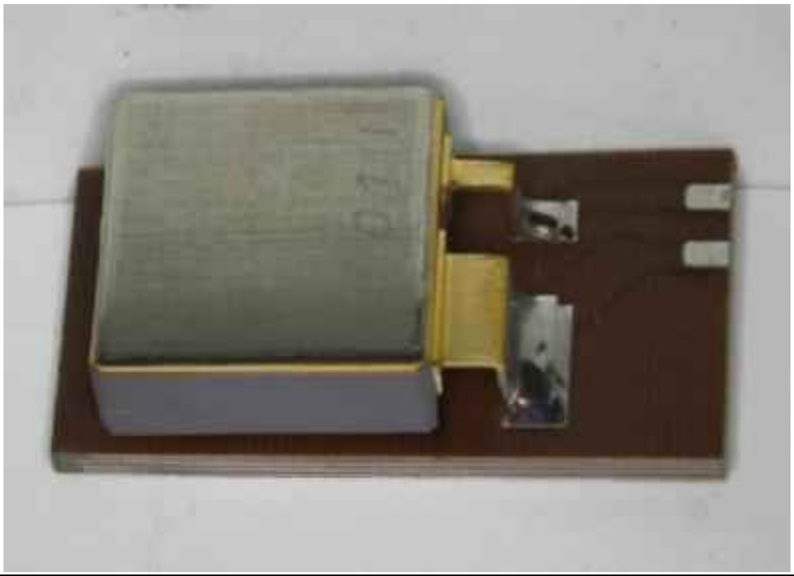

Figure 29 SupIR-SMD, side view

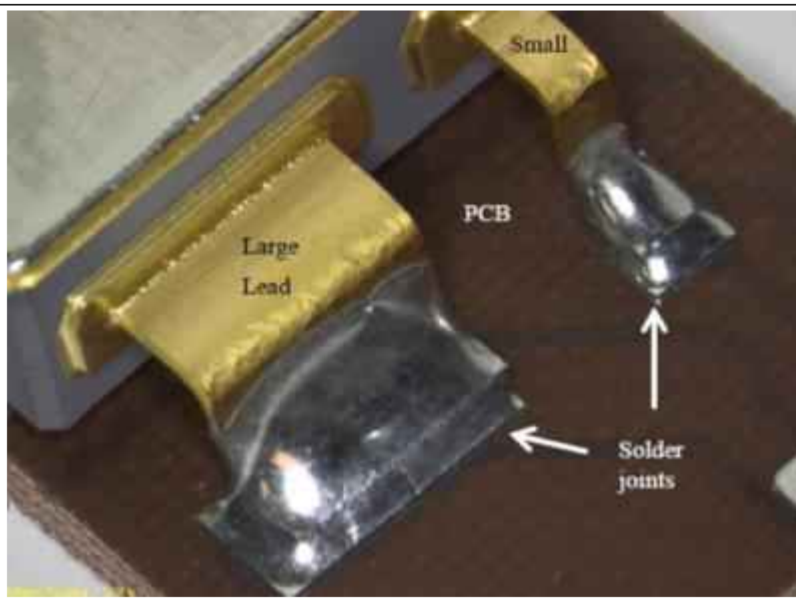

Figure 30 SupIR-SMD, close-up view of joints

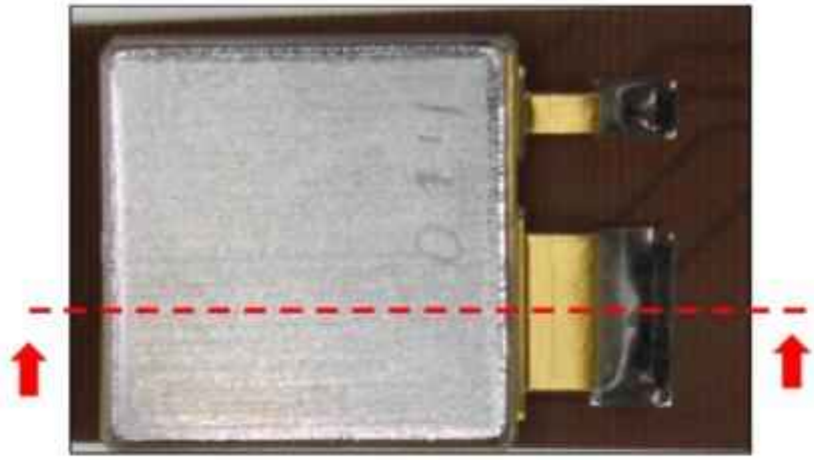

Figure 31 Cross section plane and direction of cut, large lead

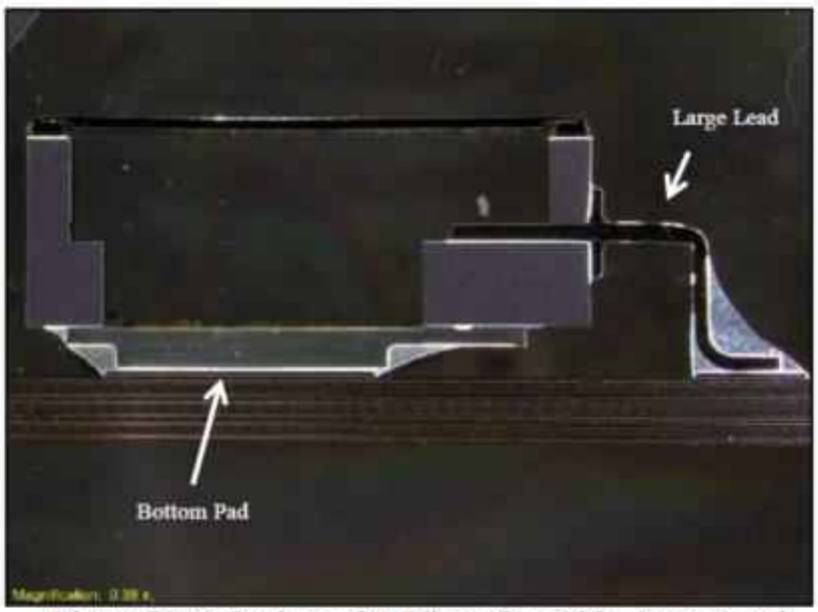

Figure VI-5: Package Cut View, One Side, Large Lead

Figure 32 Package cut view, one side, large lead

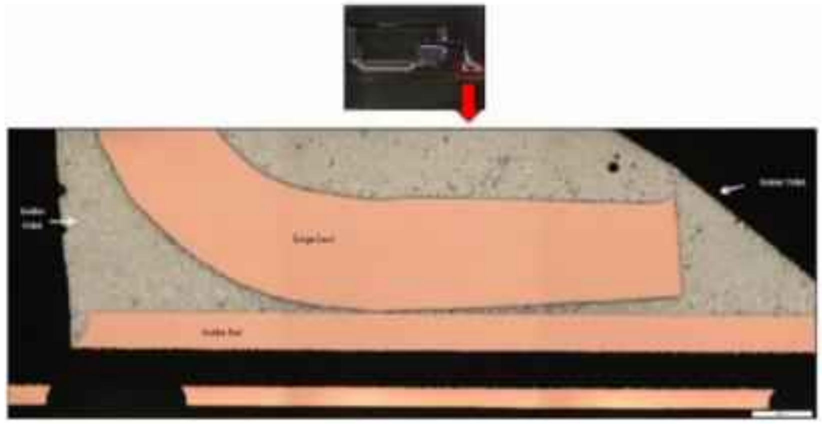

Figure 33 Cross section of large lead

In Figure 33, the cross section of the solder attached fillet on the large leads appears normal with minimal voiding. In Figure 34, the cross section of the pad also appears equally intact.

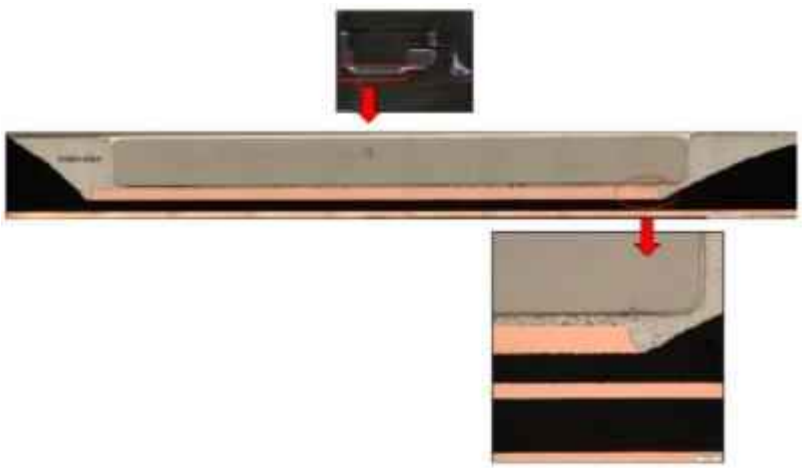

Figure 34 Cross section of pad in-plane with large lead

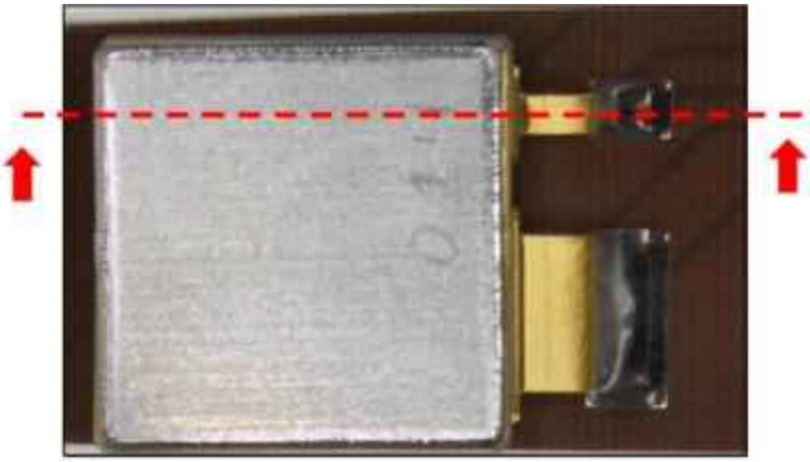

Figure 35 Cross section plane and direction of cut, small lead

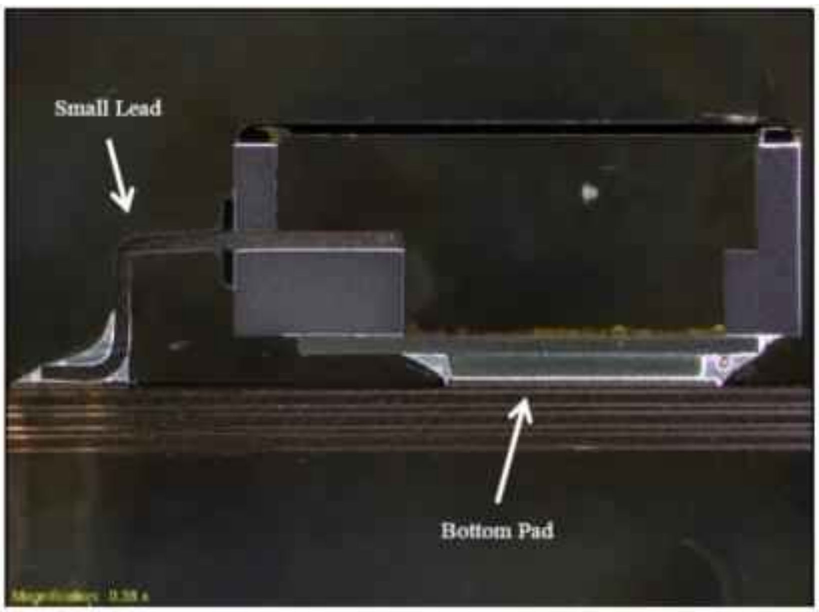

Figure 36 Package cut view, one side, small lead

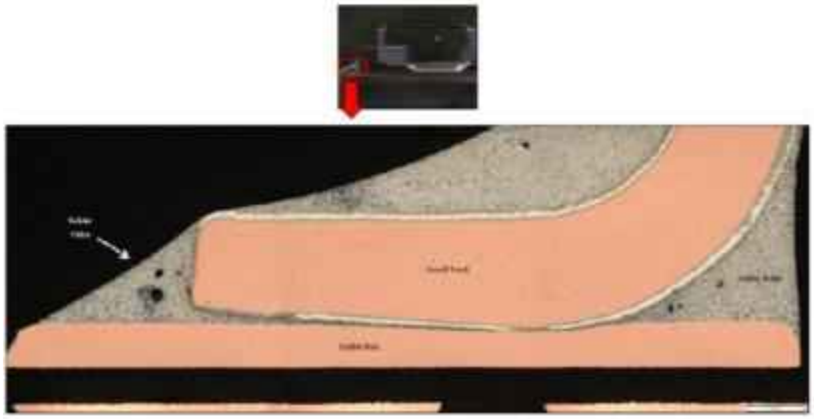

Figure 37 Cross section of small lead

Again, the small lead cross section appears to be in excellent shape with no cracks.

7 Application

The application of the SupIR-SMD is fairly straightforward. It is to be assembled on printed circuit board just as with any other surface mount device. It works well with most common PCB types in industry, for example, FR-4 and polyimide. The most common solder for surface mount of the package is lead-tin eutectic solder (Sn63Pb37). Suggested solder pads for PCB layout used are shown in Figure 38. These pad layouts work well for us, and customers are invited to use these as well. If there are special, customer-driven requirements for PCB assembly or other guidelines required for any given application, those should be considered in any layout with the SupIR-SMD.

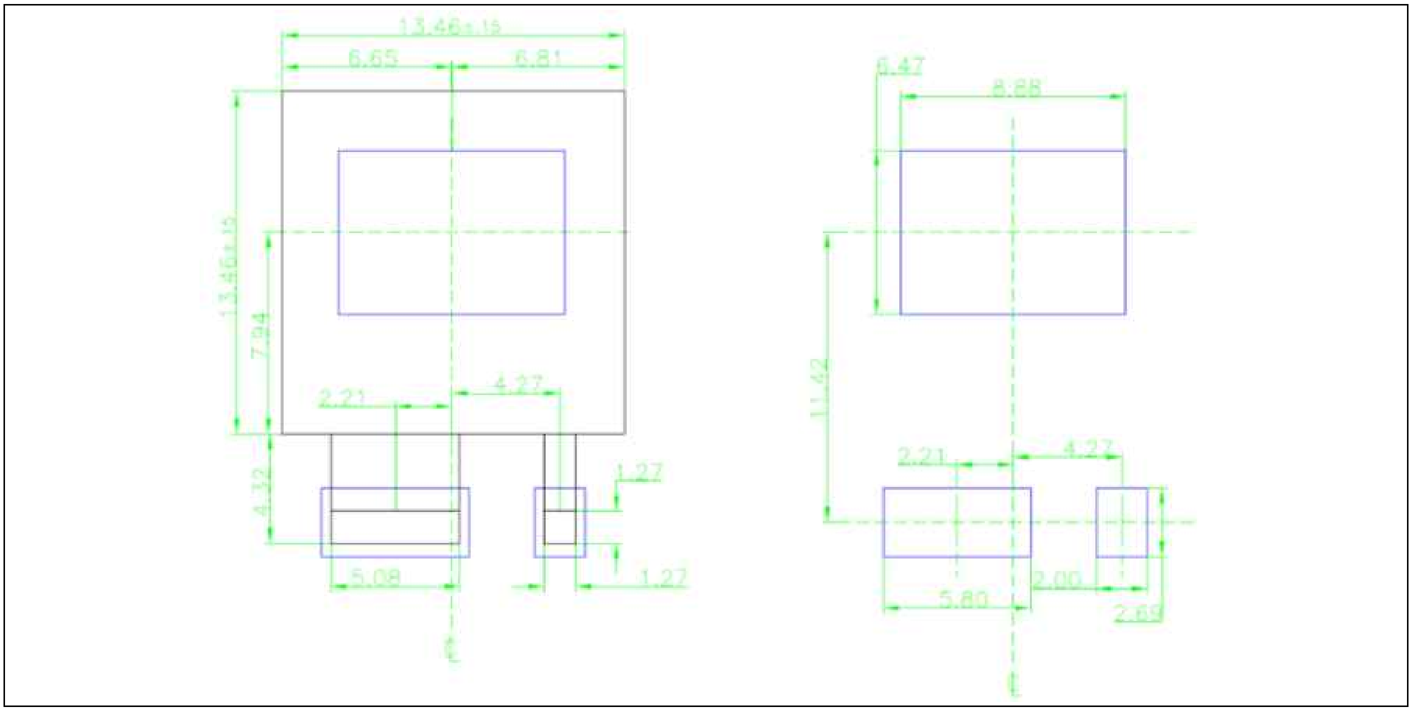

Figure 38 SupIR-SMD nominal, suggested solder pads (dimensions in mm)

The cleaning of solder flux residual is also easy. The two leads are visible and accessible, and the pedestal raises up the package to give a clearance of at least 20 mils between the package and PCB. This aids the process of using cleaning fluid or vapor to carry away solder flux residual completely, which increases the reliability of the solder joint and the device.

The product nomenclature for SupIR-SMD MOSFET devices starts with “IRHNS”. There are diodes offered with this technology as well, with a package designation of “NS” in the product nomenclature.

The early adopters of the SupIR-SMD have been satisfied with the performance of this package platform. As one of the customers put it: “The new SupIR offering has opened up our design to a product that can move more power with better reliability and lower manufacturing cost.”

8 Conclusions

The extensive test results show that the new SupIR-SMD package has an excellent ability to withstand thermal expansion difference between package and printed circuit board, maintaining the hermetic integrity of the package as well as the solder joint from the part to a printed circuit board. In comparison to the prior art, this new package also allows for a significantly reduced footprint on the board, reduced weight, and a more direct thermal path for heat transfer. Specific details on each part offered in this package can be found in the parts' respective product datasheets on the Infineon web site for IR HiRel: www.infineon.com/irhirel.

9 References

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Revision history

Document version	Date of release	Description of changes
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1.1	2020-10-05	Update to latest document template, package figures

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