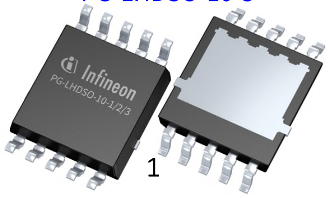
Automotive MOSFET

OptiMOS™ 6 Power-Transistor

PG-LHDSO-10-3



Features

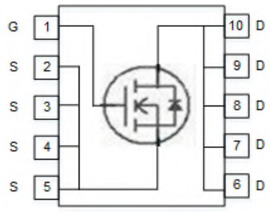
- OptiMOS™ power MOSFET for automotive applications
- N-channel – Enhancement mode – Normal Level
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- RoHS compliant
- 100% Avalanche tested
- Top Side Cooling

Potential applications

General automotive applications.

Product validation

Qualified for automotive applications. Product validation according to AEC-Q101.



Pins 10 - 6 & Tab on Drain

Product Summary

V_{DS}	40	V
$R_{DS(on)}$	0.75	mΩ
I_D (chip limited)	390	A

Type	**Package**	**Marking**
IAUCN04S6N007T	PG-LHDSO-10-3	6A4

Table of Contents

Maximum ratings

at Tj=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	V_{GS}=10 V, Chip limitation[1,2]	390	A
		V_{GS}=10V, DC current	120	
		T_a=85 °C, V_{GS}=10 V, R_{thJH} on 2s2p[2,4]	95	
Pulsed drain current[2]	$I_{D,pulse}$	T_C=25 °C, t_p= 100 µs	1300	
Avalanche energy, single pulse[2]	E_{AS}	I_D=60 A	624	mJ
Avalanche current, single pulse	I_{AS}	–	115	A
Gate source voltage	V_{GS}	–	±20	V
Power dissipation	P_{tot}	T_C=25 °C	206	W
Operating and storage temperature	T_j, T_{stg}	–	-55 ... +175	°C

Thermal characteristics[2)]

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal resistance, junction - case	R_{thJC}	–	–	0.36	0.73	K/W
Thermal characterization parameter, source pin[5)]	Ψ_{source}		–	5.3	–	
Thermal characterization parameter, drain pin[6)]	Ψ_{drain}		–	5.4	–	
Thermal resistance, junction - heatsink[4)]	R_{thJH}		–	6.8	–	
Thermal resistance, junction - ambient[3)]	R_{thJA}	–	–	45	–	

Electrical characteristics

at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Static characteristics						
Drain-source breakdown voltage	$V_{(Br)DSS}$	V_{GS}=0 V, I_D=1 mA	40	–	–	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=120 µA	2.2	2.6	3.0	
Zero gate voltage drain current	I_{DSS}	V_{DS}=40 V, V_{GS}=0 V, T_j=25 °C	–	–	1	µA
		V_{DS}=40 V, V_{GS}=0 V, T_j=125 °C[2)]	–	–	30	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	–	–	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=7 V, I_D=60 A	–	0.81	0.95	mΩ
		V_{GS}=10 V, I_D=60 A	–	0.68	0.75	
Gate resistance[2)]	R_G	–	–	0.97	–	Ω

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics[2)]						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=25 V, f=1 MHz	–	6950	9035	pF
Output capacitance	C_{oss}		–	2100	2730	
Reverse transfer capacitance	C_{rss}		–	98	147	
Turn-on delay time	$t_{d(on)}$	V_{DD}=20 V, V_{GS}=10 V, I_D=120 A, R_G=3.5 Ω	–	12	–	ns
Rise time	t_r		–	7	–	
Turn-off delay time	$t_{d(off)}$		–	33	–	
Fall time	t_f		–	15	–	

Parameter	Symbol	Conditions	min.	typ.	max.	Unit
Gate Charge Characteristics[2)]						
Gate to source charge	Q_{gs}	V_{DD}=32 V, I_D=120 A, V_{GS}=0 to 10 V	–	26	34	nC
Gate to drain charge	Q_{gd}		–	19	29	
Gate charge total	Q_g		–	100	130	
Gate plateau voltage	$V_{plateau}$		–	3.9	–	V

Parameter	Symbol	Conditions	min.	typ.	max.	Unit
Reverse Diode						
Diode continous forward current[2)]	I_S	T_C=25 °C	–	–	120	A
Diode pulse current[2)]	$I_{S,pulse}$	T_C=25 °C, t_p= 100 µs	–	–	1300	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=60 A, T_j=25 °C	–	0.8	1.1	V
Reverse recovery time[2)]	t_{rr}	V_R=20 V, I_F=50 A, di_F/dt=100 A/µs	–	46	–	ns
Reverse recovery charge[2)]	Q_{rr}		–	42	–	nC

1) Practically the current is limited by the overall system design including the customer-specific PCB.

2) The parameter is not subject to production testing – specified by design.

3) Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7) without thermal vias. PCB is vertical in still air.

4) Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7) without thermal vias, heatsink of 71x110x2 mm is attached through TIM with 3.3 W/(m*K) and 400µm thickness to top side pad. Heatsink fixed to 85°C ambient temperature.

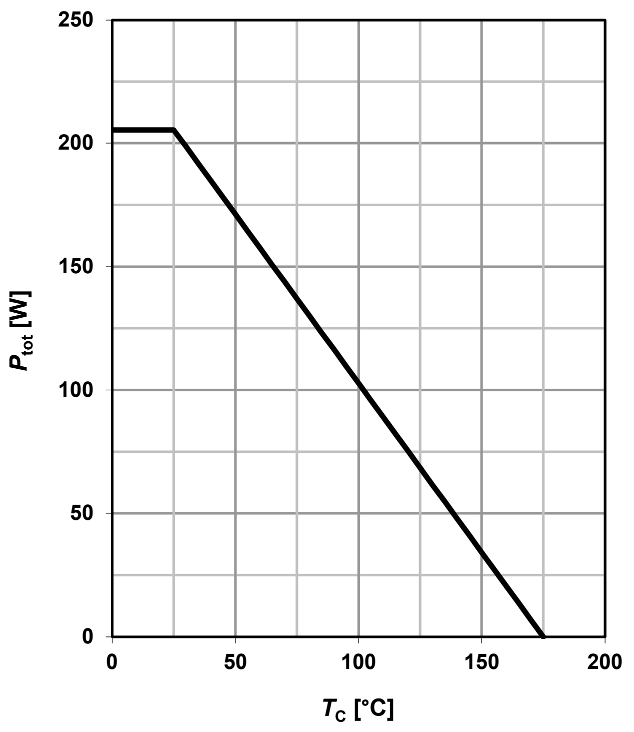
5) Thermal characterization parameter, calculated as $\psi_{source} = (T_{source} - T_{ambient})/P_{dis}$ in condition of 4). Used to determine PCB temperature at source pins for given power.

6) Thermal characterization parameter, calculated as $\psi_{drain} = (T_{drain} - T_{ambient})/P_{dis}$ in condition of 4). Used to determine PCB temperature at drain pins for given power.

Electrical characteristics diagrams

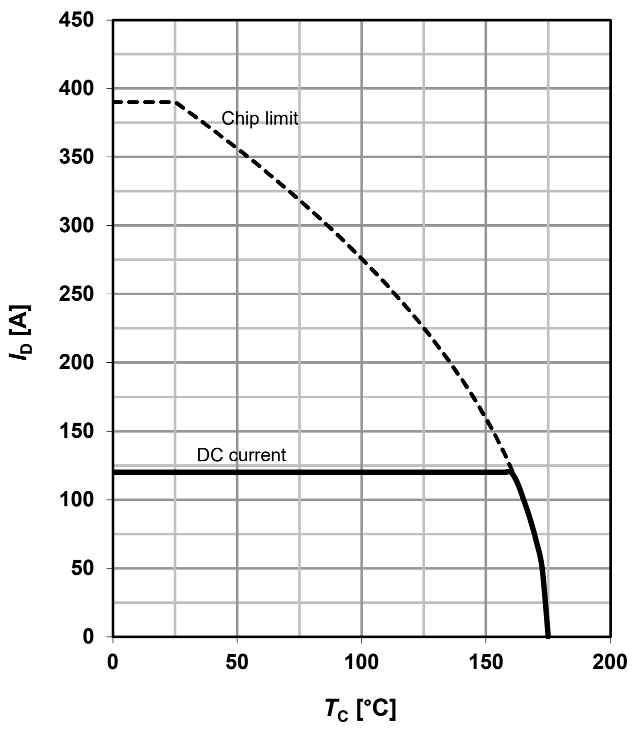
1 Power dissipation

$P_{tot} = f(T_C)$; $V_{GS} \geq 6$ V



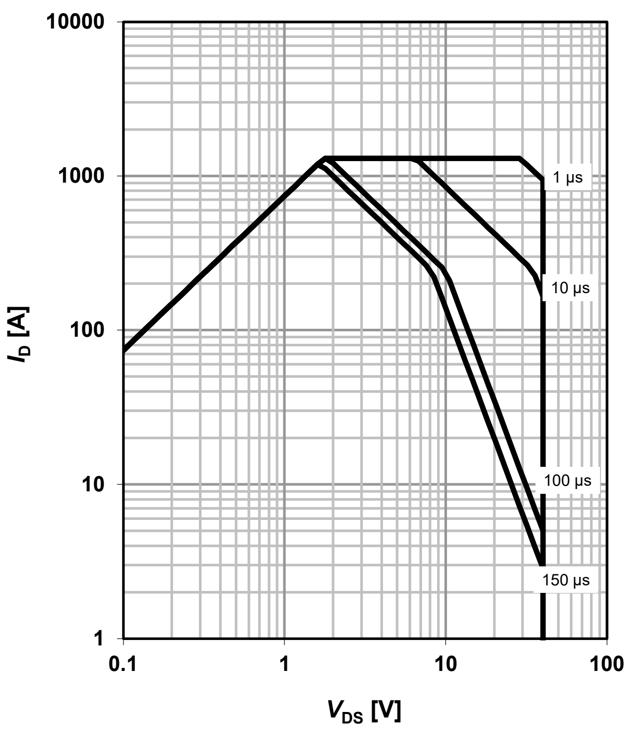
2 Drain current

$I_D = f(T_C)$; $V_{GS} \geq 6$ V



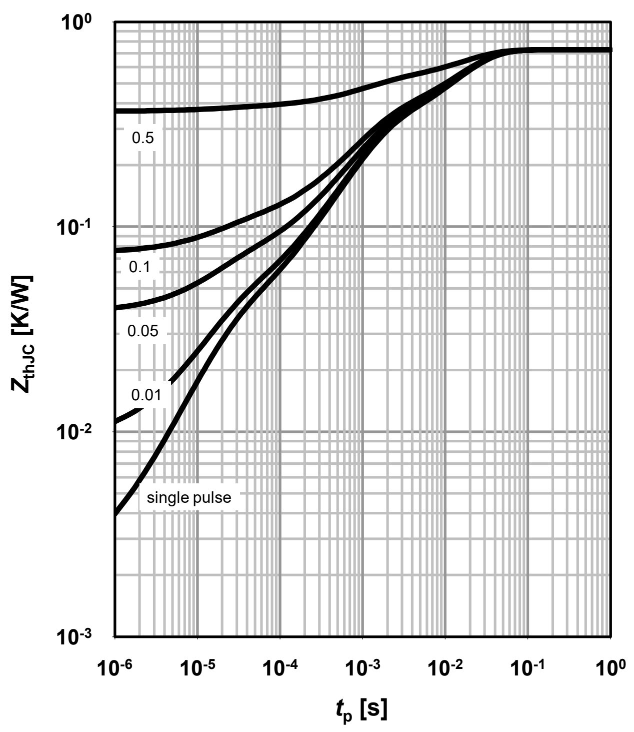
3 Safe operating area

$I_D = f(V_{DS})$; $T_C = 25$ °C; $D = 0$; parameter: t_p



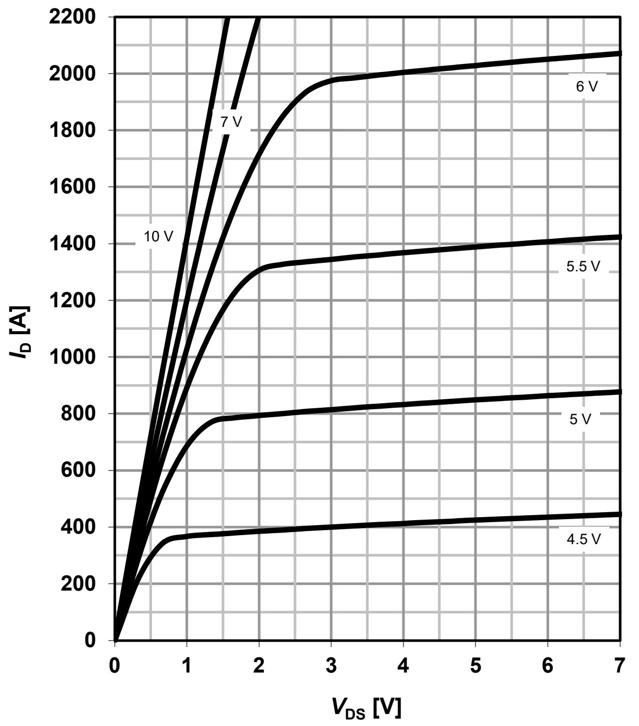
4 Max. transient thermal impedance

$Z_{thJC} = f(t_p)$; parameter: $D = t_p/T$



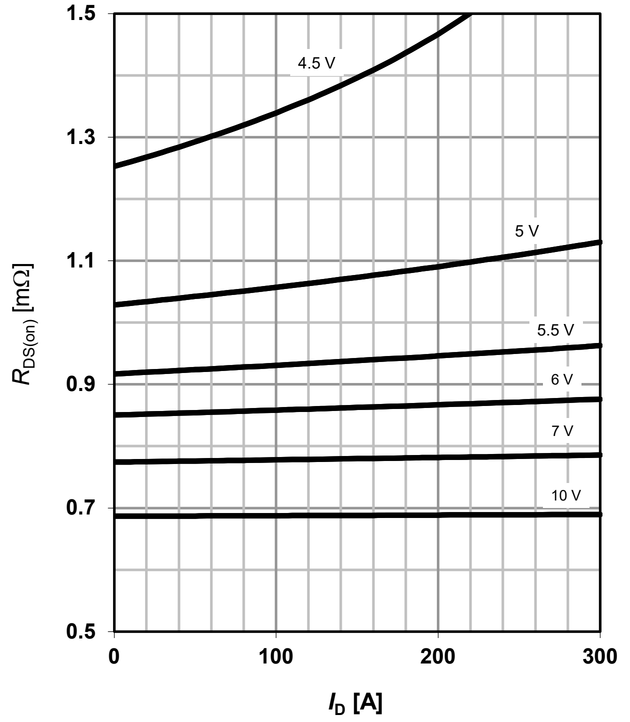
5 Typ. output characteristics

$I_D = f(V_{DS})$; $T_j = 25$ °C; parameter: V_{GS}



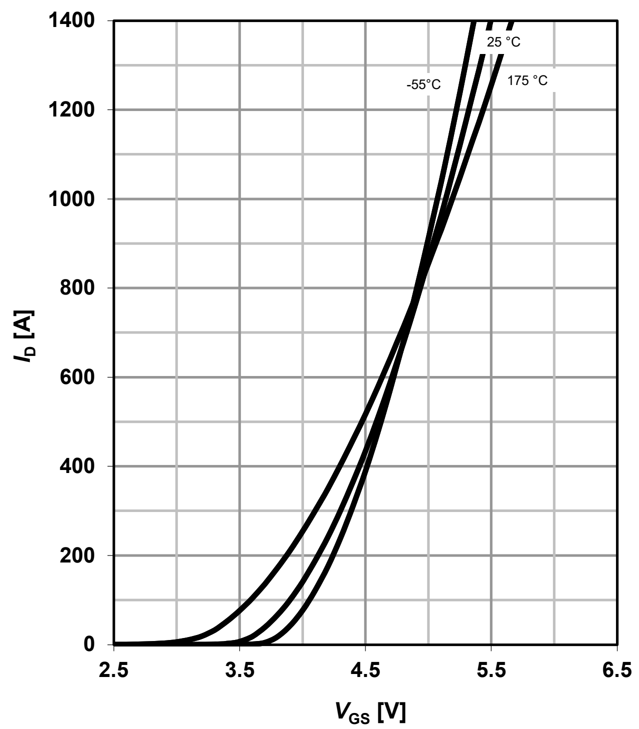
6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D)$; $T_j = 25$ °C; parameter: V_{GS}



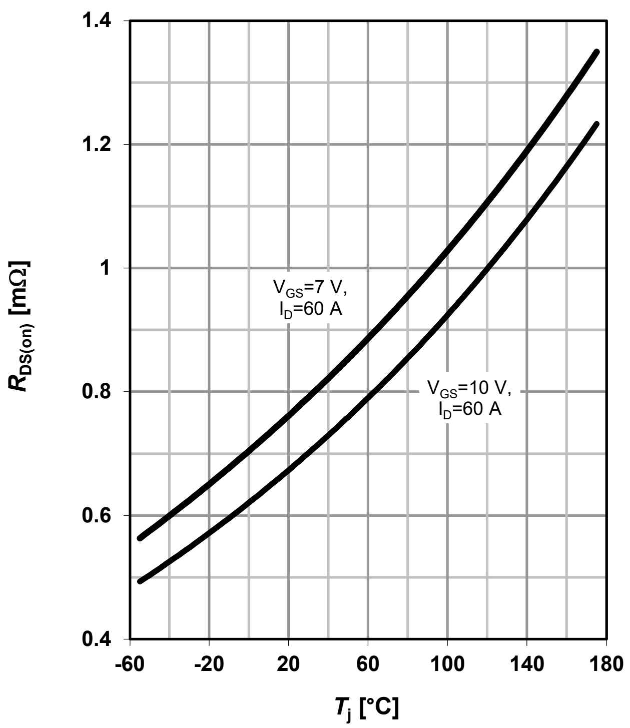
7 Typ. transfer characteristics

$I_D = f(V_{GS})$; $V_{DS} = 6$ V: parameter: T_j

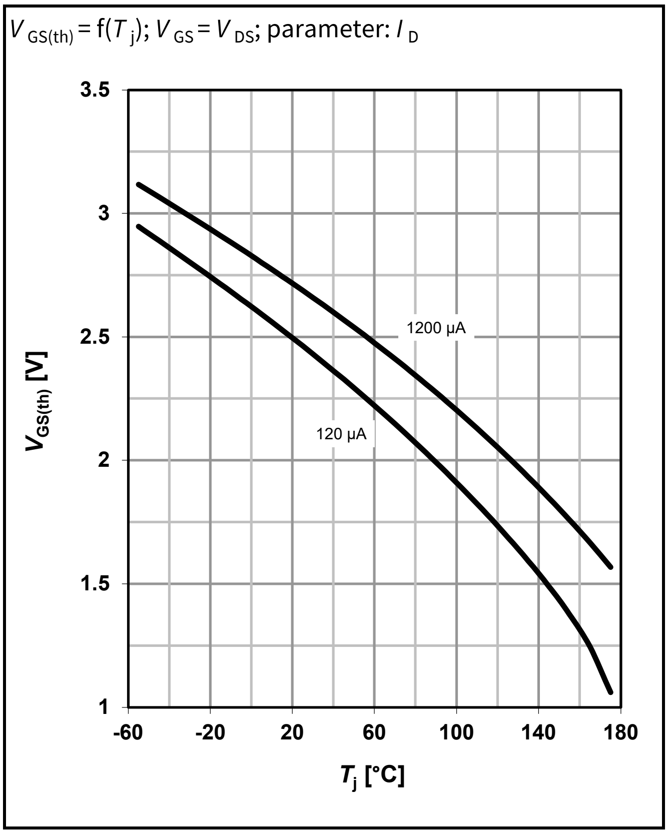


8 Typ. drain-source on-state resistance

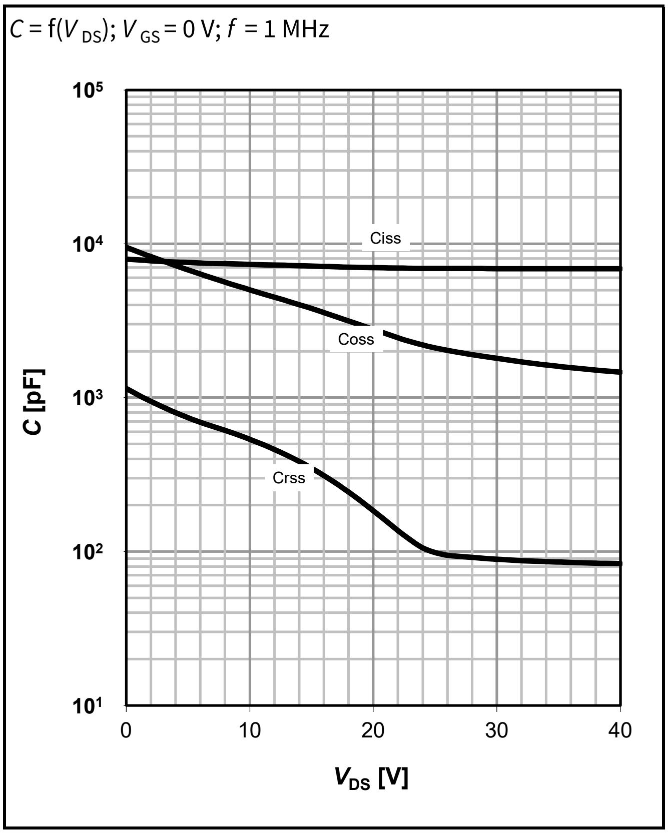
$R_{DS(on)} = f(T_j)$; parameter: I_D, V_{GS}



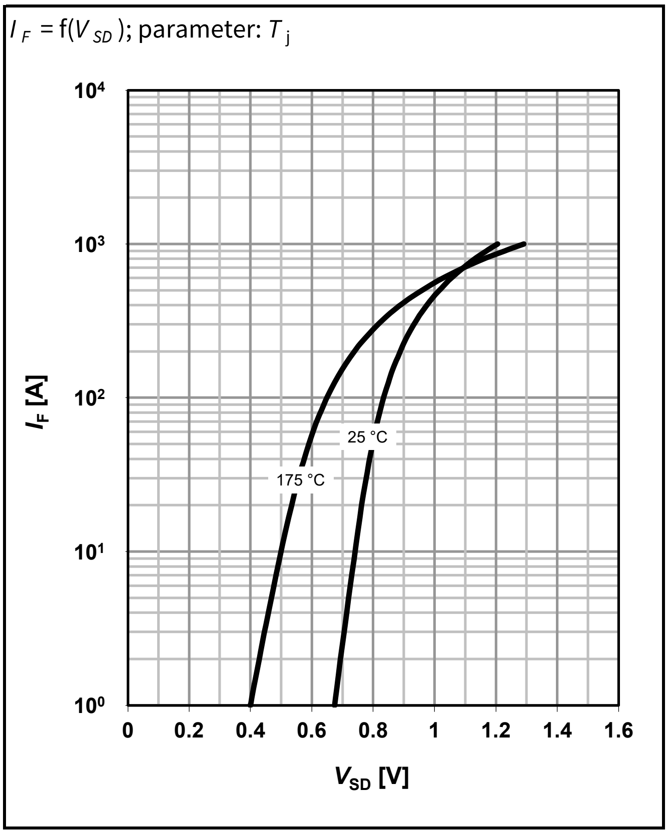
9 Typ. gate threshold voltage



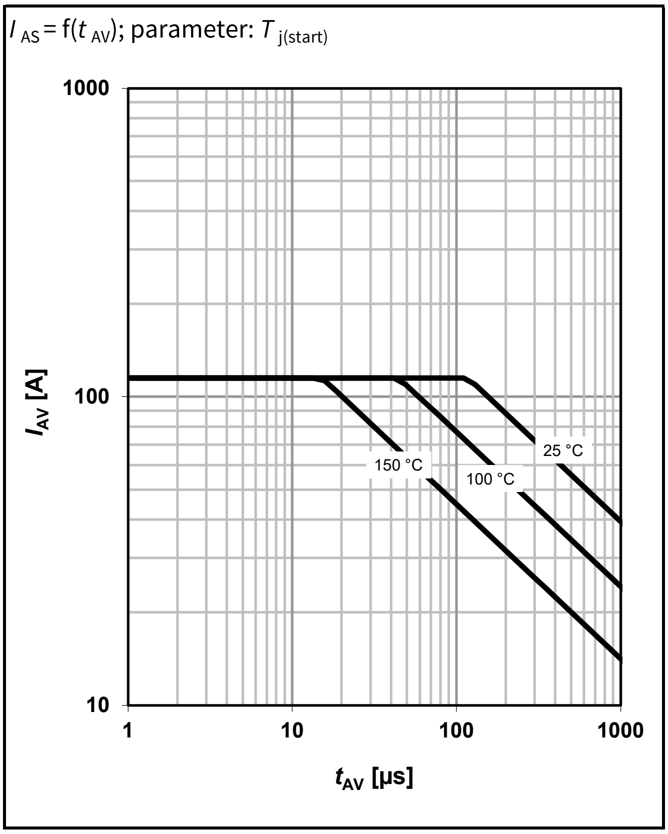
10 Typ. capacitances



11 Typical forward diode characteristics

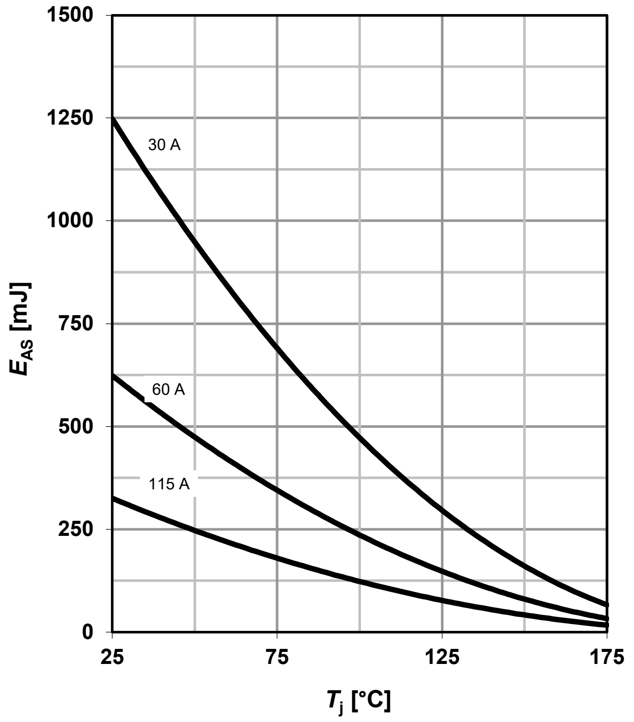


12 Typ. avalanche characteristics



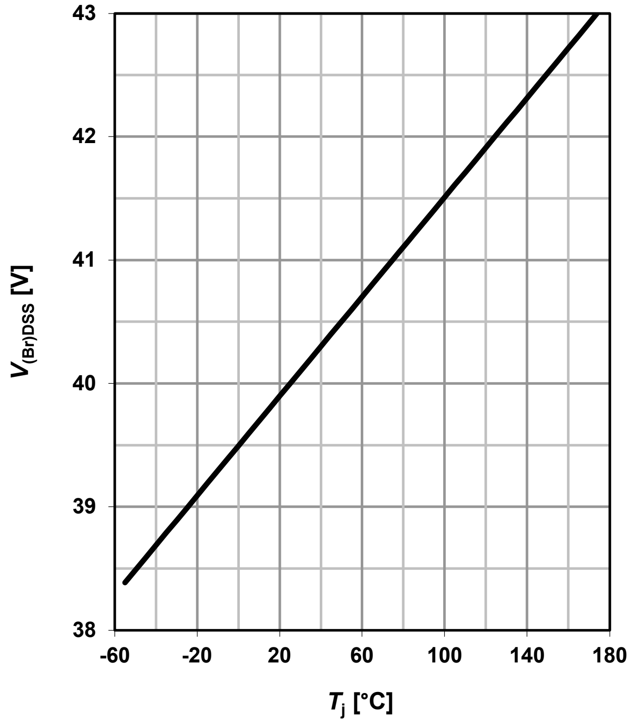
13 Typical avalanche energy

$E_{AS} = f(T_j)$; parameter: I_D



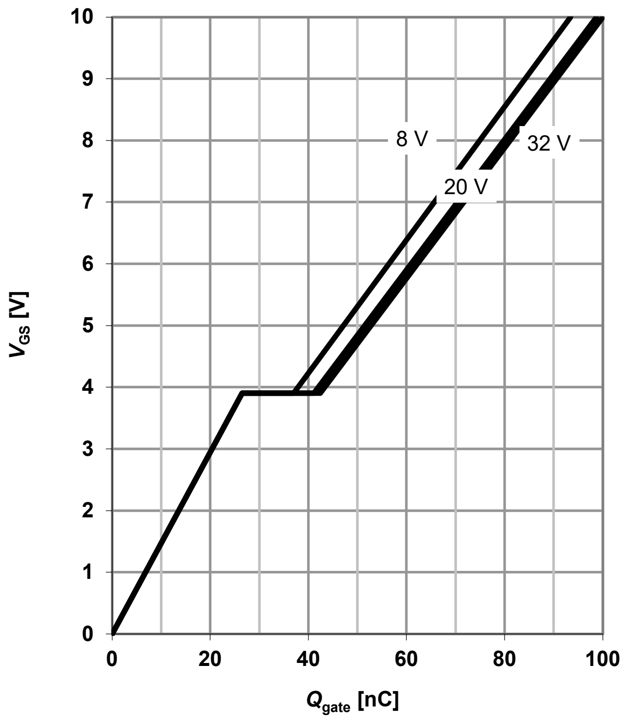
14 Drain-source breakdown voltage

$V_{(Br)DSS} = f(T_j)$; $I_{D\_typ} = 1$ mA

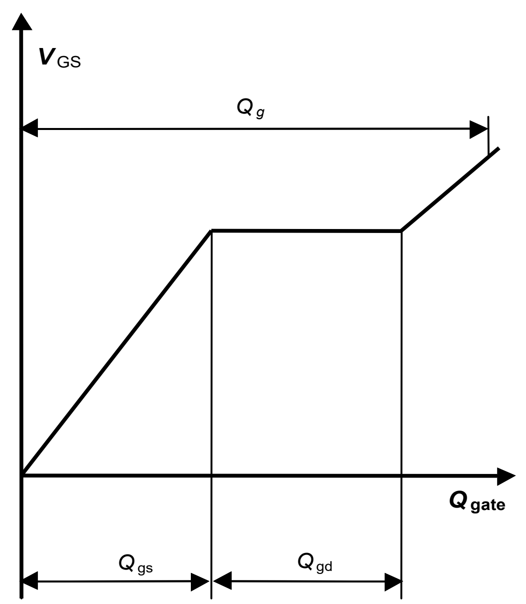


15 Typ. gate charge

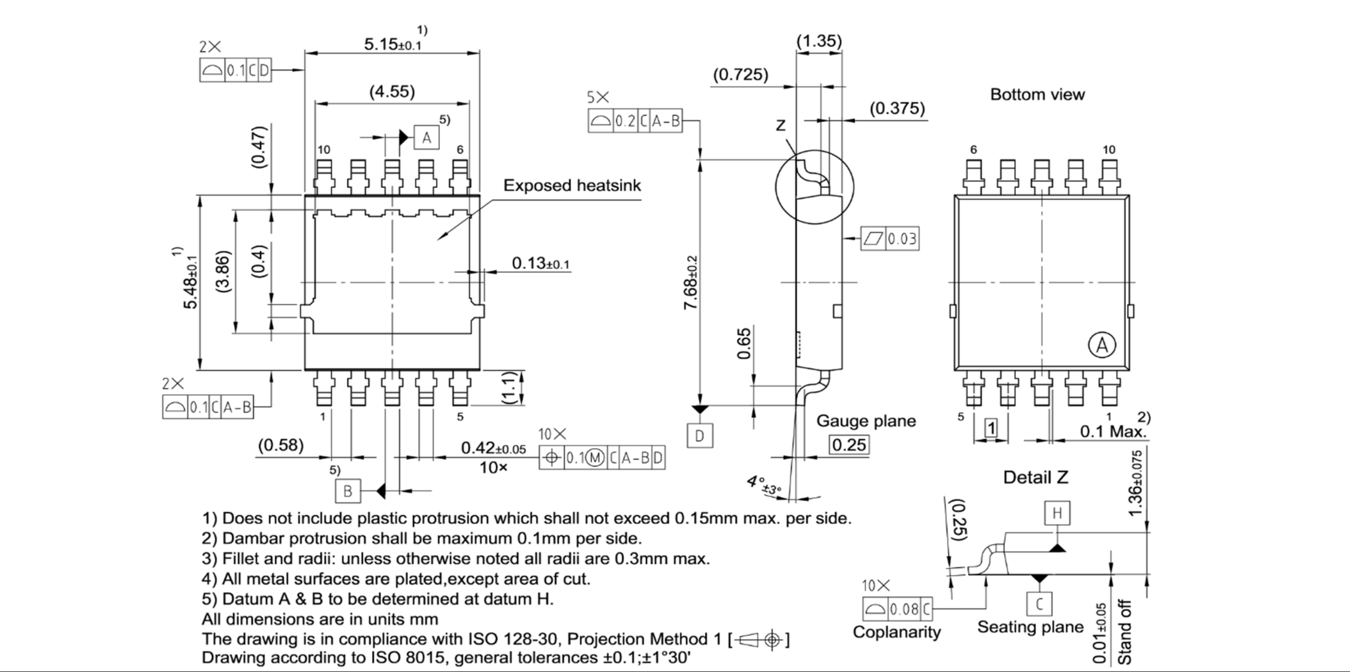
$V_{GS} = f(Q_{gate})$; $I_D = 120$ A pulsed; parameter: V_{DD}



16 Gate charge waveforms

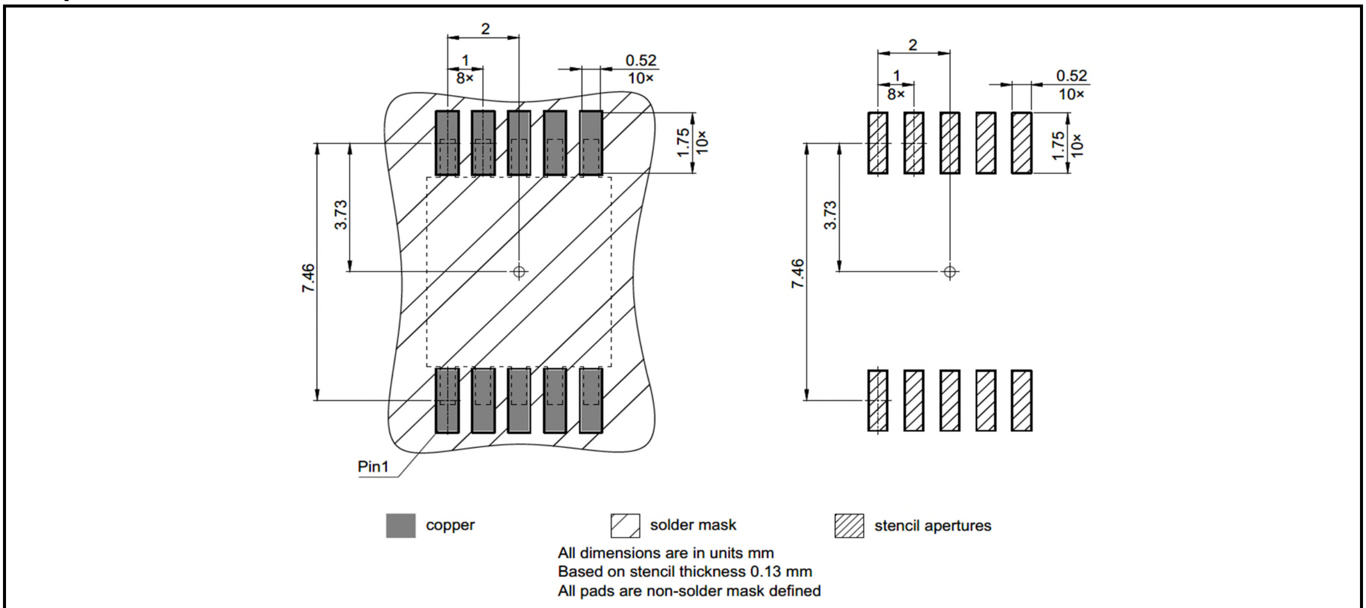


Package Outline

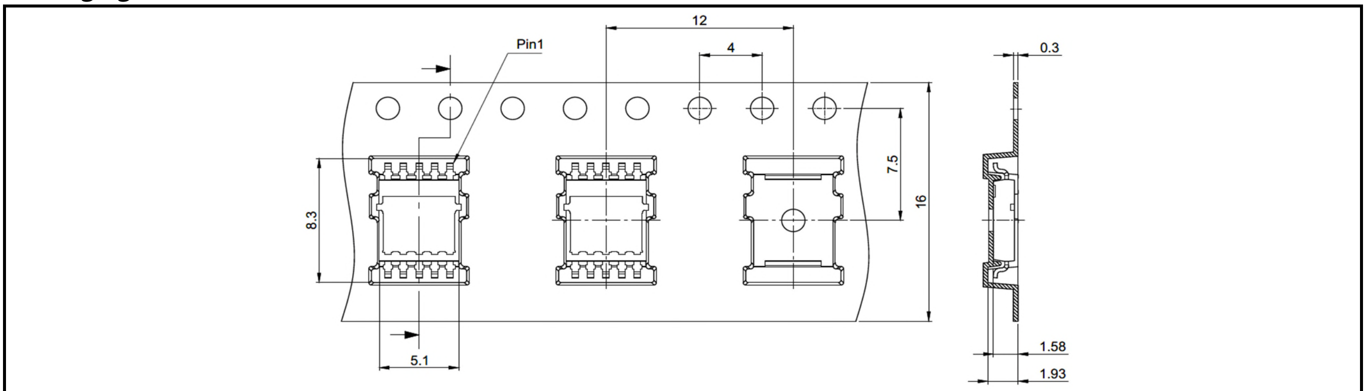


https://www.infineon.com/cms/en/product/packages/PG-LHDSO/PG-LHDSO-10-3

Footprint



Packaging



all dimensions in mm

Revision History

Revision	Date	Changes
Revision 1.1	10.08.2023	Final data sheet
Revision 1.2	31.07.2024	updated package drawing with harmonized & standardized tolerance writing methodology

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Edition 2024-07-31

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference IAUCN04S6N007T-Data-Sheet-12-Infineon