



Sr Staff Elect Design Engr (#21062)

Job description

Design of CPU Subsystem IPs including micro architecture, logic design, LINT, Clock Domain Crossing Analysis, UPF, LEC, Synthesis, ATPG, overseeing all verification, backend implementation and validation aspects of the IP etc.

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Profile

- 1.Strong written and verbal communication skills - Facilitator of direct and open communication, diversity of opinion, and debate.
- 2.In addition, be self-motivated with the initiative to seek constant improvements in the logic design methodologies.
- 3.The candidate must also possess strong initiative, analytical/problem solving skills, team working skills, ability to multitask and be able to work within a diverse team environment.
- 4.Minimum Requirements: BS or MS degree in Electrical Engineering, Computer Engineering or other related field of study with a minimum of 10+ years of relevant experience in IP/SoC design.
- 5.Must have the following:
- 6. Proven expertise in Silicon product development preferably in micro controller space
- 7. Experience with designing/dealing with various type of blocks like SRAM, SROM, embedded Flash macros etc.
- 8.The ability to work as an individual and as part of a team to deliver complex IPs starting from the creation of the spec, design, verification, and finally high volume productization is a strong requirement.
- 9. Expertise in dealing and designing with complex IP's from different sources onto the same piece of silicon.
- 10.Understand system implications of the silicon design decisions. Degree & Discipline: ME, MICROELECTRONICS & EMBEDDED SYSTEMS

At a glance

Location: **Shanghai,**

Job ID: **CY21062**

Entry level: **5+ years**

Type: **Full time**

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