



Staff Engineer - Verification & Validation

Job description

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Profile

Good understanding of ASIC verification concepts and techniques. Very good knowledge of Verilog/System Verilog and UVM.
Experience and knowledge in Verification of SoCs related to different applications. Good Knowledge in Power aware verification and Gate level verification is preferable. Should be able to understand the Full-chip Verification requirements well and good knowledge in industry standard protocols is a plus

Benefits

- **Bangalore:** Coaching, mentoring & networking possibilities ; Wide range of training offers & planning of career development; Regional and local talent programs; International assignments; Career paths: Management career, Project management career, Technical ladder career, Individual contributor career, Professional career; Flexible work timing, Part time work, Work from home; Home office; Health & wellness reimbursement, Employee motivation forum, Spoorthi – Diversity club, Master health check up, Health promotion campaigns; Crèche facility; Annual success bonus; Medclaim (dependents & top up), Personal accident, Term life; National Pension Scheme; Health promotion programs; Statutory benefits; Access for wheelchairs; On-site canteen; Paid sick leave, long term illness leave; On site Yoga classes, Sports club

Why Us

1. Will be part of a team that handles Verification for complex SoCs and close the Verification to the challenging milestones.
2. SoC Verification: Full-chip VR creation as per the chip requirements and UVM/OVM Test benches creation
3. Support in building verification infrastructure at the chip level as per the

At a glance

Location:

Job ID: **337098**

Start date: **as soon as possible**

Entry level: **3-5 years**

Type: **Full time**

Contract: **Permanent**

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requirements

4. Capable of handling multiple areas of SoC Verification: RTL, Power Aware and Gate Level Verification

