



## SENIOR STAFF ENGINEER SIMULATION

### Job description

In this role, you are responsible for Assembly Process Simulation of Semiconductor Packaging (e.g., Die Attach, Wire Bonding, Transfer Molding, Trim Form & Singulation, etc.)

In your new role you will:

- Plan and execute simulation-based risk assessment to address project technical risks identified during early phase
- Recommend risk mitigation strategies to achieve robustness (e.g. Design change, process optimization, etc.)
- Offer physics-based explanations to support Root Cause Investigation during Failure Analysis and suggest appropriate countermeasures
- Participate in generating Design Rules, Invention Disclosures and Patents thru close collaboration with DEV partners (e.g., I-Projects, InnoNet)
- Develop New Sim Methods and/or enhance methods to improve prediction accuracy
- Provide technical guidance & coaching to junior colleagues thru knowledge sharing

### Profile

You are best equipped for this task if you have:

- Master's or PhD Degree in Engineering (Mechanical, Material Science, etc.), Mathematics, Physics or equivalent.
- Minimum 6 to 8 years of professional experience
- Advanced Level in Finite Element Analysis (minimum)
- Experience in modeling non-linear material behavior (e.g., viscoelasticity, creep, fatigue, etc.)
- Backend Assembly Process experience and related tooling design know-how will be considered
- Ability to communicate complex technical solutions in a way that clients clearly understand

### At a glance

Location: **Melaka**  
Job ID: **306652**  
Start date: **immediately**  
Entry level: **5+ years**  
Type: **Full time**  
Contract: **Permanent**

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