



Sr Elect Design Engr (#23441)

Job description

Work on block-level ASIC design, at least in one stage of design phase, RTL/synthesis /verification/DFT/P&R.

1. Graduate level design engineering position for logic verification and HDL design entry of system on chip (SOC) projects
2. Work on block-level ASIC design, at least in one stage of design phase, RTL/synthesis /verification/DFT/P&R.

Profile

1. Education in MSEE/CE
2. Graduate level with workign expreience <= 1 year
3. Familiar with digital logic and analog designs with basic knowledge in IP and SoC design flow
4. Basic programming skills with language knowledge of C, C++, System Verilog/OVM /UVM, Makefiles, C-shell scripts, Perl, Unix / Linux, MS office products (Word, Excel, PowerPoint, Project)

Benefits

- **Shanghai**, : Coaching, mentoring networking possibilities; Wide range of training offers & planning of career development; International assignments; Different career paths: Project Management, Technical Ladder, Management & Individual Contributor; Flexible working conditions; Medical coverage; On-site social counselling and works doctor, in Wuxi only.; Provision of health tips, health knowledge sharing, annual medical check; Employees in Shanghai are entitled to use a gym located close to the office for free; On-site canteen, in Wuxi only.; Private insurance offers in some sites.; Wage payment in case of sick leave; Corporate pension benefits in some sites.

Why Us

Part of your life. Part of tomorrow.

We make life easier, safer and greener – with technology that achieves more, consumes less and is accessible to everyone. Microelectronics from Infineon is the key to a better future. Efficient use of energy, environmentally-friendly mobility and security in a connected world – we solve some of the most critical challenges that our society faces while taking a conscientious approach to the use of natural resources.

At a glance

Location: **Shanghai, (China)**

Job ID: **CY23441**

Entry level: **0-1 year**

Type: **Full time**

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