



Doctoral Thesis: Concept Modeling (f/m/div)*

Job description

The industrial doctorate at Infineon: Pursue a doctoral degree at a university and gain professional experience simultaneously - an ideal start for your career. Advance your research with us and profit from our vast network of doctoral candidates and the expertise of a university. Mentorship is handled by both professors and dedicated Infineon employees. We are offering a doctoral thesis dealing with Concept Modeling. Virtual prototyping – especially using SystemC and its TLM libraries – is a widely accepted approach to describe hardware architectures in a more abstract way than RTL. Virtual prototypes are used for architecture exploration, as reference models and for SW verification. Even though virtual prototypes are faster to build than RTL code, they have several drawbacks. • The TLM modeling abstraction is not defined clearly. Despite the building of the model is defined by SystemC and its libraries, the chosen value and property (as timing or power) representation, accuracy, and granularity leaves many degrees of freedom. As a result, different modeling styles are used for the same purpose, even inside the same company. • Concept and architecture trade-off simulation requires fast to build and rapidly to simulate models. • Reference models require a full functionality, where as timing can be adjusted in the testbenches' scoreboard. • Models for SW verification require a relative high accuracy, especially at the hardware-software interface. This causes a permanent update of the models if the design changes. • In addition, the kind of data expected from simulating a model varies and must not necessarily require the implementation of full functionality (e.g. no except handling). There exist a set of promising modeling approaches, which however have not been applied for hardware modelling, which support only a fraction of hardware models, or which require extensions to provide the wanted information. • One example are SysML, especially Activity and State Charts, which however lack the notion of timing or other hardware features. • Another example is ETISS, which is a pure functions ISS simulation framework, which allows hooking analysis functions via extension mechanisms. • A widely used approach is the quantum keeper of SystemC, allowing to decouple the simulation time and the considered simulation time in a configurable way. • The last approach worth to mention – and there may be more – is TLM+, which includes a mechanism to handle annotated timing, however requires the SW stack to be modeled as well. This doctoral thesis should study the existing approaches and pursue for a concept modeling methodology. In parallel, this thesis should model state-of-the-art CPU subsystems, especially including accelerators, with the newly developed method to prove the applicability and get feedback to enhance the methodology. The thesis will be written in cooperation with Technical University Munich and under the supervision of Prof. Dr. Wolfgang Ecker.

The tasks within the thesis will consist of:

- An **overview of the current concept modeling approaches, SystemC TLM variants, and other languages** used for describing abstract models
- The **study of state-of-the-art abstraction methods**, the **development of a generic abstraction method**, the **definition of annotation** and the **integration of annotations** as well as an **execution model**

At a glance

Location: **Munich (Germany)**
Job ID: **361504**
Start date: **Sep 01, 2022**
Entry level: **0-1 year**
Type: **Full time**
Contract: **Temporary**

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Contact

Silke Jaschik
Student Attraction Manager



- The **approach for modeling parallelism** in an easy way. It is expected, that most parts of the model are **coded as a program** – i. e. in a sequential way – but an **approach for lightweight parallelism** may help to reduce the modelling effort
- The **finding of a software method** – potentially also with code generation as one pillar – to implement the abstraction method in a clean way

The learnings out of the thesis will lead to

- A methodology of abstract hardware modeling and HDLs and C/C++ code generation in an industrial environment
- Various modeling and abstraction concepts and their implementation
- The virtualization of hardware properties as timing beyond virtual simulation time

Profile

A doctoral student is a research enthusiast,

- › whose interests are scientific research combined with the passion for Infineon's innovative products and applications.
- › who enjoys working in an industrial environment in combination with an Infineon partner university.
- › who appreciates open communication and the contribution of an international environment.
- › and is thus an excellent candidate for a further academic or industrial career after completion of their thesis.

As the ideal candidate you:

- Graduated from **Computer Engineering, Electrical Engineering or a related field** with **very good grades**
- Show **curiosity and openness** as well as an **interest in learning and trying out new things**
- Already gained **first experience with metamodeling, (template-based) code generation and/ or model-driven architecture**
- Possess **know-how in object-oriented programming** with languages such as C/ C++ and Python
- Are **experienced in digital design and RTL and TLM modeling** with SystemC or SystemVerilog
- Have **good knowledge of processors and SoC architecture**
- Are **very good** in communicating in **English** and ideally German

Benefits

- **Munich:** Coaching, mentoring networking possibilities; Wide range of training offers & planning of career development; International assignments; Different career paths: Project Management, Technical Ladder, Management & Individual Contributor; Flexible working conditions; Home office options; Part-time work possible (also during parental leave); Sabbatical; On-site creche and kindergarden with 120 spots, open until 6pm; Holiday child care; On-site social counselling and works doctor; Health promotion programs; On-site gym, jogging paths, beachvolleyball, tennis & soccer court; On-site canteen; Private insurance offers; Wage payment in case of sick leave; Corporate pension benefits; Flexible transition into retirement ; Performance bonus; Reduced price for public transport and very own S-Bahn station; Access for wheelchairs

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The central R&D organization „**Design Enabling and Services**“ (DES) provides the design environment to the different Infineon product development teams. With state-of-the-art design methods, building blocks and a wide range of product development services DES supports Infineon's advanced IC development from early high-level system models to verified products ready for manufacturing.

** The term gender in the sense of the General Equal Treatment Act (GETA) or other national legislation refers to the biological assignment to a gender group. At Infineon we are proud to embrace (gender) diversity, including female, male and diverse.*

