



Doctoral Thesis: Hardware-IP Function Set Definition (f/m/div)*

Job description

The industrial doctorate at Infineon: Pursue a doctoral degree at a university and gain professional experience simultaneously - an ideal start for your career. Advance your research with us and profit from our vast network of doctoral candidates and the expertise of a university. Mentorship is handled by both professors and dedicated Infineon employees. We are offering a doctoral thesis dealing with Hardware-IP Function Set Definition. In the current semiconductor development flows, functional verification is one of the main resource intense activity that is known to consume more than 50% of the overall project schedule. Ensuring bug-free designs is critical to ensure the quality of the products. Formal verification is a verification technique that uses mathematical reasoning to prove the presence or absence of bugs in a design. However, developing a good property set for a given design from a set of specification is known to be hard. Additionally, manual coding of properties is erroneous and time tedious. As a result, formal verification which offers an exhaustive solution has not been widely adopted for functional verification. A pre-requisite to develop a good property set with minimal efforts is to have a good specification set, ideally in a well-defined format. For example, processor-based designs are specified through Instruction Set Architecture (ISA) manuals. ISAs have been successfully used to document the expected operations from a processor implementation. There have been numerous approaches on generating the RTL code and properties from ISA models to automate both design and verification steps for processor designs. For non-processor designs, the specifications are captured typically in an informal format. While the informal specification can be formalized, and eventually, the properties can be generated from the formalized specification models, the process needs to be repeated for different non-processor designs. To address these critical topics of functional verification, this PhD thesis focuses on the following:

- Explore the adaption of ISA notation for specifying the functions of processor-like and non-processor designs
- Develop the ideas to adapt the notation for designs with different characteristics
- Explore the generation of RTL code, formal verification properties, and behavioral models from the ISA-like formalized specifications of functions
- Apply the explored methods on the designs developed at Infineon and show both qualitative and quantitative advantages over the state-of-the-art methods

There is already a known work in this direction from Princeton University, USA. The approach is termed as ILA (see e.g. Instruction-level abstraction (ILA): A uniform specification for system-on-chip (SOC) verification Bo Yuan Huang, Hongce Zhang, Pramod Subramanyan, Yakir Vizel, Aarti Gupta, Sharad Malik). However it lacks generality and the adoptability. Scalability of the approach at the industry level has not been explored. Additionally, the generated code from the approach is unreadable and may need additional efforts to make it usable in real design projects. This doctoral thesis should study the existing approaches to formalize specifications and pursue for a generic methodology for capturing specifications of hardware designs. In parallel, this thesis should model state-of-the-art CPU peripherals with the newly develop method to

At a glance

Location: **Munich (Germany)**
Job ID: **361165**
Start date: **Sep 01, 2022**
Entry level: **0-1 year**
Type: **Full time**
Contract: **Temporary**

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Contact

Silke Jaschik
Student Attraction Manager



prove the applicability and get feedback to enhance the methodology. The thesis will be written in cooperation with Technical University Munich and under the supervision of Prof. Dr. Wolfgang Ecker.

The tasks within the thesis will consist of:

- Gaining an **overview of the state-of-the-art methods for formalizing design specifications and code generation approaches**
- **Studying current formal verification approaches** to functional verification, **innovating new formal approaches** to improve the verification quality
- Developing a **methodology to capture design specifications**
- **Building a generation framework** for generating RTL code, formal properties, and virtual prototypes from the formalized specifications
- **Applying the methods on designs** developed at Infineon and **benchmarking the results** against the state-of-the-art methods

The learnings out of the thesis will lead to

- Functional verification methodologies with a special focus on formal verification
- The methodology of 'code generation' in an industrial environment
- Various modeling and abstraction concepts and their implementation
- Comprehensive consideration of verification solutions to complex designs

Profile

A doctoral student is a research enthusiast,

- › whose interests are scientific research combined with the passion for Infineon's innovative products and applications.
- › who enjoys working in an industrial environment in combination with an Infineon partner university.
- › who appreciates open communication and the contribution of an international environment.
- › and is thus an excellent candidate for a further academic or industrial career after completion of their thesis.

As the ideal candidate you:

- Graduated in **Computer Engineering, Electrical Engineering or a related field** with very good grades
- Bring **curiosity and openness** as well as an **interest in learning and trying out new things**
- Already gained **first experience with metamodeling, (template-based) code generation and/ or model-driven architecture**
- Show **know-how in object-oriented programming** with languages such as C/ C ++ and Python
- Possess **good knowledge of digital design and RTL modeling** in VHDL and/ or (system) Verilog; RTL synthesis would be a plus
- Bring **first experience with verification**, ideally formal verification is desired
- Have **good knowledge of processors and SoC architecture**
- Have **very good knowledge of English and ideally German**

Benefits

- **Munich:** Coaching, mentoring networking possibilities; Wide range of training offers & planning of career development; International assignments; Different career paths: Project Management, Technical Ladder, Management & Individual Contributor; Flexible working conditions; Home office options; Part-time work possible (also during parental leave); Sabbatical; On-site creche and



kindergarden with 120 spots, open until 6pm; Holiday child care; On-site social counselling and works doctor; Health promotion programs; On-site gym, jogging paths, beachvolleyball, tennis & soccer court; On-site canteen; Private insurance offers; Wage payment in case of sick leave; Corporate pension benefits; Flexible transition into retirement ; Performance bonus; Reduced price for public transport and very own S-Bahn station; Access for wheelchairs

Why Us

Part of your life. Part of tomorrow.

Infineon is a world leader in semiconductor solutions that make life easier, safer, and greener. Our solutions for efficient energy management, smart mobility, and secure, seamless communications link the real and the digital world.

The central R&D organization „**Design Enabling and Services**“ (DES) provides the design environment to the different Infineon product development teams. With state-of-the-art design methods, building blocks and a wide range of product development services DES supports Infineon's advanced IC development from early high-level system models to verified products ready for manufacturing.

** The term gender in the sense of the General Equal Treatment Act (GETA) or other national legislation refers to the biological assignment to a gender group. At Infineon we are proud to embrace (gender) diversity, including female, male and diverse.*

