



## Staff Engineer Design Verification

### Job description

Actively participate in definition of Verification infrastructure including test bench components, testcases which are scalable and portable across various projects and platforms.

- Actively participate in definition of Verification infrastructure including test bench components, testcases which are scalable and portable across various projects and platforms
- Define verification strategy (constraint random, Formal, Directed etc.) for IP /Subsystem/SOC verification
- Identify, document and execute test plans on verification platforms, develop and debug random constrain verification test suite to fully verify the design under test
- Experience with pre-silicon Verification of designs which include multiple processor cores and other custom logic
- Actively participate in post-silicon bring-up, validation and compliance testing
- Actively participating in cross functional collaboration with design, software and hardware teams to ensure a successful product delivery
- Self-motivated with the initiative to seek constant improvements in the verification methodologies
- Possess strong initiative, analytical/problem solving skills, teamworking skills and ability to multitask

### Profile

Solid understanding of verification methodologies and one or more of the standard test bench languages: System Verilog (OVM/UVM), C/C++, Perl, Tcl scripting

- Experience in developing verification infrastructure for complex IPs/Subsystem/SoCs
- Good understanding of SoC verification which covers reset, clocking, power transitions, io-muxing, DMA etc
- Knowledge of industry standard interfaces like PCIe, USB, AMBA, SDIO and MIPI standards are highly desirable
- Familiarity with functional coverage, code coverage, other coverage metrics
- Knowledge of processor based SoC verification which includes, ARM core programming, boot process, error exceptions, handshake b/w processor and test bench is desirable
- Familiarity with pre-silicon validation and post silicon validation flow is a plus
- Good understanding of power aware verification and Gate level simulation
- Knowledge of C, python, tcl, perl etc. for developing SoC verification test content and scripts

### Benefits

### At a glance

Location: **Bangalore (India)**  
Job ID: **351933**  
Start date: **as soon as possible**  
Entry level: **5+ years**  
Type: **Full time**  
Contract: **Permanent**

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### Contact

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