



## Senior Engineer Elect Design

### Job description

#### Job Description

- 1) Participate in block/IP/chip floor planning from scratch, performing routing & layout verification (LVS, DRC, antenna & others) and troubleshooting the results;
- 2) Co-lead/lead the physical layout of IP/full chip design by working closely with cross functional team leader;
- 3) Conduct thorough layout design reviews internally, and external review with circuit designers;
- 4) Extensive use of CAD tools (cadence virtuoso VXL & mentor calibre) in IP/chip integration and verification;
- 5) capable in guiding/coaching junior engineers for on time delivery and quality.

### Profile

#### Job Specification

- 1) Bachelor degree in Electrical/Electronic Engineering/physics with VLSI exposure or equivalent 9 -15 years of job experience in analog layout design;
- 2) Hands-on experience in analog layout from scratch. Knowledge & experience in HV layout will be a plus;
- 3) Deep understanding of analog circuit layout concepts in submicron CMOS technologies;
- 4) Posses strong technical, analytical & problem solving skills in analog layout design;
- 5) Ability to work as strong team player and participate in cross functional activities;
- 6) Good interpersonal, verbal and communication skill with good initiative at work.

### Why Us

#### Part of your life. Part of tomorrow.

Infineon is a world leader in semiconductor solutions that make life easier, safer, and greener. Our solutions for efficient energy management, smart mobility, and secure, seamless communications link the real and the digital world.

### At a glance

Location: **Penang (Malaysia)**  
Job ID: **350138**  
Start date: **as soon as possible**  
Entry level: **1-3 years**  
Type: **Full time**  
Contract: **Permanent**

Apply to this position online by following the URL and entering the Job ID in our job search:

Job ID: **350138**  
[www.infineon.com/jobs](http://www.infineon.com/jobs)

