



## Senior Staff Engineer - Digital IC Design

### Job description

You will be responsible for delivering high-quality RTL coding, verification and synthesis. You will also be in charge of the concept, DFT and design of the IP assigned.

In your new role you will:

- Responsible to deliver **high-quality RTL coding, verification and synthesis on area of work.**
- Responsible for the **concept, DFT and design of the IP** assigned.
- Tightly working with **SOC Layouters and the analog/software team.**
- Perform full **pre and post-layout IP and Fullchip verifications.**
- Implement **digital design in FPGA** and **perform the FPGA debugging.**
- Exposure to **all stages of IC Design processes and flow.**
- Continuous improvement on **digital design methodologies and flow.**
- Define **silicon bring up plan** and **component validation of 1st silicon.**
- Define **IP /Chip micro-architecture** for design reviews in the project.

### Profile

You are best equipped for this task if you have:

- Good knowledge in **digital design techniques** and the state-of-the-art design verification method.
- Solid fundamentals in IC design flow and verification concepts.
- Experience with **RTL2GDS, floorplanning, static timing analysis, timing closure and verification**
- Hands-on exposure on of **FPGA, formal verification and power analysis.**
- Knowledge in **ACDC SMPS IC design-related** will be an advantage.
- Good in scripting using **PERL/PYTHON**
- **Exposure to Cadence and Synopsys tools**
- Experienced in DFT scan tools and test mode concepts will be an advantage.
- Able to communicate well and good in interpersonal skills
- Strong analytical and problem-solving skills

### Why Us

#### At a glance

Location: **(Singapore)**  
Job ID: **346764**  
Start date: **as soon as possible**  
Entry level: **5+ years**  
Type: **Full time**  
Contract: **Permanent**

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