



## Principal Engineer Timing Sign-Off Methodology (f/m/div)\*

### Job description

We are offering a position in the area of advanced timing sign-off validation methodology. Your task is to drive the Static Timing Analysis (STA) and timing methodology development. In addition, you assess product requirements and drive solutions to fulfill them. Furthermore, you understand and follow the trends of semiconductors and transfer them into strategic projects for our team. If you are highly motivated to understand technical details then take this chance and apply now! The Technical Ladder is a special career path for those who share innovative ideas, demonstrate comprehensive technical knowledge, show thought leadership, possess problem solving abilities and are able to create business value.

In your new role you will:

- **Develop and apply methodologies** for the timing sign-off process supporting technologies from 5nm to 130nm
- **Review and update of digital timing sign-off guidelines**
- **Be responsible for analysis of DSM effects** and their impact on performance
- **Develop methods** to estimate/measure performance of products
- **Assess and evaluate foundry signoff regulations**
- **Be responsible for the investigation** of observed and described effects
- **Transfer dynamic effects** into static analysis methods
- **Define and fine-tune implementation- and signoff-guardbands** for optimum design robustness
- **Act as coach and role model for other team members** and support them to develop

### Profile

You take in information quickly, evaluate it from different points of view, and uncover hidden correlations in it. Moreover, you accept responsibility for decisions and for their positive or negative outcome as well as you cooperate across boundaries and appreciate the contributions of other people.

You are best equipped for this task if you have:

- A technical **degree in Electrical Engineering, Computer Science, Physics** or similar; ideally a PhD
- At least **6+ years experience in timing analysis and verification and/or in digital chip design**

### At a glance

Location: **Munich (Germany)**  
Job ID: **338911**  
Start date: **as soon as possible**  
Entry level: **5+ years**  
Type: **Full time**  
Contract: **Permanent**

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### Contact

**Mona Straßmair**  
Talent Attraction Manager



- Excellent **experience in statistical analysis of DSM effects** and their impacts on chip design and timing verification
- **Deep knowledge in Static Timing Analysis and SPICE simulation**
- Advanced **programming skills in Perl/ Python and SQL**
- **Experience on Digital Implementation flow and STA** (Cadence/Synopsys) is expected
- **Fluent communication skills in English** and use them to share your knowledge actively, German is a plus

## Benefits

- **Munich:** Coaching, mentoring networking possibilities; Wide range of training offers & planning of career development; International assignments; Different career paths: Project Management, Technical Ladder, Management & Individual Contributor; Flexible working conditions; Home office options; Part-time work possible (also during parental leave); Sabbatical; On-site creche and kindergarden with 120 spots, open until 6pm; Holiday child care; On-site social counselling and works doctor; Health promotion programs; On-site gym, jogging paths, beachvolleyball, tennis & soccer court; On-site canteen; Private insurance offers; Wage payment in case of sick leave; Corporate pension benefits; Flexible transition into retirement ; Performance bonus; Reduced price for public transport and very own S-Bahn station; Access for wheelchairs

## Why Us

**Part of your life. Part of tomorrow.**

We make life easier, safer and greener – with technology that achieves more, consumes less and is accessible to everyone. Microelectronics from Infineon is the key to a better future. Efficient use of energy, environmentally-friendly mobility and security in a connected world – we solve some of the most critical challenges that our society faces while taking a conscientious approach to the use of natural resources.

The central R&D organization „**Design Enabling and Services**“ (DES) provides the design environment to the different Infineon product development teams. With state-of-the-art design methods, building blocks and a wide range of product development services DES supports Infineon's advanced IC development from early high level system models to verified products ready for manufacturing.

*\* The term gender in the sense of the General Equal Treatment Act (GETA) or other national legislation refers to the biological assignment to a gender group. At Infineon we are proud to embrace (gender) diversity, including female, male and diverse.*

