# Senior Staff Engineer Elect Design

## Job description

We are looking for professional with 8-12 years of timing analysis and signoff experience. Also, having strong STA fundamentals.

- Should have strong STA fundamentals.
- Has done timing sign-off including timing margin calculations independently atleast for one project as hands-on lead.
- Experience in handling STA of multi-power domain designs & constraint mode merging.
- STA flow development, abstraction with bottleneck identification. Proficient in design margins and SDC constructs.
- TAT reduction in multi-mode, multi power domain/designs. Generate timing ECOs for Physical design.
- Drive ambitious schedules, and enables dependent teams to accomplish.
- Interface to design team and PD team and drive TAT reduction for PD.

## Profile

- BTech/MTech degree in Electrical/Electronics with 8-12 years of timing analysis and signoff experience.
- Thorough knowledge of the ASIC design timing closure flow and methodology.
- Experience in static timing analysis and timing signoff with complex SoCs in advanced tech nodes involving multiple modes/corners.
- Knowledge of timing corners/modes, process variations and signal integrity related issues.
- Proficient with EDA tools from Synopsys/Cadence/Mentor.
- Excellent analytical & communication skills. Shown ability to collaborate in a multi-functional environment, cross-site or cross-time zone.
- Proficient in Tcl and Perl or other scripting relevant language is a plus.
- Proficient with EDA tools from Synopsys/Cadence/Mentor.

## At a glance

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|---|---|
| Location: | **Bangalore (India)** |
| Job ID: | **331323** |
| Start date: | **immediately** |
| Entry level: | **5+ years** |
| Type: | **Full time** |
| Contract: | **Permanent** |

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## Contact

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