Senior Staff Engineer Packaging

Job description

Job Description:

- Design laminate substrate and wafer level products using Cadence and AutoCAD package design tools.
- Products may span a wide spectrum – from single die to multi die including active and passive components, wire bond and flip chip BGA or wafer level.
- Knowledge in Signal Integrity with capability to extract and analyze Package Parasitic will be considered a distinct plus.

Profile

Job Requirements:

- Bachelor's/Master's degree in Electronics, Electrical, Microelectronics or other related Engineering field.
- At least 5 years of related working experience in semiconductor industry.
- Good knowledge of SI fundamentals including Electromagnetics, transmission line theory and S-parameters and familiarity with Cadence and Ansys SI tools to perform Package electrical analysis will be considered a major asset.
- Skilled in programming/scripting languages and knowledge in AutoCAD, Cadence -Allegro package design, Cadence –PCB.
- Strong communication and interpersonal skills.
- Ability to work productively independently and in a team environment.

At a glance

Location:	**Penang (Malaysia)**
Job ID:	**331056**
Start date:	**immediately**
Entry level:	**5+ years**
Type:	**Full time**
Contract:	**Permanent**

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