Staff Engineer Elect Design

Job description

Candidate will be responsible for building/maintaining highly configurable and reusable IO Subsystems.

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- (Note: An IO Subsystem is a logic IP that processes the IO Pads/IO Ring information and builds required logic to allow multiple on-chip peripherals to share the same IOs in a configurable manner).
- Candidate will be responsible for RTL design for integration of IO pads into SoC, building the required multiplexing logic and necessary power control signals integration.

Profile

- Must have worked in ASIC Design flow for more than 5 years.
- Must be strong in scripting using PERL..
- Must be familiar with RTL design for ASIC development using Verilog.
- Must be familiar with LINT (LEDA/Spyglass), Clock-Domain-Crossing analysis, UPF, MVRC, Synthesis, Timing constraints and debugging STA reports.
- Strong mindset towards automation of repetitive work.
- Strong fundamentals in DFT/Fault-grading and/or hands on experience.

At a glance

Location:	**Bangalore (India)**
Job ID:	**324276**
Start date:	**immediately**
Entry level:	**5+ years**
Type:	**Full time**
Contract:	**Permanent**

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