



## Staff Engineer Elect Design

### Job description

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- (Note: An IO Subsystem is a logic IP that processes the IO Pads/IO Ring information and builds required logic to allow multiple on-chip peripherals to share the same IOs in a configurable manner).
- Candidate will be responsible for RTL design for integration of IO pads into SoC, building the required multiplexing logic and necessary power control signals integration.

### Profile

- Must have worked in ASIC Design flow for more than 5 years.
- Must be strong in scripting using PERL..
- Must be familiar with RTL design for ASIC development using Verilog.
- Must be familiar with LINT (LEDASpyglass), Clock-Domain-Crossing analysis, UPF, MVRC, Synthesis, Timing constraints and debugging STA reports.
- Strong mindset towards automation of repetitive work.
- Strong fundamentals in DFT/Fault-grading and/or hands on experience.

### Benefits

- **Bangalore:** Coaching, mentoring & networking possibilities ; Wide range of training offers & planning of career development; Regional and local talent programs; International assignments; Career paths: Management career, Project management career, Technical ladder career, Individual contributor career, Professional career; Flexible work timing, Part time work, Work from home; Home office; Health & wellness reimbursement, Employee motivation forum, Spoorthi – Diversity club, Master health check up, Health promotion campaigns; Crèche facility; Annual success bonus; Medclaim (dependents & top up), Personal accident, Term life; National Pension Scheme; Health promotion programs; Statutory benefits; Access for wheelchairs; On-site canteen; Paid sick leave, long term illness leave; On site Yoga classes, Sports club

### Why Us

### At a glance

Location: **Bangalore (India)**  
Job ID: **324276**  
Start date: **as soon as possible**  
Entry level: **5+ years**  
Type: **Full time**  
Contract: **Permanent**

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### Contact

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