Digital Verification Engineer (f/m/div)*

Job description

Are you a passionate young engineer who wants to join an energetic Verification team that uses leading-edge tools and methodologies? You can now be part of the #1 semiconductor partner in the fast-changing world of automotive! You just have to apply to join Infineon's Design Center in Padova as a Digital Verification Engineer.

As a Digital Verification Engineer, you will be part of a small, fast-paced Verification team using leading-edge verification tools and methodologies to enable the functional verification of PMICs (Power Management ICs) for the Automotive market.

In your new role you will:

- Create **verification plans and test suites** based on design specification;
- Build **verification environments** consisting in test benches for top/block level;
- Design **self-checking test benches** using modern verification techniques based on SystemVerilog and UVM methodology;
- Design **verification components** such as bus functional models, monitors, and behavioral models;
- Develop and implement **functional coverage plans** and assertions using SystemVerilog;
- Be responsible for **analyzing and debugging simulation failures**;
- Make **regression simulation**, evaluating functional coverage and performance results.

Profile

You demonstrate high quality standards for yourself and generate value with your ideas and solutions. You demonstrate strong communication skills, know how to establish lasting relationships and networks. Moreover, you have a structured working style and coordinate your work with colleagues, regularly sharing your insights with them.

You are best equipped for this job if you have:

- A **degree in Electronic/ Electrical Engineering** or equivalent field of studies;
- Knowledge of **object-oriented verification languages**;
- Some **debugging and scripting skills**;
- Excellent **communication skills in English and Italian**.

At a glance

Location:	**Padua (Padova) (Italy)**
Job ID:	**322030**
Start date:	**immediately**
Entry level:	**1-3 years**
Type:	**Full time**
Contract:	**Permanent**

Apply to this position online by following the URL and entering the Job ID in our job search:

Job ID: 322030
www.infineon.com/jobs

Contact

Margarida Carneiro
Talent Attraction Manager

It is an advantage if you have:

- Experience in IC Verification, including use of SystemVerilog, VHDL or Verilog;
- Experience with C/C++ and TCL, Python or Perl for scripting;
- Knowledge of Cadence/Synopsys/Mentor Graphics tools for Digital Design and Verification, such as Modelsim, Xcelium, Ncsim, vManager.

Although experience is an advantage we also **welcome applications from fresh graduates**.