



Senior Staff Engineer - Verification & Validation

Job description

In your new role, you will:

- Verification of complex SoCs / IPs and provide technical leadership to the team while creating test plans and test bench architecture
- Development of constraint-random verification environment at both sub-system and SoC level
- Develop expertise in multiple areas of verification – RTL, Gate level and Power aware simulations
- Drive verification closure on complex modules and SoCs using SV/UVM based methodology
- Leading medium complex SoCs Verification to close the Verification on time
- Schedule management and handling cross functional team interactions
- Should be a good mentor and guide for junior engineers in the team

Profile

You are best equipped for this task if you have:

- Bachelor's - 9 to 11 years' experience, Master's - 8 to 10 years' experience
- Good understanding of ASIC verification concepts and techniques
- Ability to develop verification architecture documents for complex modules /systems
- Ability to architect complex module / sub system / Full chip test benches and build verification infrastructure
- Very good knowledge of Verilog/System Verilog and UVM
- Should be a good mentor and guide for junior engineers in the team
- Candidate should have worked on ARM based SoC verification covering RTL, Power Aware and Gate level simulations.

At a glance

Location: **Bangalore (India)**
Job ID: **320531**
Start date: **immediately**
Entry level: **5+ years**
Type: **Full time**
Contract: **Permanent**

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