



Staff Engineer Verification & Validation

Job description

AMS Verification on multiple SOC's or sub-systems. One should have proficiency in AMS simulation environment using Cadence/Synopsys/Mentor tools.

- Candidate should have working experience with AMS Verification on multiple SOC's or sub-systems. One should have proficiency in AMS simulation environment using Cadence/Synopsys/Mentor tools.
- Knowledge of digital design techniques, Verilog HDL, and standard RTL coding styles, as well as analog circuit basics, with previous analog design experience a plus.
- Candidate should be familiar with the concepts of behavioral modeling - both digital (Verilog-D) and analog (Verilog-A or Verilog-AMS). Experience in SV and UVM testbench development/modifications from mixed signal perspective is a plus.
- Functional knowledge of analog and mixed signal building blocks, such as comparators, op-amps, switched cap circuits, various types of ADCs and DACs, current mirrors, charge pumps, and regulators is expected. Working knowledge of Perl / Skill/ Python/Tcl or other scripting relevant language is a plus.
- Candidate should have ability to lead a project team, and work collaboratively in a multi-site development environment.
- AMS Verification for SoC or IPs - Meeting Full Expectations
- Test plan preparation as per the dynamics of product specifications - Meeting Full Expectations
- Dealing challenges with AMS methodologies of Cadence: irun/xrun or Synopsys: XA-VCS or Mentor Eldo ADMS - Meeting Full Expectations
- Testcase Debug & proposing new scenarios - Meeting Partial Expectations
Behavioral modeling: Verilog, Wreal or SV-RNM - Meeting Partial Expectations
- Handling project dynamics on scope, schedule and effort – coming up with alternative verification plans, Mentoring Junior engineer - Meeting Partial Expectations

Profile

- Candidate with 5 to 9 years of experience.
- Bachelors/Masters degree in Electrical Engineering.
- Experienced in AMS Verification - handling IP/SoC AMSV independently and guide junior engineers.
- SPICE modeling is as an add on is preferable.
- Automation skills in Perl/Python.

At a glance

Location: **Bangalore (India)**
Job ID: **319807**
Start date: **as soon as possible**
Entry level: **5+ years**
Type: **Full time**
Contract: **Permanent**

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Contact

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- Strong analog basics and skillful in Verilog/VerilogAMS and System verilog TB.

Benefits

- **Bangalore:** Coaching, mentoring & networking possibilities ; Wide range of training offers & planning of career development; Regional and local talent programs; International assignments; Career paths: Management career, Project management career, Technical ladder career, Individual contributor career, Professional career; Flexible work timing, Part time work, Work from home; Home office; Health & wellness reimbursement, Employee motivation forum, Spoorthi – Diversity club, Master health check up, Health promotion campaigns; Crèche facility; Annual success bonus; Medclaim (dependents & top up), Personal accident, Term life; National Pension Scheme; Health promotion programs; Statutory benefits; Access for wheelchairs; On-site canteen; Paid sick leave, long term illness leave; On site Yoga classes, Sports club

Why Us

Part of your life. Part of tomorrow.

We make life easier, safer and greener – with technology that achieves more, consumes less and is accessible to everyone. Microelectronics from Infineon is the key to a better future. Efficient use of energy, environmentally-friendly mobility and security in a connected world – we solve some of the most critical challenges that our society faces while taking a conscientious approach to the use of natural resources.

