Senior Staff Engineer - Verification engineer

Job description

Designing self-checking test benches using modern verification techniques

o Designing self-checking test benches using modern verification techniques
o Implementing functional coverage and assertions using System Verilog and UVM
o Developing test and functional coverage plans based on device specifications.
o Analyzing and debugging simulation failures, as well as analyzing functional coverage results to guarantee zero defect outcomes.

Profile

• BSc in Electrical Engineering, or equivalent experience
• 7+ years' experience in IC verification. Experience with constrained-random, coverage driven verification environments is a plus
• Experience developing and working with verification languages like: System Verilog, OVM, UVM
• A solid understanding of verification concepts and experience designing class-based test benches
• C coding and Power aware simulation will be an advantage
• Excellent written and oral communication skills
• Strong debugging skills

At a glance

Location:	**Bangalore**
Job ID:	**314084**
Start date:	**immediately**
Entry level:	**5+ years**
Type:	**Full time**
Contract:	**Permanent**

Apply to this position online by following the URL and entering the Job ID in our job search:

Job ID: 314084
www.infineon.com/jobs

Contact

Rajani Bhaskar