Lead Principal Engineer SoC Integration

Job description

In this role, you will be involved with all phases of physical design from RTL to tapeout, with a primary focus on STA (Static Timing Analysis)

In your new role you will:

- Coordinate with a **small team of engineers to plan and lead the STA effort** for SoC projects in Infineon's MCU and IoT processors teams.
- Understanding **SoC and IP specs** and being able to translate those into STA requirements
- Working with **Timing Signoff methodology** experts to ensure STA flows, margining, etc are appropriate
- Work with **IP and SoC Design and DFT teams** to understand, implement, and validate constraints for SoC-level and physical partitions
- **Run SoC timing analysis** across all design hierarchies
- **Analyze timing and work with RTL/DFT teams** to facilitate logic changes, as required for timing
- **Create ECOs** for timing and power closure on final design closure
- Work with P&R engineers for timing ECOs and signal integrity ECOs
- **Place & Route of SoCs, IP/blocks, and chip-level partitions.** This includes all aspects, from placement, CTS, timing debug, routing, and post-route timing closure to meet power/performance/area requirements
- Participate in **continuous improvement and innovation of CAD and physical design** methodologies

#LI-MH1

Profile

You are best equipped for this task if you have:

- **10+ years of Static Timing Analysis (STA) and Physical Design (RTL to GDSII) experience on SoC designs** across multiple technology nodes
- **Hands on experience and expertise in setting up, running, and debugging** multi-scenario STA, methodology, and tools
- Solid understand of **STA margining requirements**, as related to process variation modeling , clocking, IR dependences, etc
- Hands-on experience in many aspects of physical design including d **ata preparation, synthesis, floor planning, placement, clock tree synthesis, routing, STA, and low power/multi-voltage physical** implementation

At a glance

Location:	**Austin, TX (United States)**
Job ID:	**345405**
Start date:	**as soon as possible**
Entry level:	**5+ years**
Type:	**Full time**
Contract:	**Permanent**

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Job ID: 345405
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- Experience with **ECO flows for functionality, timing, and power**
- Experience with physical implementation tools such as **Innovus/ICC2,Genus/DC, Redhawk, and especially Primetime/Tempus**. Some Tempus experience preferred
- Knowledge of **Basic SoC Architecture and HDL languages like Verilog**
- Solid understanding of **scripting languages such as Tcl/Python/Perl**
- Knowledge of **UPF and low power implementation** techniques and debug
- **Collaborative mindset** to work with local team members, as well as international team members and IP providers
- Strong **problem solving and debug skills** across various levels of design hierarchies
- Strong **verbal and written presentation/communication** skills
- **B.S. or M.S. in EE/ECE/CE/CS**

Why Us

Part of your life. Part of tomorrow.

We make life easier, safer and greener – with technology that achieves more, consumes less and is accessible to everyone. Microelectronics from Infineon is the key to a better future. Efficient use of energy, environmentally-friendly mobility and security in a connected world – we solve some of the most critical challenges that our society faces while taking a conscientious approach to the use of natural resources.

Cypress Semiconductor Corporation is an equal opportunity employer. All qualified applicants will receive consideration for employment without regard to race, color, religion, sex (including pregnancy, childbirth, or related medical conditions), gender identity, national origin, ancestry, citizenship, age, physical or mental disability, legally protected medical condition, family care status, military or veteran status, marital status, domestic partner status, sexual orientation, or any other basis protected by local, state, or federal laws. Applicants with questions about access or requiring a reasonable accommodation for any part of the application or hiring process should contact the Talent Network by phone at (408) 503-2194.

Employment at Infineon is contingent upon proof of your legal right to work in the United States under applicable law, verification of satisfactory references and successful completion of a background check and drug test, and signing all your on-boarding documents .

In some instances, if applicable, U.S. export control laws require that Infineon obtain a U.S. government export license prior to releasing technologies to certain persons. This offer is contingent upon Infineon's ability to satisfy these export control laws as related to your employment and anticipated job activities. The decision whether or not to submit and/or pursue an export license to satisfy this contingency, if applicable, shall be at Infineon's sole discretion.

IMPORTANT NOTICE:
Infineon is requiring all new U.S. employees and contractors to be fully vaccinated against COVID-19. Full vaccination is defined as two weeks after both doses of a two-dose vaccine or two weeks since a single-dose vaccine has been administered. Anyone unable to be vaccinated, either because of a sincerely held religious belief or a medical condition or disability that prevents them from being vaccinated, can request a reasonable accommodation.

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