Scenario:

I want to drive 2 Infineon CoolGaN IGO60R070D1 in half-bridge configuration. I know there is a dedicated driving solution for this (1EDi-G1) but I was wondering if I can use the 2EDi for PCB space reasons.

Solution:

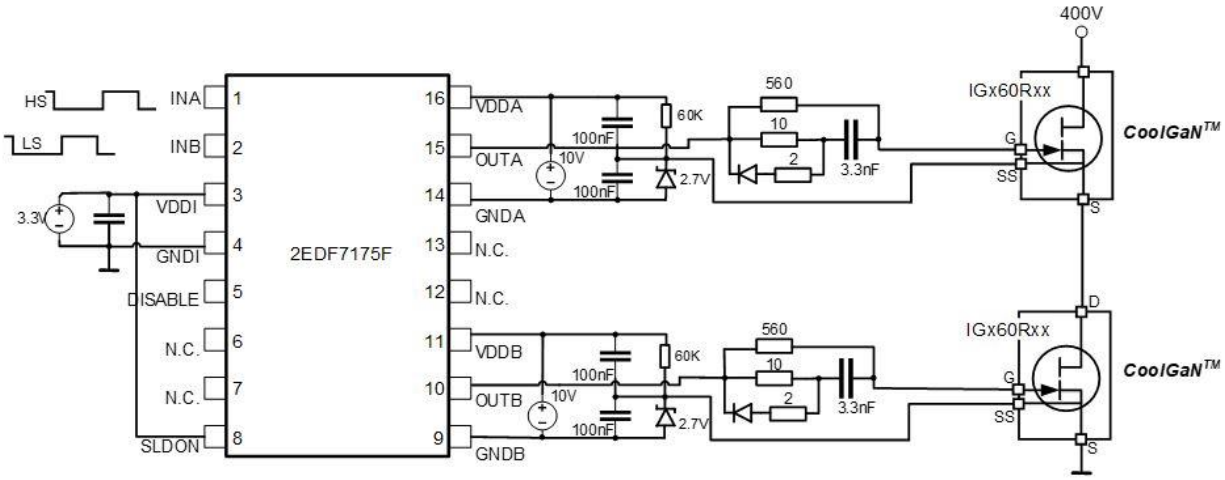
Yes, of course. Link shows an Infineon application note explaining how to drive the IGO60R070D1. Actually, the application note refers to the 1EDI20N12AF, which is a different single-channel isolated gate driver for MOSFET; however, the presented concepts are valid as well for the 2EDi dual-channel gate drivers' family.

1A/2A peak source and sink currents are good enough to properly switch the IGO60R070D1. I suggest you to use the 2EDS8165H if you need reinforced isolation (LLC with microcontroller in secondary) or 2EDF7175F if you only need functional isolation (Totem Pole PFC with PFC microcontroller).

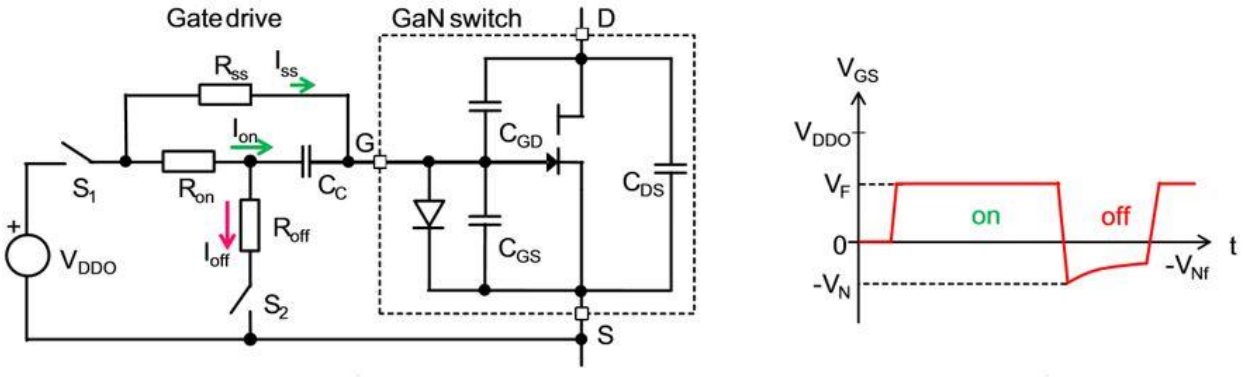
Below you find an example using the 2EDF7175F to drive a GaN based half-bridge. The gate drive scheme is using the well-known RC circuit on the gate used to differentiate the static and dynamic behavior of the GaN switch. The theory behind the dimensioning of those resistances is well described in the mentioned application note. You can find guidelines for the dimensioning also in the 1EDi-G1 datasheet (link, Chapter 8).

A constant current of 10mA must be feed to the switch in steady-state operation (V_{GS} fixed to ~3.3V); considering that 8V is a common choice for the driver positive supply, a steady state resistance of 560Ω is recommended. Of course, 560 Ω is too big to provide enough source and sink currents for proper switching of IGO60R070D1; for that reasons, a different low-ohmic switching path is necessary. Moreover, source and sink path are usually split since a very low sink resistance is usually preferred to avoid false turn-on due to Miller coupling.

Below you find a reference design for driving IGO60R070D1 CoolGAN with the 2EDF7175F driver.



You would notice that, compared to the reference circuit in the application note, a two-split bypass capacitance structure is added in the picture above. The reasons are explained further in this answer.
As you probably know, the RC is also responsible to generate a negative V_{GS} in OFF state, important to avoid shoot-through events particularly critical when using GaN due to the very low gate threshold (~1V). However, this voltage is decreasing during the OFF state due to RC discharge as described in the 1EDi-G1 datasheet (Figure below).



1st consequence is that the voltage available at the beginning of the turn-on phase changes with OFF state duration; this leads to a consequent dependence of switching dynamics on duty cycle and frequency. 2nd problem can happen for example in start-up or burst-mode when the MOSFETs are not switching for long time; in this situation, the coupling gate capacitance Cc discharges and the negative voltage is no longer available in the next turn-on (possible shoot-through in the next turn-on called "1st pulse problem").

With a four-output switches-based approach, the optimized GaN driver (1EDi-G1) solves the 1st problem pulling down to 0V the negative V_{GS} in turn-off after a sufficiently safe time TNEG. The 2nd problem is solved with a 3rd negative V_{GS} level; the driver autonomously recognizes long no-switching times and pull the V_{GS} from 0V down to $-V_{DDO}$ to avoid the 1st start-up problem. This is the reason why the 1EDi-G1 is optimized for GaN switches driving.

With 2EDi and any normal driver, those described features are not available. However, if you want to use the 2EDi you can solve the 2nd problem described before using a negative "supply voltage" that keeps the V_{GS} down at the same level in OFF-state. The most convenient configuration from cost and space point of view is the one based on split capacitance. This one, in fact, is generating the negative supply without an additional auxiliary supply but simply using an 8V zener diode. Using a 10V auxiliary supply, 8V and -2V supplies are available in turn-on and turn-off; in OFF-state after a negative peak linked to the RC charge distribution, the V_{GS} is kept constant to the safe level -2V.

Compared to 1EDi-G1, the driving solution based on 2EDi can benefit from price and power density. However, a constant negative V_{GS} is always present in turn-off with consequent bigger reverse conduction losses when compared to 1EDi-G1.

In a soft configuration as the LLC and considering a good layout, the gate ringing could not be so critical. In this case, you can consider the single supply option described in the application note (link); it is your choice. In this case, bootstrap is also an option.

For completeness, you find below the simulation results of the 2EDi reference circuit shown before.