Recommendations for Board Assembly of Infineon Wafer Level Ball Grid Array Packages



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Acronyms and Abbreviations

AOI	Automated Optical Inspection
AXI	Automated X-ray Inspection
BGA	Ball Grid Array
ESD	Electrostatic Discharge
eWLB	embedded Wafer-Level Ball Grid Array
IC	Integrated Circuit
I/O	Input/Output
MSL	Moisture-Sensitivity Level
NSMD	Non-Solder Mask Defined
PG	Plastic Green
PCB	Printed Circuit Board
RDL	Redistribution Layer
SAC	Tin Silver Copper (SnAgCu)
SG	Silicon Green
SMD	Solder Mask Defined
SMD	Surface-Mount Device
SMT	Surface-Mount Technology
UFWLP	Ultra-thin profile Fine pitch Wafer-Level Package
WFWLB	Very, Very thin profile Fine pitch Wafer Level Ball grid array
WLB	Wafer-Level Ball Grid Array
WLP	Wafer-Level Package
XFWLB	Extremely thin profile Fine pitch Wafer Level Ball grid array

1 Package Description

This document provides information about the board assembly of Level Packages (WLP), Wafer-Level Ball Grid Array (WLB) packages and embedded Wafer-Level Ball Grid Array (eWLB) packages. The package and component types cover a wide range of chip sizes and numbers of terminals. The terminals consist of lead-free solder balls that allow for assembly by Surface Mount Technology (SMT). Ball pitches of 0.4 mm and of 0.5 mm are available.

This document does not discuss Ball Grid Array (BGA) packages and wafer-level packages without solder balls. These package families are described in a separate document.

1.1 WLP Package Type

Infineon WLP feature a silicon body that can be rectangular or square. They are chip-size packages without redistribution layer, additional passivation, dielectric, or solder-stop layer. The solder ball terminals feature a size of 250 or 300 µm. The typical number of Input/Output connections (I/O) is up to 12. **Figure 1** shows examples of the WLP package family.

- SG-UFWLP packages

SG = Silicon Green
U = Ultra-thin profile
F = Fine pitch
WLP = Wafer-Level Package



Figure 1 Example of a WLP package.

1.2 WLB Package Type

Infineon WLB feature a silicon body that can be rectangular or square. They are chip-size package with a fan-in redistribution and a dielectric/solder-stop layer. The solder ball terminals feature a size of 230, 250 or 300 µm. The typical number of I/O connections is up to 25. **Figure 2** shows an example of the WLB package family.

- SG-WFWLB packages
- SG-XFWLB packages

SG = Silicon Green
W = Very, Very thin profile
X = Extremely thin profile
F = Fine pitch
WLB = Wafer Level Ball grid array

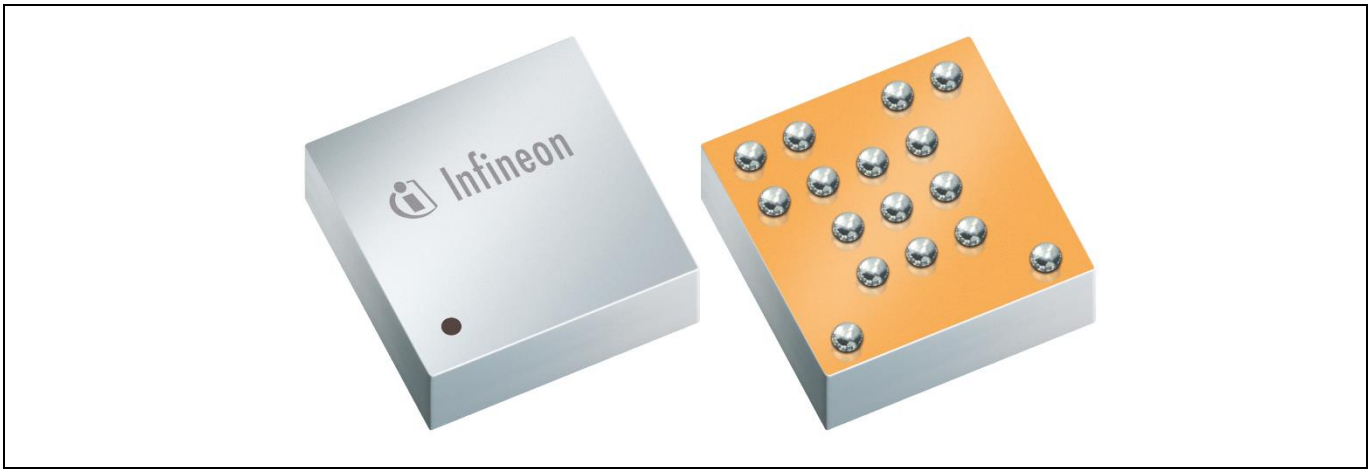

Figure 2 Example of WLB packages.

1.3 Embedded WLB Package Type

Infineon embedded WLB feature a body made of mold compound that can be rectangular or square. They are chip scale packages with fan-in/fan-out redistribution that extends over the silicon die by dielectric material. The I/O side features additional dielectric/solder-stop layers and the opposite side can feature a backside protection. The solder ball terminals feature a size of 250 or 300 µm. The typical number of I/O connections is up to 150. **Figure 3** shows an example of the embedded WLB package family.

- PG-WFWLB packages

PG = Plastic Green
W = Very, Very thin profile
F = Fine pitch
WLB = Wafer Level Ball grid array

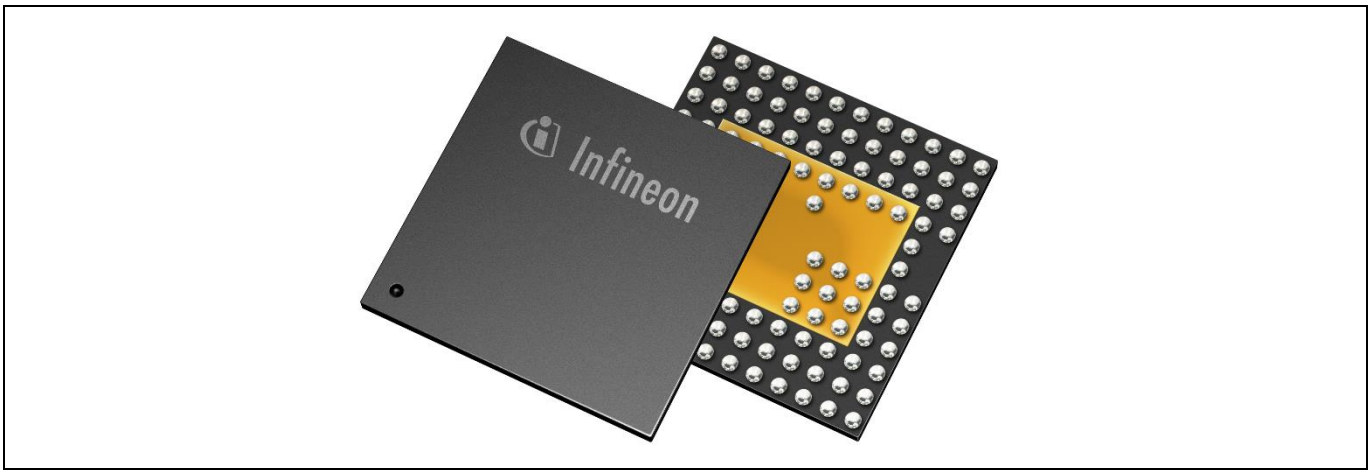

Figure 3 Example of embedded WLB packages.

1.4 Package Features and General Handling Guidelines

General Handling Guidelines

Semiconductor devices are sensitive to excessive electrostatic discharge (ESD), moisture, mechanical handling, and contamination. Therefore, they require specific precautionary measures to ensure that they are not damaged during transport, storage, handling, and processing.

Automatic and especially manual handling of components in or out of the component packing may cause mechanical damage to WLP and WLB package balls and/or silicon body. The mechanical properties of the package body are mainly determined by the silicon, which is much more brittle than the mold compound of plastic package types.

Note: Any manual handling of wafer level ball grid array packages during board assembly should be avoided.

Parameters and settings for automated SMT placement equipment are outlined in detail in **Section 3.3**. In case it is necessary to handle packages for any other purpose such as analysis, plastic tweezers should be used instead of metal ones. Vacuum tweezers would be the ideal choice.

To avoid the risk of damaging the component, bending stress should generally be minimized. In particular, local stress such as tension forces on the WLP, WLB and eWLB packages should be avoided during all handling steps:

- Convex bending of the device with tension stress on the package must be avoided. Such stress conditions could occur during electrical testing, for example, when the forces on top and bottom of the package are applied by probe pins (pogo pins).
- If force is applied to the center of the device's bottom side, the device must be supported on the opposite side to provide a central counterforce to prevent package bending.

After board assembly WLP, WLB and eWLB packages are fixed to the Printed Circuit Boards (PCB) by the solder connection. However, the silicon bodies of WLP and WLB are not protected from the environment. When handling the assembled PCBs protecting the components from any mechanical impact is necessary. One may consider the following items:

- Use support pins for solder-paste printing of the second PCB side.
- Take care during insertion of assembled PCBs into magazines or the housing of the application.
- Use specific clamping or support in adapters for electrical testing, or insertion of the assembled PCBs into the housing of the application.

The silicon body wafer level packages can be protected from mechanical impact by placing the passive components of a PCB design close to them. Due to their increased height (in most cases they should be higher than 0.7 mm) they are acting as distance holders. In case the PCB design does not allow for placing functional passives close to the devices they can also be used in a non-functional "dummy" configuration. The specific dimensions as well as the number of passive components per side need to be chosen according to the package size of the wafer level package to protect. **Figure 4** shows a schematic top view as well as photographs of such a protection design.

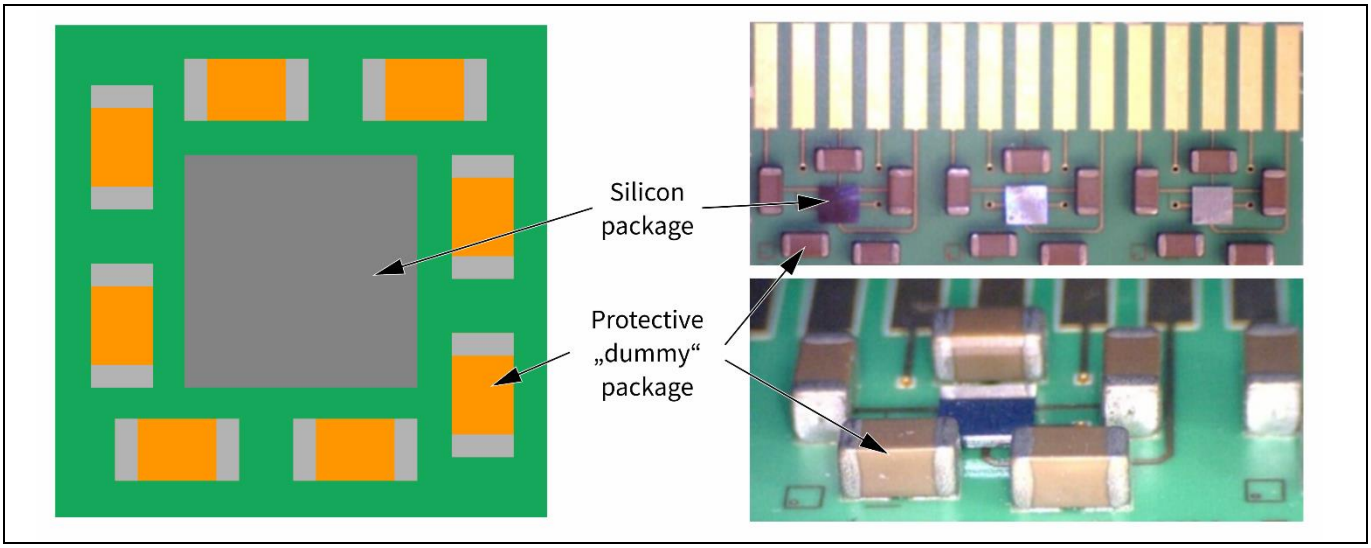

Figure 4 Schematic top view and photographs of showing passive components surrounding a silicon package for mechanical protection.

Processing contaminations of the wafer level components or their packing by foreign material may lead to a device damages affecting the solderability, corrosion tendency or electrical functionality (e.g. electrical shorts due to conductive particles). In many applications, the package must be electrically isolated from its mounting surface. The isolation material has a comparatively high thermal resistance, which raises junction operating temperatures.

For further information about component handling, please refer to the *General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

Package Description

Internal Construction

The chip-size WLP and WLB components feature a silicon body and a similar I/O configuration. The component body of eWLB is exceeding the Integrated Circuit (IC) by plastic mold fan-in/fan-out redistribution. That allows for much larger number of I/O by keeping a chip scale size. The silicon body components are manufactured directly from the wafer. The molded components are singulated by sawing through the plastic between individual units. **Figure 5** to **Figure 7** shows schematic drawings of the inner setup of the Infineon wafer level ball grid array packages.

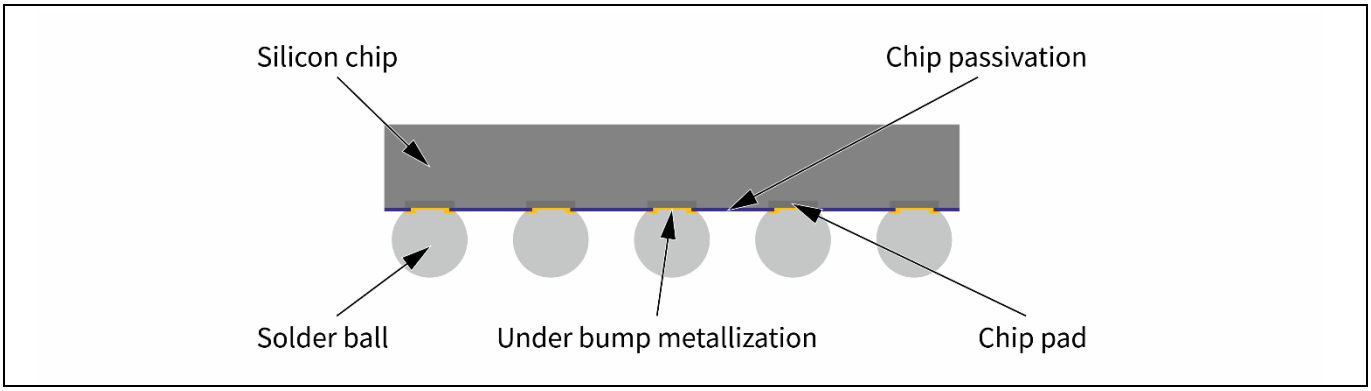

Figure 5 Schematic of the inner setup of typical WLP components.

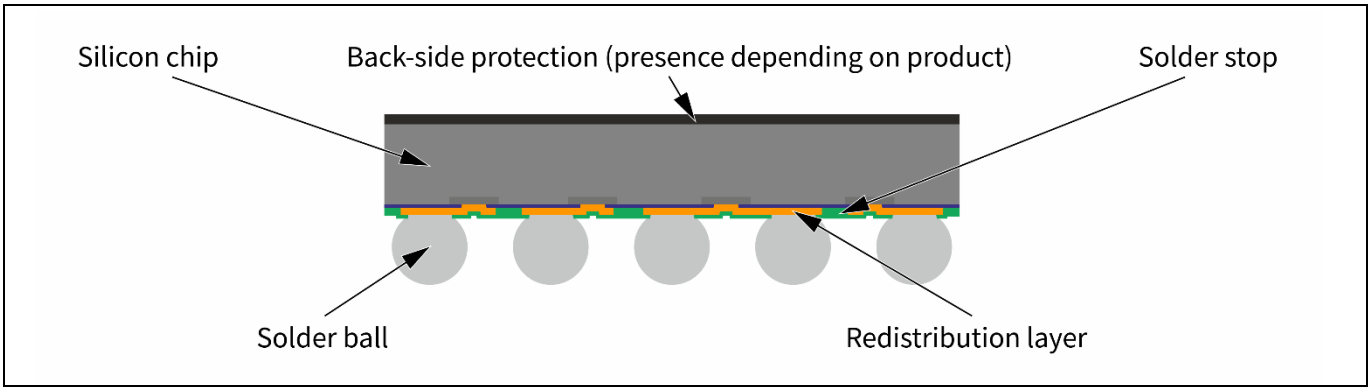

Figure 6 Schematic of the inner setup of typical WLB components.

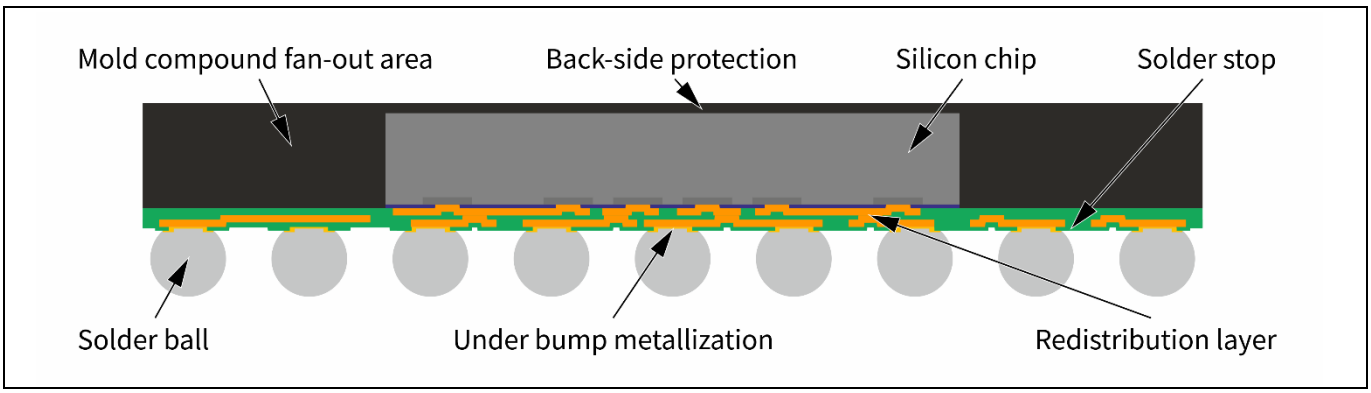

Figure 7 Schematic of the inner setup of typical eWLB components.

Termination Design

Typically WLP and WLB components feature Solder-Mask-Defined (SMD) pads and eWLB feature Non-Solder-Mask-Defined (NSMD) pads. Depending on the specific product, the packages can however also feature the other pad design. **Figure 8** shows schematics of both pad types.

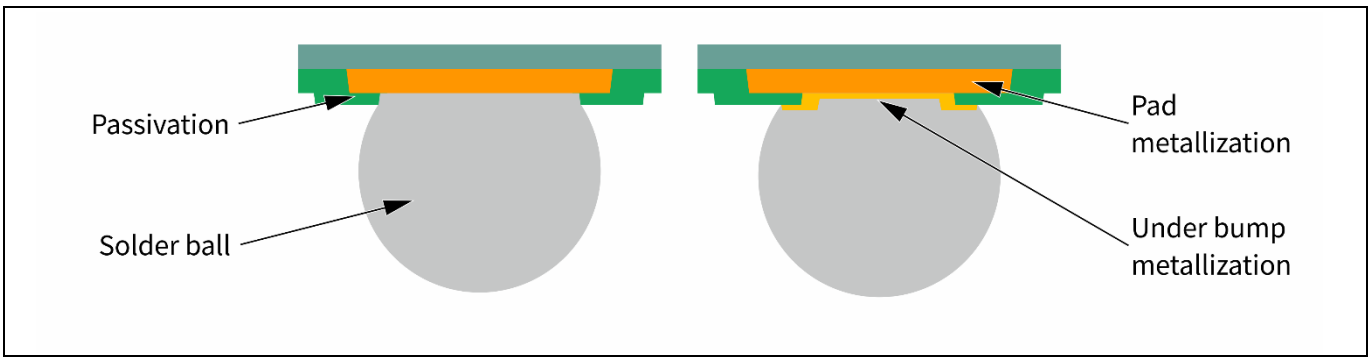

Figure 8 Schematic comparison of a typical SMD ball pad (left) on WLB components and a NSMD ball pad (right) on eWLB components.

2 Printed Circuit Board

2.1 Routing

The array configuration of WLP, WLB and eWLB components implies different concepts for routing the signal, power, and ground pins on the PCB compared with e.g. leadframe-based components. Typically fine-line PCBs with conductor width/spacing of 100 µm or less (e.g. 75 µm) are necessary for routing. The specifics of the PCB design to be used strongly depend on the board technology (conventional technology with drilled vias, build-up technology with microvias), the conductor width/spacing, number of metal layers, and electrical restrictions.

The PCB design and construction are key factors for achieving highly reliable solder joints. WLP, WLB and eWLB packages should not be placed opposite one another on the PCB (if double sided mounting is used), because this stiffens the assembly and results in earlier solder-joint fatigue compared to a design where the components are offset. Furthermore, the board stiffness itself has a significant effect on the reliability (temperature cycling) of the solder-joint interconnect if the system is used in critical temperature-cycling conditions. The lower bending stiffness of thinner boards (e.g. 1.0 mm) improves solder-joint reliability (temperature cycling) compared to thick boards (e.g. 1.6 mm).

2.2 Pad Design

The quality and reliability of interconnect solder joints to the board are affected by:

- Pad type (Solder Mask Defined or Non-Solder Mask Defined)
- Specific pad dimensions
- Pad finish (also called metallization or final finish)
- Via layout and technology

The NSMD pad type on PCB is preferred since it allows for appropriate pad precision and good board reliability. **Figure 9** shows the recommended NSMD PCB pad design for BGA packages. The dimensions recommended for individual pad diameter and solder mask clearance depend on the specific component, and can be found in the package data base that is available on the Infineon web page [1]. Please choose a specific package when searching the data base, which will then show an example of the stencil aperture layout for each package. Design details will depend on the PCB technology used, the capability of the suppliers, and the planned routing.

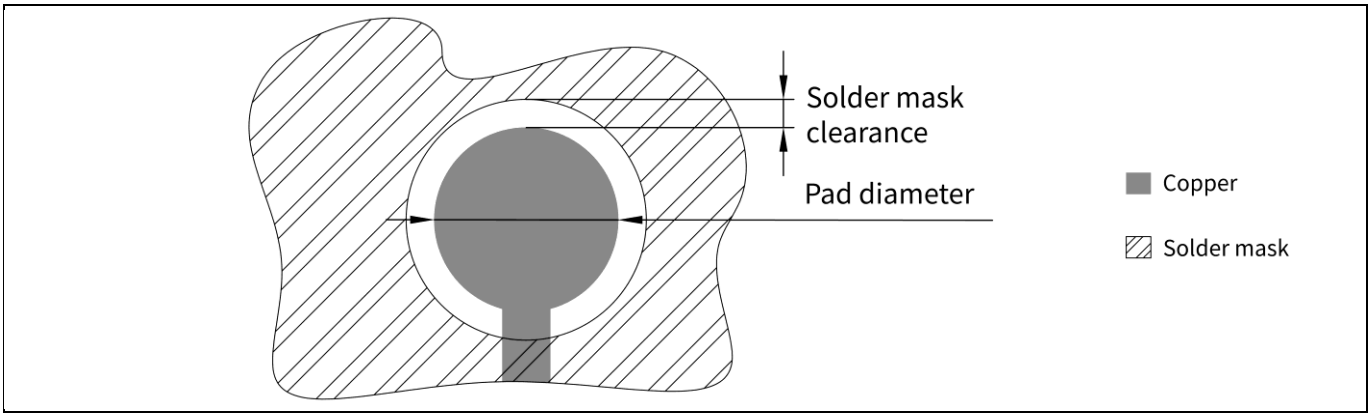

Figure 9 Recommended NSMD PCB pad design. Pad diameter and solder-mask clearance depend on the individual components, and can be found in the Infineon package data base that is available on the Infineon web page [1].

Figure 10 shows an example of a eWLB solder ball with NSMD pad design on the component and PCB side. Investigations on board-level reliability within Infineon have shown that in most cases a NSMD PCB pad results in the highest solder-joint reliability. The NSMD configuration allows the solder to grip the PCB pad sidewalls, improving the reliability of the solder joint.

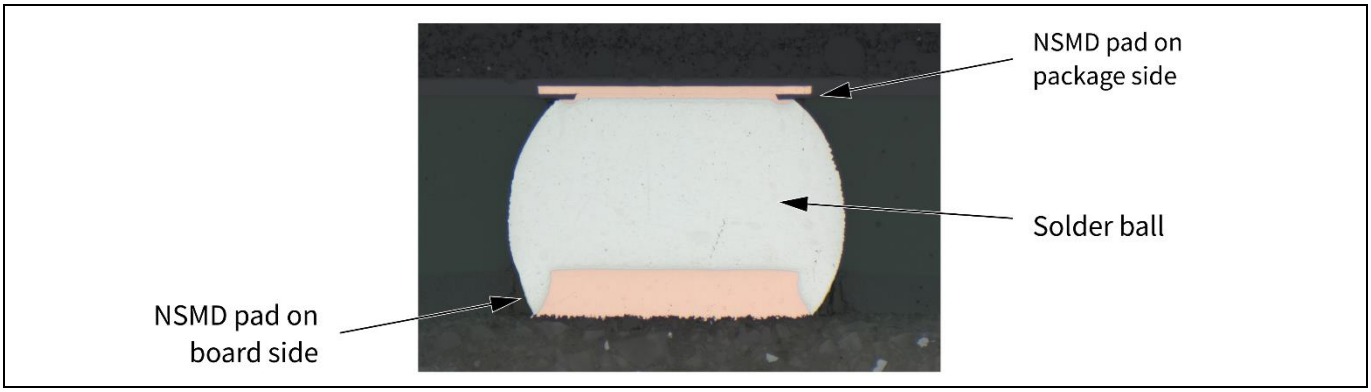

Figure 10 Cross-section of an eWLB solder ball with NSMD pad on the component side and NSMD pad on the board side. The latter allows the solder to "grip" the pad sidewalls increasing the board level reliability of the component.

If any kind of via hole is placed inside the pad area, its opening should be closed by plugging or plating in order to prevent solder flowing into it. If closed microvias are placed inside the pads, their intersection with the pad should be as flat as possible. Deep dips inside the pads may cause voiding in the solder joint even if the microvia opening is closed.

For further information about PCB pad and via design, please refer to the *General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

3 PCB Assembly

3.1 Solder Paste Stencil

In SMT, the solder paste is applied onto the PCB metal pads by stencil printing. For low-pitch components such as Infineon WLP, WLB and eWLB packages a regular cleaning cycle (wet or dry) of the stencil is advisable. The volume of the printed solder paste is determined by the stencil aperture and the stencil thickness.

The stencil aperture for WLP, WLB and eWLB packages should be circular. The stencil thickness can vary between 80 and 100 µm depending on aperture area ratio, the stencil material, and the aperture diameter. The aperture diameter should be at least of the size of that of the metal pad on the PCB. Overprinting it may provide a better solder paste release, but also increases the risk for solder bridging.

Specific stencil aperture recommendations can be found in the package data base that is available on the Infineon web page [1]. Please choose a specific package when searching the data base, which will then show an example of the stencil aperture layout for each package.

To ensure a uniform and sufficient solder paste transfer to the PCB, laser-cut stencils (mostly made from stainless steel) or electroformed stencils (nickel) are preferred. For individual design adaptations to use the optimum amount of solder, the stencil thickness, the PCB pad finish, quality and solder masking, the via layout, and the solder paste type should be considered. In every case, application-specific experiments are recommended.

For further information about solder stencil design, please refer to the *General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

3.2 Solder Paste

Pb-free solder pastes typically contain some type of SnAgCu alloy (SAC solder with typically 1-4% Ag and <1% Cu). The most common alloy is SAC305 (3.0% Ag and 0.5% Cu). The average alloy particle size must be suitable for printing the solder stencil aperture dimensions. Type 4 pastes are recommended for optimum transfer efficiency during the assembly of WLP, WLB and eWLB components. Test results have however shown, that for pitches larger than 0.5 mm Type 3 pastes can work well depending on the specific stencil transfer.

The solder alloy particles are dispersed in a blend of liquid flux and chemical additives (approx. 50% by volume or 10% by weight), forming a creamy paste. The flux and chemical solvents have various functions such as adjusting the viscosity of the paste for stencil printing or removing contamination and oxides from the surface.

The solder paste solvents have to evaporate during reflow soldering, while residues of the flux will remain on the solder joint. The capacity of the flux additive for removing oxides is given by its activation level, which also affects the potential need for removing the flux residuals after the assembly. For area-array packages such as WLB, WLP and eWLB, in which the solder joint is formed mainly on the bottom side, a “no-clean” paste is recommended to avoid subsequent cleaning underneath the package. The small gaps make cleaning highly difficult if not impossible. Certain precautions have to be taken if any kinds of flux residues remain on the board prior to any kind of coating.

Generally, solder paste is sensitive to ageing, temperature, and humidity. Please follow the handling recommendations of the paste manufacturer.

3.3 Component Placement

Although the self-alignment effect due to the surface tension of the liquid solder will support the formation of reliable solder joints, the components have to be placed accurately depending on their geometry. Positioning the packages manually is not recommended, especially for packages with small terminals and pitch. An automated pick-and-place machine is recommended to obtain reliable solder joints.

Component placement accuracies of +/-50 µm and less are obtained with modern automatic component placement machines using vision systems. With these systems, both the PCB and the components are optically measured and the components are placed on the PCB at their programmed positions. The fiducials on the PCB are located either on the edge of the PCB for the entire PCB, or at additional individual mounting positions (local fiducials). These fiducials are detected by a vision system immediately prior to the mounting process. Most such vision systems provide special lighting and algorithms for area array packages. For ball grid array packages it is recommended to use the ball recognition instead of the component outline recognition for centering. This approach eliminates potential tolerances between the solder ball and the package.

The automated pick-and-place is typically done using vacuum nozzles. To avoid pick-up issues (e.g. picking up the component edgewise), the size of the nozzle should be slightly smaller than the package outline. Choosing the wrong nozzle might lead to damage of the silicon body edge or early wear out of the nozzle. The preferred nozzle materials are rubber and plastic. Metal and ceramic tools may cause scratches on the component surface and should therefore be avoided.

Note: *Rubber and plastic are preferred pick-and-place vacuum nozzle materials. Metal or ceramic tools may cause damages to the component surface.*

When placing WLP, WLB or eWLB packages, the placement force should be sufficiently high, while avoiding excessive placement force that can squeeze the solder paste out of its intended location and cause solder joint shorts. Typical pick-and-place nozzle forces stay below 5 N. Simulations and real board assemblies with Infineon silicon body WLB packages have shown, that there are no mechanical damages to be expected from a centric positioned nozzle even at forces of 50 N. The data were gained using a nozzle size covering 25% of the package body. A schematic of the simulation model can be seen in **Figure 11**.

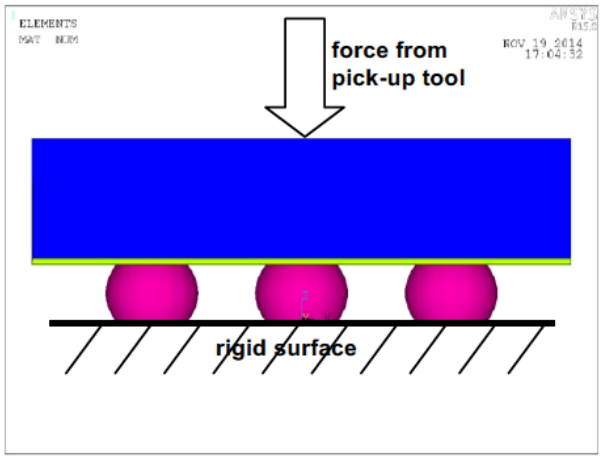

Figure 11 Schematic of the simulation model for nozzle pick force assessements.

For further information about component placement, please refer to the *General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

3.4 Reflow Soldering

For printed PCB assembly of the BGA components, the widely used method of reflow soldering in a forced convection oven is recommended. Soldering in a nitrogen atmosphere can generally improve the solder joint quality but is not necessary to create a reliable joint.

The soldering profile should be in accordance with the recommendations of the solder paste manufacturer to achieve optimal solder-joint quality. The position and the surrounding of the component on the PCB, as well as the PCB thickness, can influence the solder joint temperature significantly.

Minimum Reflow Conditions

The lower temperatures and durations of an optimal reflow profile shall stay above those of the wettability test profile of a solderability qualification. The solderability of the terminals of Infineon components is tested according to the standards IEC 60068-2-58 and J-STD-002 [2][3].

Maximum Reflow Conditions and Cycles

Components that are Moisture-Sensitivity Level (MSL) classified by Infineon have been tested by three reflow runs in accordance with the J-STD-020 standard, including a double-sided reflow and one rework cycle. The maximum temperatures must not be exceeded during board assembly. Please refer to the product barcode label on the packing material that states this maximum reflow temperature according to the J-STD-020 [4] standard as well as the MSL according to the J-STD-033 standard [5].

WLP, WLP and eWLB packages are generally suited for double-sided PCB mounting. That means that both sides of the PCB are fitted and reflowed one after another. As a consequence, the side that was initially assembled experiences two reflow cycles. During the second cycle, the components are hanging upside-down. Therefore, during the peak zone of the reflow profile (where the solder is liquid), the components are only held by wetting forces of the molten solder. Gravity acting in the opposite direction will elongate the solder joints, unlike joints on the top side, where gravity forces the components nearer to the PCB surface. This shape will be frozen during cooling and therefore will result in a higher stand-off on the bottom side after the reflow process. Any mechanical impacts on components that are soldered upside down should be avoided.

BGA components have a natural tendency for warpage due to its layered construction. During package development projects the warpage is addressed by specific investigations in order to minimize a potential impact on the solder joint formation.

For further information about reflow soldering, please refer to the *General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

4 Cleaning

After the soldering process, some flux residues will remain on the board, especially near the solder joints. Generally, cleaning beneath a component with bottom-only terminals is difficult due to the small gap between the component body and the PCB. Therefore, a “no-clean” flux is recommended whose residues usually do not have to be removed after the soldering process.

In case the solder joints have to be cleaned, the cleaning method (e.g. ultrasonic, spray, or vapor cleaning) and cleaning solution have to be selected while taking into account the type of package, the flux used in the solder paste (rosin/resin-based, water-soluble, etc.) as well as the environmental and safety aspects. Even small residues of the cleaning solution should be removed or dried out very thoroughly. For recommended cleaning solutions, please contact the solder paste or flux manufacturer.

5 Underfill

Infineon reliability tests (e.g. drop test, temperature cycling on board, and bend test) without underfilling have been of positive result, passing typical market requirements. Based on that knowledge, additional underfilling is not necessary for WLP, WLB and eWLB packages, and it is therefore strongly recommend not to use underfill material. Depending on the properties of the underfill material and properties of other parts of the application (such as the PCB), underfilling can also have a negative effect on the reliability of solder joints or the package construction in board level condition.

In case of questions on underfilling WLP, WLB or eWLB components, please contact your local sales, application, or quality engineer.

6 Inspection

6.1 Optical Solder Joint Inspection

A visual inspection of WLP, WLB or eWLB solder joints with conventional AOI (Automated Optical Inspection) systems is not possible. As can be seen in **Figure 12**, even a side-view can only reveal a certain number of the terminal solder balls in their area array configuration.

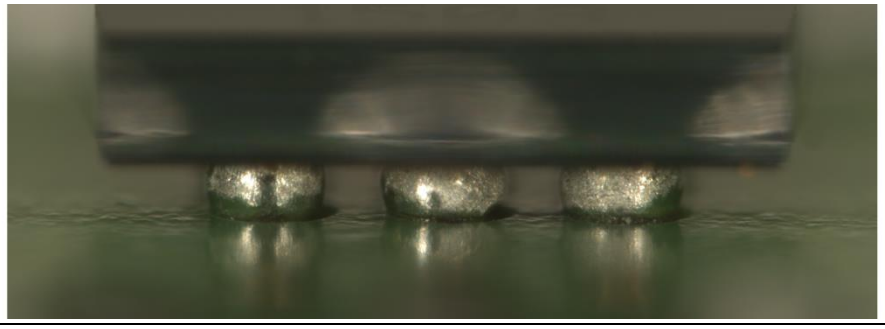

Figure 12 Side view of a WLB package mounted on NSMD PCB pads. The component silicon body and the solder ball terminals can be seen from top to bottom.

For engineering tasks, cross-sectioning can offer detailed information about the solder joint quality. Due to its destructive character, cross-sectioning during monitoring is naturally not practical.

6.2 X-Ray Solder Joint Inspection

Automated X-ray Inspection (AXI) systems are appropriate for efficient inline control of components such as WLP, WLB and eWLB whose terminals cannot be inspected properly by optical systems. AXI systems are available as 2D and 3D solutions. They usually consist of an X-ray camera and the hardware and software needed for inspection, controlling, analyzing, and data transferring routines. These reliable systems enable the user to detect soldering defects such as poor soldering, bridging, voiding, and missing parts. However, other defects such as broken solder joints are not easily detectable by X-ray.

Figure 13 shows a section of an X-ray photograph of a properly soldered WLB component. Solder balls as well as the Redistribution Layer (RDL) are visible. X-ray images might also reveal a certain amount of voiding in the solder balls. The extent of voiding depends on the solder paste, the reflow profile, and the presence of microvias-in-pad. For the acceptability of electronic assemblies, please refer also to the IPC-A-610 standard [6].

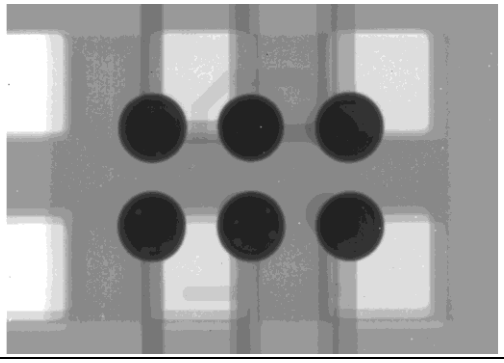

Figure 13 X-ray photograph of a properly soldered WLB component. The solder balls and the RDL lines are visible.

7 Rework

Single solder joint repair of bottom-only terminated packages is highly difficult, if not impossible, and is therefore generally not recommended. Furthermore, the reuse of de-soldered components is not recommended. The de-soldered components should be replaced by new ones.

A rework process is commonly done on special rework equipment. There are various systems available that meet the requirements for reworking SMD packages. All handling guidelines discussed in this document have to be respected. Special focus should be on the following items:

- It is recommended to use only vacuum-supported tools comparable to what is used in the pick-and-place process for handling WLP, WLB and eWLB packages. As for pick-and-place, the right nozzle size should be chosen. It is also important not to apply any uncontrolled force to the package during rework processes.
- • Due to the decreased automation level given by the general rework approach, even higher care compared to standard assembly must be taken. Tools that do not damage the component mechanically have to be chosen. Mechanical forces that do not necessarily cause visible external damage can still cause internal damage that reduces the component's reliability. A proper handling system with vacuum nozzle may be the gentlest process and is therefore recommended. However, the impact of rework tools has to be assessed properly. In general, more manual handling increases the effort for documentation, training, and monitoring of the rework process(es).
- During rework, special care must be taken concerning the proper moisture level of the component according to the J-STD-033. Drying the PCB and the component prior to rework might be necessary. A proper drying procedure for SMD packages is described in the international J-STD-033 standard [5]. Please also refer to the recommendations of your PCB manufacturer and take all specific needs of components, PCB, and other materials into account.
- Whatever heating system is used (hot air, infrared, hot plate, etc.), the applied temperature profile at the component must never exceed the maximum temperature according to the J-STD-020 standard. Depending on the specific heating profile used during rework, components adjacent to the mounting location might also experience a further "reflow run" in terms of the J-STD-020 standard [4]. Internal investigations have shown that the temperature profile must be recorded.

If a device is suspected to be defective and a failure analysis is planned, Infineon usually expects customers to desolder the component prior to return to Infineon. The component shall be returned in a proper condition according to the original package outlines.

In some special cases such as solder joint inspection Infineon may request that the PCB or part of the PCB with the component still attached should be sent to Infineon.

Note: *Before returning a device for failure analysis at Infineon, please clarify the return condition of the suspected component (ie onboard or desoldered) with the Infineon Application Engineer or Customer Quality Manager who supports your company.*

For further information about component rework on PCB, please refer to the *General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

8 References

[1] Infineon: Packages. www.infineon.com\packages.

[2] International Electrotechnical Commission: IEC 60068-2-58. Environmental testing - Part 2-58: Tests - Test Td: Test methods for solderability, resistance to dissolution of metallization and to soldering heat of surface mounting devices (SMD).

[3] Electronic Components Industry Association, Assembly and Joining Processes and JEDEC Solid State Technology Association Committee: EIA/IPC/JEDEC J-STD-002. Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires.

[4] JEDEC Solid State Technology Association: IPC/JEDEC J-STD-020. Moisture/Reflow Sensitivity Classification for Nonhermetic Surface Mount Devices.

[5] JEDEC Solid State Technology Association: IPC/JEDEC J-STD-033. Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices.

[6] Association Connecting Electronics Industries: IPC-A-610. Acceptability of Electronic Assemblies.

Revision History

Page or reference	Major changes since the last revision
Section 7 “Rework”	Update of sample conditions in case of return.
Entire document	Editorial review.

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