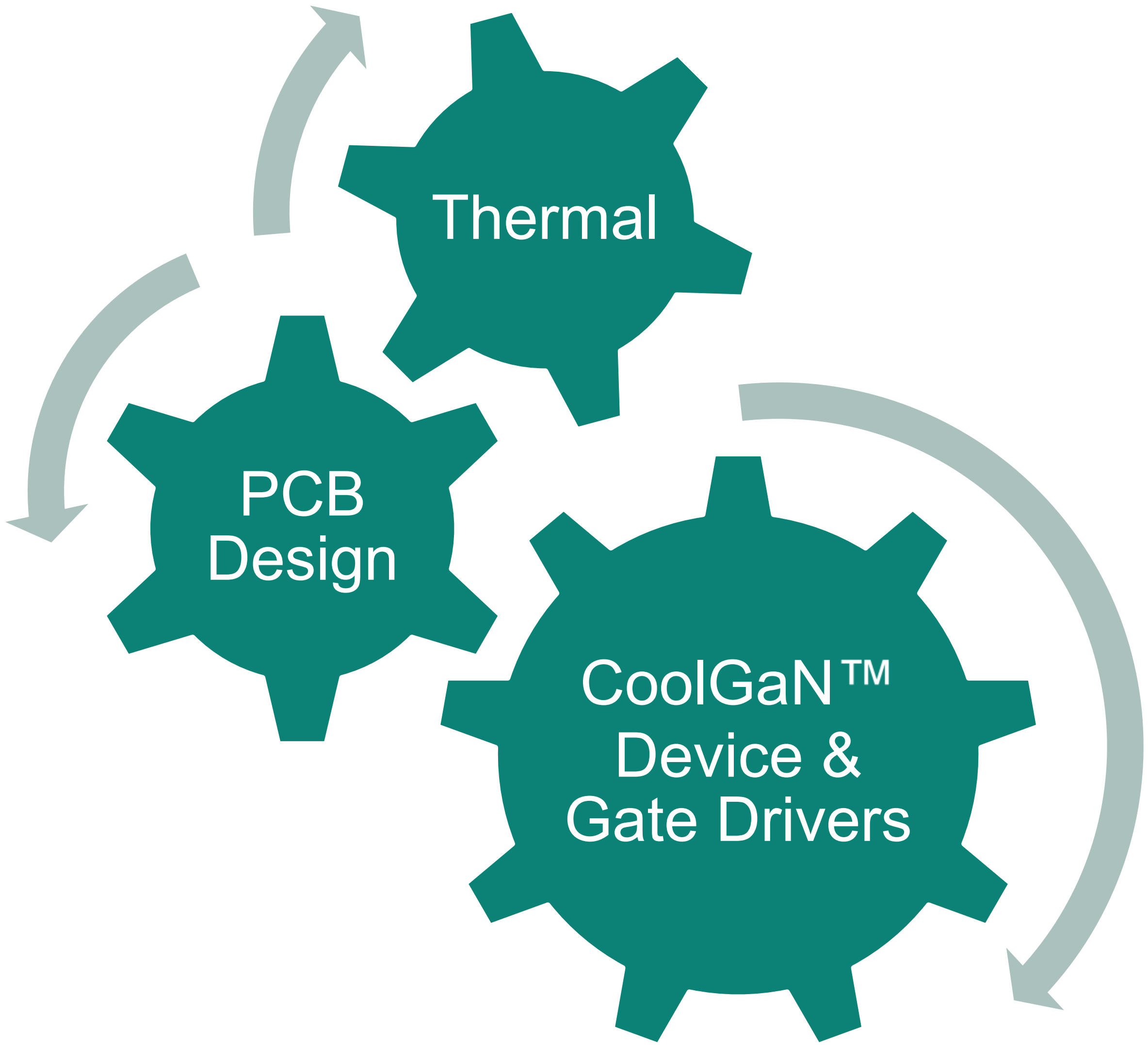
Unlocking higher performance with CoolGaN™: Design, Layout and Thermal management

March 26, 2026

Agenda



Technology of GaN & pushing more power with CoolGaN™

Technology of Gallium Nitride (GaN)

- Gallium Nitride (GaN) is creating an **innovative shift** throughout the power electronics world.
- Gallium Nitride is a **binary III/V** direct bandgap semiconductor that is well-suited for high-power transistors capable of **operating at high temperatures**.
- Gallium Nitride is coming to market as the technology solution for next generation demands in **efficiency, power density and system cost**. **GaN will replace Silicon** in applications such home appliances, drones, robotics, adapters & chargers and all areas of SMPS.

Properties	Silicon	SiC-4H	GaN
Band gap (eV)	1.1	3.2	3.4
Critical field (MV/cm)	0.3	2.2	2.5
Electron mobility ($cm^2/V*sec$)	1350	900	1900
Thermal conductivity (W/cm^2K)	1.5	3.8	1.5

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Positioning of technologies

Technology	Voltage	$R_{DS(on)}$*E_{oss}	$R_{DS(on)}$*Q_g	$R_{DS(on)}$*Q_{oss}	$R_{DS(on)}$*Q_{rr}
Silicon	600 V	100%	100%	100%	100%
SiC	650 V	88%	41%	13%	9%
GaN	**650 V**	**91%**	**6%**	**11%**	**0%**

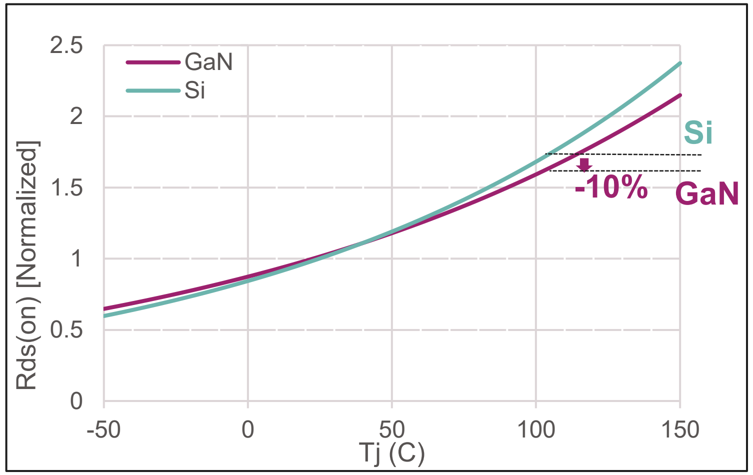
- **GaN demonstrates significant advantages in dynamic performance, showcasing drastically lower E_{oss}, Q_g, Q_{oss} & Q_{rr} compared to Si and SiC.**
- **GaN delivers high efficiency and minimal switching losses, making it best-suited technology for high-performance and fast-switching applications.**

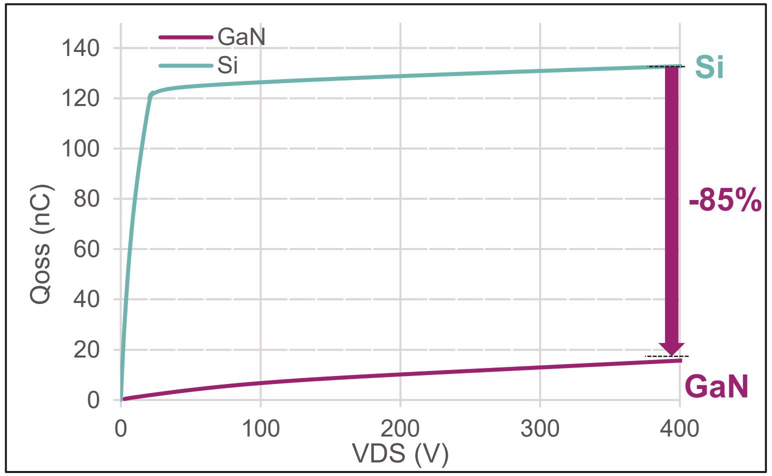
Value propositions of GaN

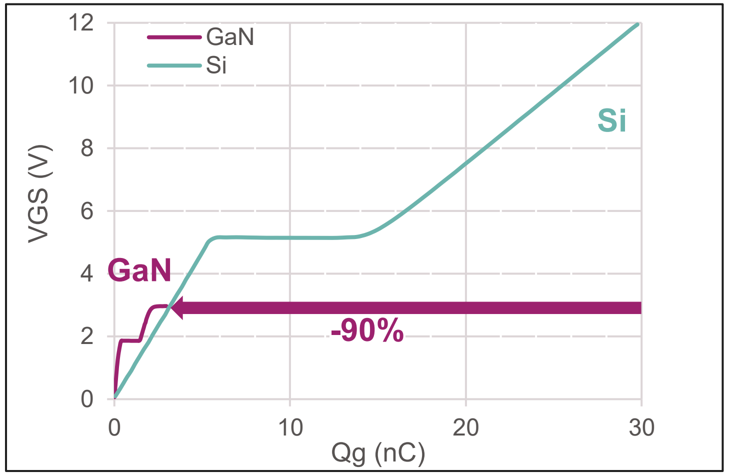
- ↓ **Reduced weight**
- ↓ **Reduced size**
- ↓ **Reduced cost**
- ↑ **Increased energy efficiency**
- ↑ **Higher thermal performance**

Pushing more power with CoolGaN^{TM}

CoolGaN™ Transistor vs Si MOSFET







10% lower $R_{DS(on)}$*temperature coefficience:

- Enabling **higher power and efficiency** and simulataneously around 10% **lower temperature**

85% lower Q_{oss}:

- Enabling **high-frequency operation**
- **Increasing power density** and **improving efficiency**

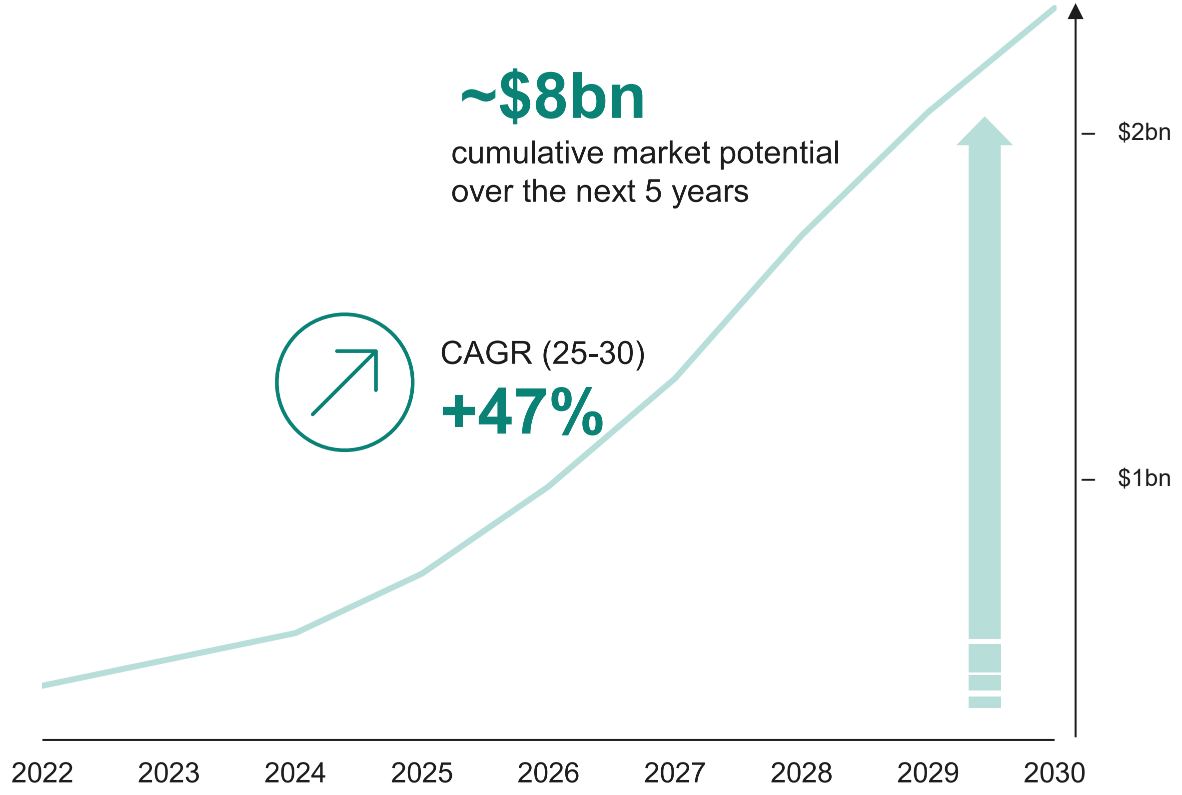
90% lower Q_g:

- Enabling **soft-switching** and **high-frequency operation**

CoolGaN^{TM} enables up to 50% higher power and 50% smaller device sizes at 20% lower system cost, thanks to their lower capacitances and better temperature behavior

Positioning of GaN technology

GaN market forecast growing quickly to > $2B



Source: Yole: Power SiC and GaN Compound Semiconductor Market Monitor Q1 2025

- GaN power market is experiencing rapid upward growth with projected CAGR 47%
- The growth trajectory emphasizes the accelerating adoption of GaN technology in market

CoolGaN™

- **Highly efficient for power conversion**
- **Fast turn-on/off speed**
- **Minimum switching losses**
- **Large variety of package option**
- **Enabling simple & fast time-to-market**

High-voltage CoolGaN™ Transistor in-house portfolio
Broad portfolio enables optimized product selection

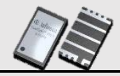
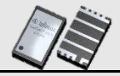
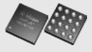
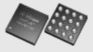
CoolGaN™ Transistor G5								
$R_{DS(on, typ)}$ [mΩ]	650 V						700 V	
	ThinPAK 5x6	DFN 8x8	DSO TSC	ThinPAK 8x8	TOLL	TOLT	DPAK	ThinPAK 5x6
								
500							IGD70R500D2S	
270	IGLR65R270D2						IGD70R270D2S	IGLR70R270D2S
200	IGLR65R200D2						IGD70R200D2S	IGLR70R200D2S
140	IGLR65R140D2	IGLD65R140D2		IGL65R140D2	IGT65R140D2		IGD70R140D2S	IGLR70R140D2S
100/110		IGLD65R110D2		IGL65R110D2		IGLT65R110D2		
65/80		IGLD65R080D2		IGL65R080D2				
55		IGLD65R055D2	IGOT65R055D2	IGL65R055D2	IGT65R055D2	IGLT65R055D2		
45			IGOT65R045D2		IGT65R045D2	IGLT65R045D2		
30/35			IGOT65R035D2		IGT65R035D2	IGLT65R035D2		
20/25			IGOT65R025D2		IGT65R025D2	IGLT65R025D2		

https://www.infineon.com/products/power/gallium-nitride

Infineon CoolGaN™ LV/MV product (G3) portfolio

Sales Code	Voltage class	$R_{DS(on),typ}$	Package type (mm)	Package figure	Positioning

IGC033S101	100 V	2.4 mΩ	PQFN 3x5 BSC		– Lower $R_{DS(on)}$ ➔ higher power rating
					– PQFN package
					  – Smaller and lowest parasitic inductance
					  – Bottom-side and dual-side cooling

IGC033S10S1			PQFN 3x5 DSC		
IGB110S101		9.4 mΩ	PQFN 3x3 BSC		
IGB110S10S1			PQFN 3x3 DSC		
IGB070S10S1		5 mΩ	PQFN 3x3 DSC		
IGC019S06S1	60 V	1.3 mΩ	PQFN 3x5 DSC		
IGC025S08S1	80 V	1.8 mΩ	PQFN 3x5 DSC		
IGC037S12S1	120 V	2.7 mΩ	PQFN 3x5 DSC		
IGC090S18S1*	175 V	6.7 mΩ	PQFN 3x5 DSC		
IGK080B041S	40 V BDS	6 mΩ	WLCSP 1.7x1.7		Lower cost and lower $R_{DS(on)}$ in smaller package size vs. back-to-back Si MOSFETs
IGK120B041S	40 V BDS	9 mΩ	WLCSP 1.2x1.7		
IGK048B041S	40 V BDS	4 mΩ	WLCSP 2.1x2.1		

https://www.infineon.com/products/power/gallium-nitride

Gate drive circuit design for GaN power applications

Gate drive configuration for GaN power transistors

- **Every switch needs a driver – the right driver makes a difference**
- Power electronics applications employ power device switches. And power device switches require optimum gate drive solutions. That's why Infineon offer more than 500 EiceDRIVER™ gate driver IC solutions suitable for any power switch, and any application
- Wide-bandgap semiconductors allow higher electric field strengths and thus result in significantly smaller transistors compared to silicon alternatives
- Consequently, GaN transistors can operate at high switching frequencies without compromising efficiency
- Infineon's gate drivers are designed to drive all **CoolGaN™ Families**
- With proper layout, the same PCB design can drive both switch types

EiceDRIVER™ gate driver ICs >> perfect fit to GaN transistors

CoolGaN™ Transistors

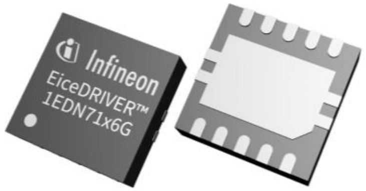
IGC019S06S1
60 V

IGC033S101
100 V

IGC090S20S1
175 V

IGT65R025D2
650 V

EiceDRIVER™ GaN Drivers



1EDN7116G

1EDB7275F

2EDR6258X

Infineon is the only company offering both common enhancement-mode (normally-off) types available in the market: the gate injection transistor (GIT) with an ohmic-gate contact, and the Schottky gate transistor (SG)

Gate driver ICs for GaN transistors up to 200 V

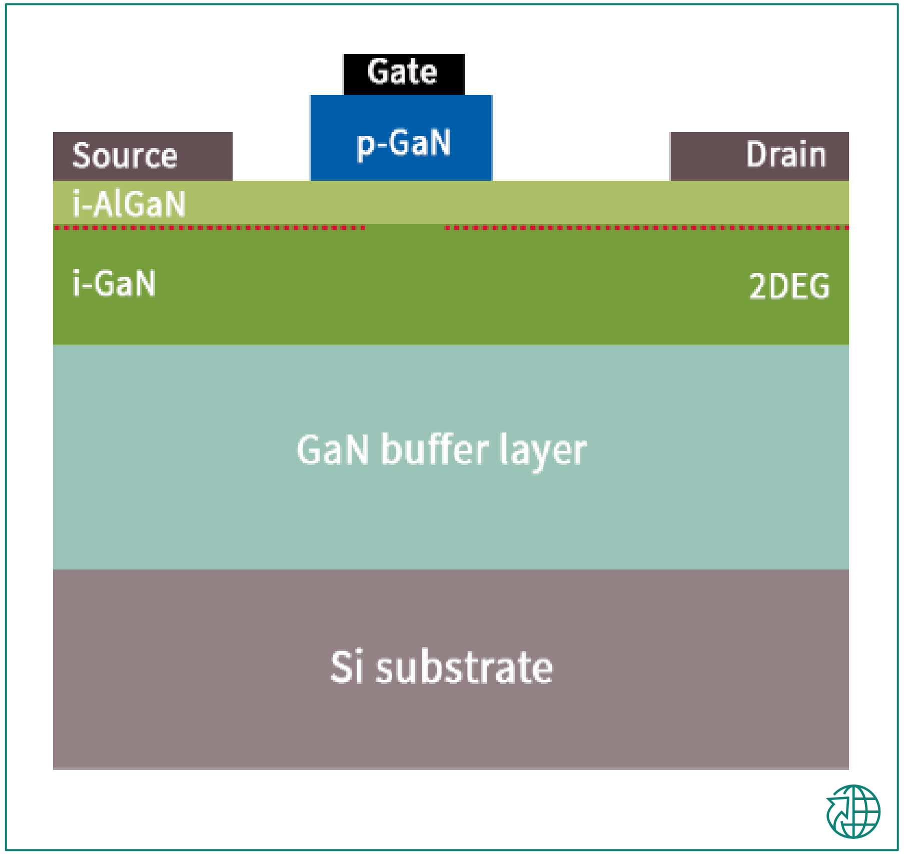


Figure: MV CoolGaN™ SG Transistor device structure

- High efficiency and high power density are key requirements for modern power electronics systems, which are enabled by state-of-the-art GaN transistors
- As shown in the figure, many enhancement-mode GaN transistors utilize a Schottky-type gate to emulate a typical insulated MOSFET gate
- **Gate driver product family:** 2EDF72x8G
- **Best-in-class system solutions for target applications:**
  - eMobility
  - Cordless power tools and gardening tools
  - Multicopters and drones
  - Industrial servo motor drives
  - Robotics, including mobile robots, service robots, and cobots
  - DCDC converters for data centers and telecom infrastructure
  - Solar power optimizers
  - USB-C chargers
  - Wireless power transfer
  - Battery management systems and UPS
  - LED lighting
  - Audio amplifiers

The right gate driver IC help designers achieve the best performance in their GaN-based systems, while simultaneously minimizing R&D efforts and associated costs

Gate driver ICs for GaN transistors 650 V

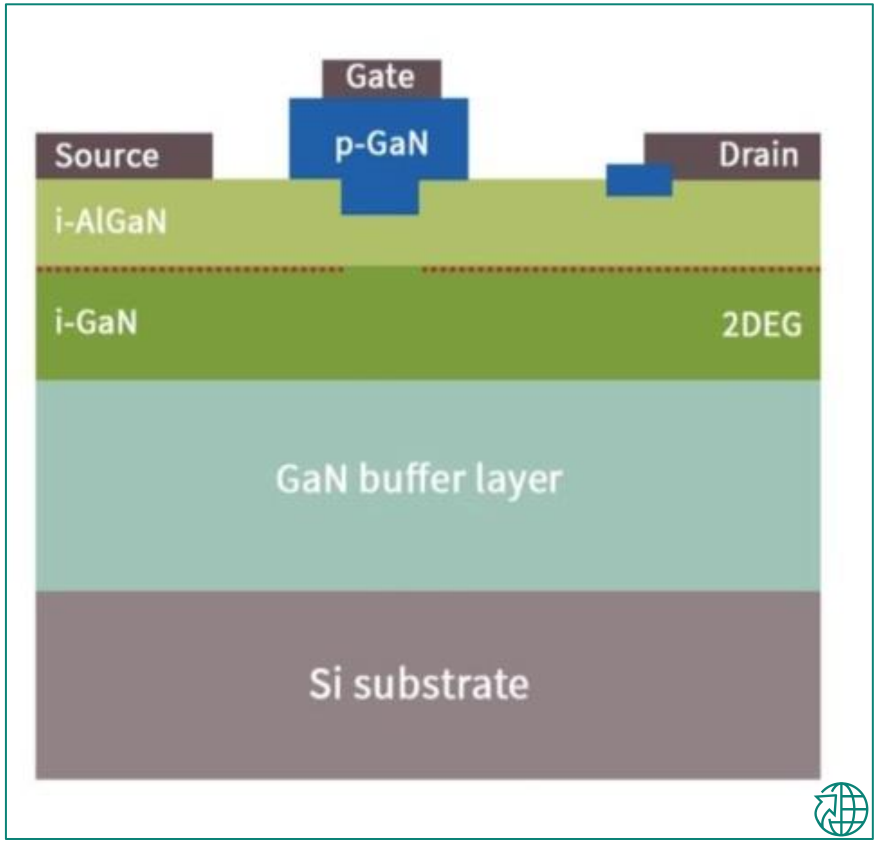


Figure: HV CoolGaN™ GIT Transistor device structure

– Infineon's CoolGaN™ gate injection transistor (GIT) technology is based on a hybrid-drain transistor with p-GaN gate resulting in a robust normally-off power switch.

– To deal with the particularities of this concept, an innovative differential gate-drive concept has been implemented in tailor-made **product family:**

  1- Single-channel gate driver ICs of the EiceDRIVER™ 1EDBx275F product family optimized for CoolGaN™ GIT transistors.

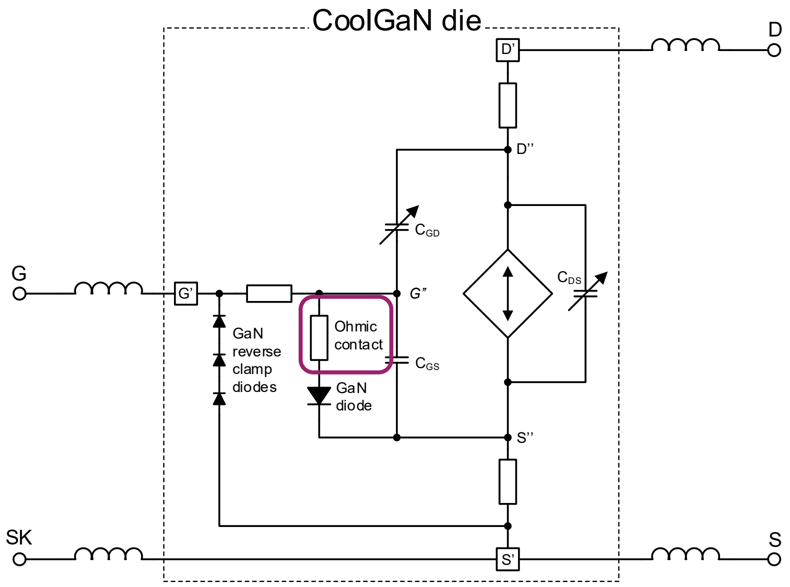
  2- Dual-channel drivers of the EiceDRIVER™ 2EDBx259Y & 2EDRx259X product family feature dead-time control (DTC) and shoot-through protection (STP) to ensure safe operation in half-bridge topologies using a single IC.

– **Potential applications:**
  – Totem-pole PFC and resonant LLC in server, telecom
  – Multilevel topologies in microinverter and energy storage
  – Inverter in motor control and drives
  – Power supply in smart TV

The 1-channel and 2-channel gate driver ICs of the EiceDRIVER™ family are the best choices to match with Infineon's CoolGaN™ GIT Transistors and achieve an optimum combination of efficiency, power density, and robustness in high-performance power conversion applications.

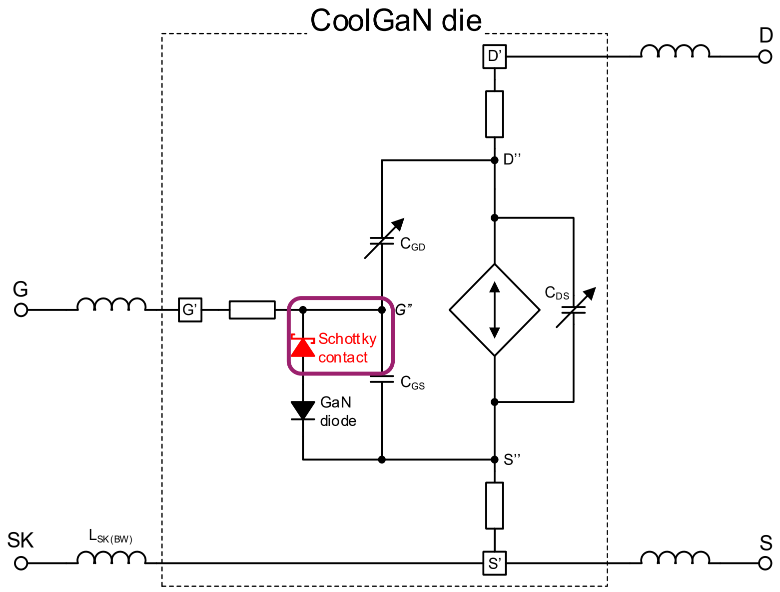
Infineon's CoolGaN™ (GIT & Schottky-gate) + EiceDRIVER™ gate driver ICs provide customers with even more design freedom

HV CoolGaN™ GIT (Gate Injection Transistor)



- **Ohmic contact**
- Non-isolated gate – **current-controlled device**
- Important to control the gate current – performed with a simple RC circuit

MV CoolGaN™ SG (Schottky-Gate) Transistor

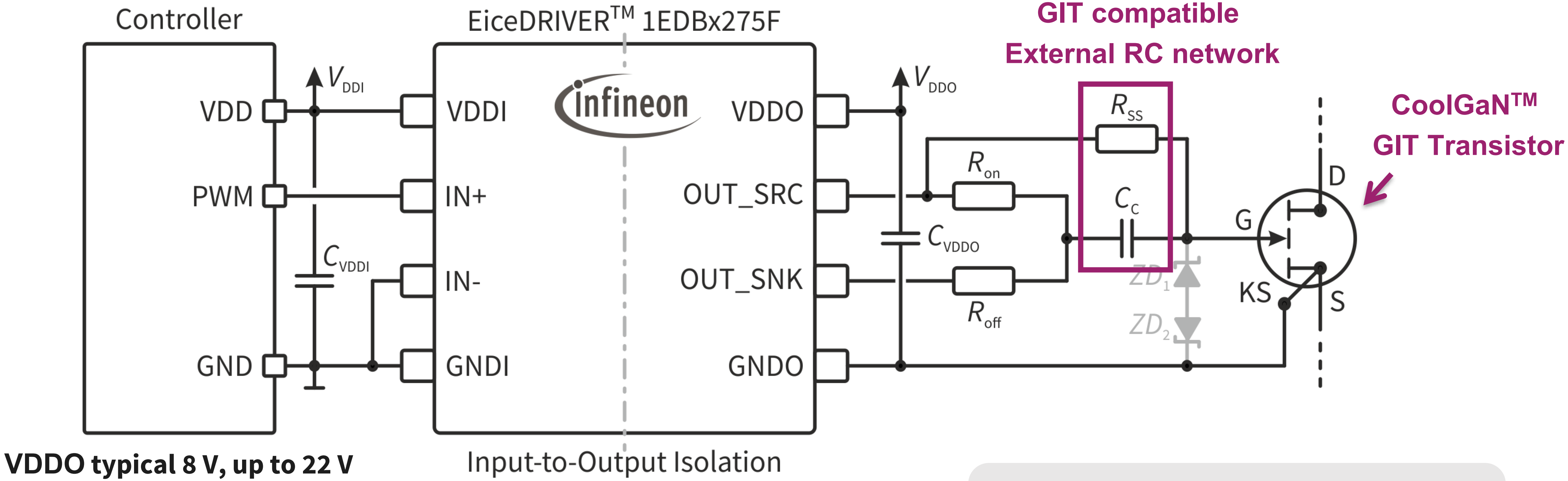


- **Schottky contact**
- Semi-insulated gate – **voltage-controlled device**
- Gate highly sensitive to overvoltage (Schottky contact) – Gate-to-Source voltage regulation is recommended

Infineon EiceDRIVER™ gate driver ICs can drive both GIT & Schottky-Gate GaN transistors

How to drive Infineon CoolGaN™ GIT Gate Injection Transistor

Implementation details of the Gate driver circuitry



[Gate drive solutions for CoolGaN™ GIT Transistors]

– R_{SS} - Determines hold current I_{SS} during ON state

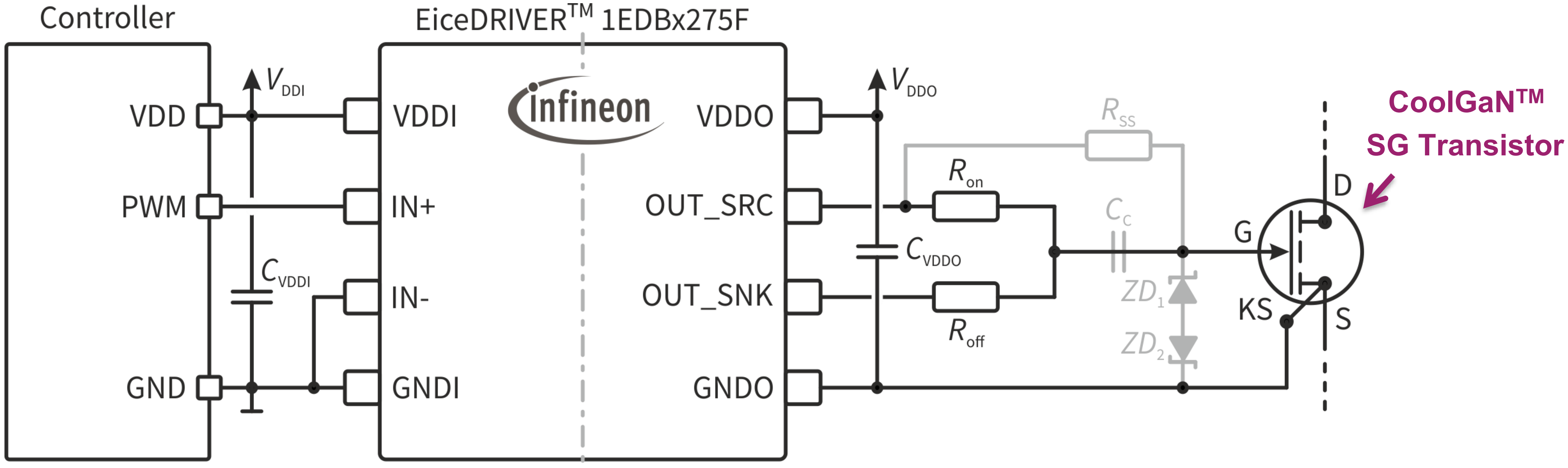
– R_{on}, R_{off} - Transient switching speed dv/dt tuning resistors

– C_C - Coupling capacitor to provide low-ohmic path for dynamic current and **negative** gate bias

External RC network ensures GIT compatibility & Infineon gate drive supports both GIT & SG transistor family

How to drive Infineon CoolGaN™ SG Schottky-Gate Transistor

Implementation details of the Gate driver circuitry



VDDO = 6 V

VDDO = 9 V, bipolar Gate voltage +6 V, -3 V reccommended

- When VDD = 6 V, driving is as for Silicon MOSFET
- R_{on}, R_{off} - Transient switching speed dv/dt tuning resistors

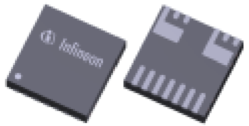
Infineon's gate drive supports family of GIT and Schottky-gate GaN transistors

Gate driver portfolio for high-voltage GaN

Choose EiceDRIVER™ product families for design optimization

GaN Driving

- Broad portfolio of isolated and non-isolated gate driver ICs in 1 channel & 2 channel configuration
- Optimal combination of efficiency, power density, and robustness in high-performance applications
- AEC-qualification
- Dedicated HV GaN gate driver ICs (GIT & SG) in development



SON-13
2EDF7268G

DSO-14 300 mil
2EDRx259X

DSO-14 150 mil
2EDBx259Y

DSO-8 150 mil
1EDBx275F

SOT23 6-pin

1EDNx550B

EiceDRIVER™ gate driver ICs for GaN

For standard & industrial applications - Available today!

Configuration	Product	Package	Input-to-Output isolation: Isolation class	Input-to-Output isolation: Rating	CMTI (min.)	Output UVLO*	Output peak source/sink current	Propagation delay (typ.)	Propagation delay accuracy	Active output clamping	Separate source/sink Output
Single-channel	1EDB7275F	DSO-8 150 mil	Basic Isolation	V_{ISO} = 3 kV_{rms} UL 1577	**300 V/ns**	4 V	**5 A / 9 A**	45 ns	- 4 ns / + 6 ns	**Yes** ✓	**Yes** ✓
	1EDB8275F					8 V					
Dual-channel	2EDR7259X	DSO-14 300 mil	Reinforced Isolation	V_{ISO} = 5.7 kV_{rms} UL 1577 V_{IOTM} = 8 kV_{pk} IEC 60747-17 EN 62368-1 GB4943.1-2022	150 V/ns	4 V	**5 A / 9 A**	38 ns	- 5 ns / + 9 ns	**Yes** ✓	No No
	2EDR8259X**					8 V					
	2EDB7259Y	DSO-14 150 mil	Basic Isolation	V_{ISO} = 3.0 kV_{RMS} UL 1577		4 V					
	2EDB8259Y					8 V					
	2EDF72x8G	SON-13	Functional Isolation	V_{IO} = 1.5 kV_{RMS}	100 V/ns	4 V					
Single-channel	1EDN7550B	SOT23 6-pin	Non-Isolated	n.a.	n.a.	4 V	**5 A / 9 A**	45 ns	- 7 ns / + 10 ns	**Yes** ✓	**Yes** ✓
	1EDN8550B					8 V					

* 8 V UVLO parts recommended for bipolar driving

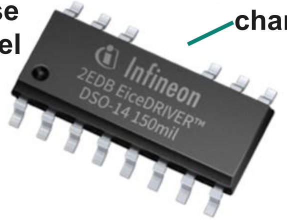
** 2EDR8258X with ENABLE function also available

Visit webpage to buy online

DSO-8 150 mil
1EDBx275F

Creepage increase channel to channel 3.3 mm

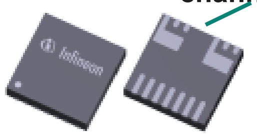
DSO-14 300 mil
2EDRx259X



Creepage increase channel to channel 3.3 mm

DSO-14 150 mil
2EDBx259Y

SOT23 6-pin
1EDNx550B



Creepage increase channel to channel 1.2 mm

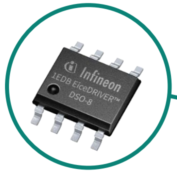
SON-13
2EDF7258G

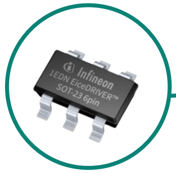
Evaluation boards to drive high-voltage GaN

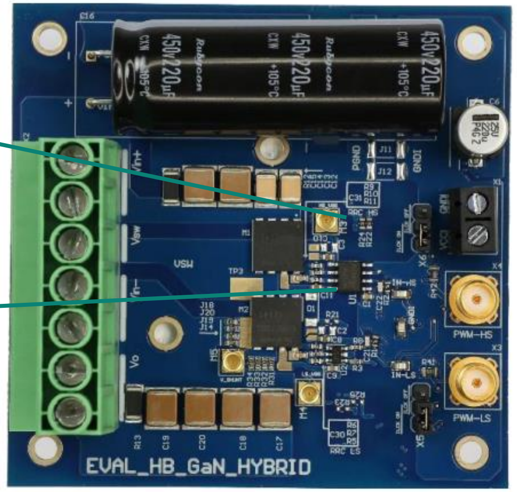
Using dedicated 1-ch and 2-ch EiceDRIVER™ products

EVAL_HYBRID_HB_GaN

EiceDRIVER™ 1EDB7275F







EiceDRIVER™ 1EDN7550B

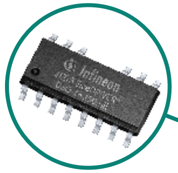
Half-bridge configuration to achieve a BOM and cost-effective solution for HV GaN
CoolGaN™ IGLD60R070D1

KIT_1EDB_AUX_GaN

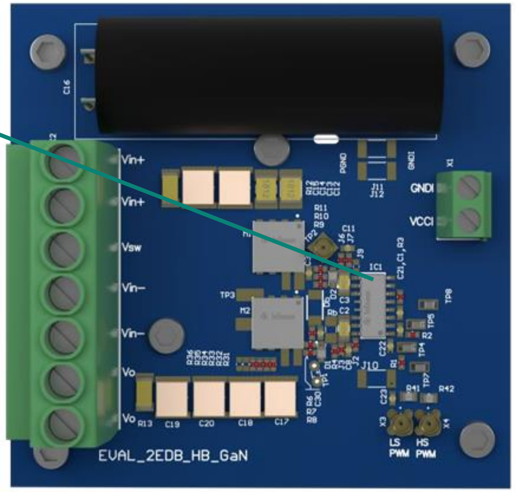
EiceDRIVER™ 1EDB8275F

Compact board with integrated bias supply for HV GaN and option for 1% regulation

EVAL_2EDB_HB_GaN



EiceDRIVER™ 2EDB8259Y



Universal half-bridge platform with integrated bias supply for HV GaN
CoolGaN™ IGLD60R070D1

Simple layout steps for maximizing GaN design performance

The practical problem

Interference problems on a PCB

To avoid

Slow down the switching speed of power devices

This solution generates

Power consumption

Efficiency

Not suitable for

High-efficiency & high-power density specifications

– In past if engineers were faced with interference problem on PCB, a common way to avoid this problem was a slow down the switching speed of power devices.

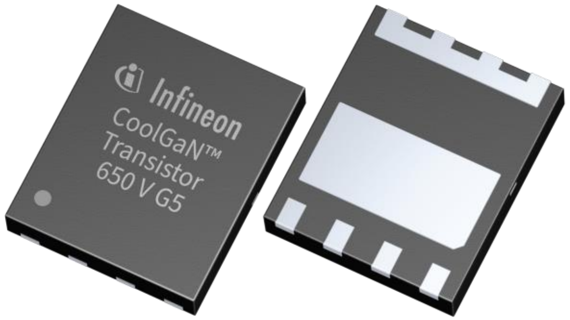
– However, this solution generated more power consumption and reduced efficiency, which is not suitable for today’s high-efficiency and high-power density specifications.

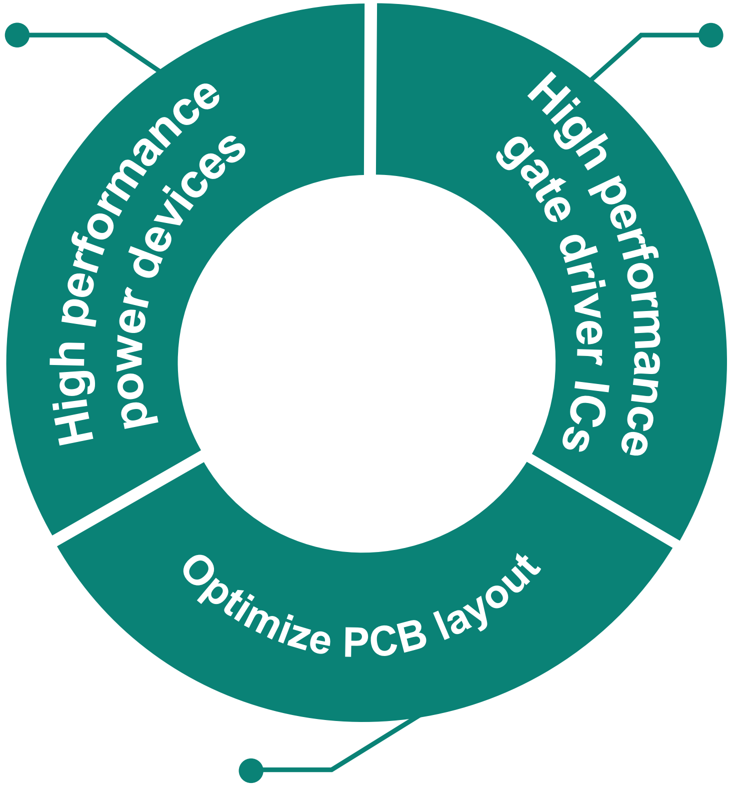
So, what is the solution?

So, what is the current solution?

Component’s of PCB design

– **CoolGaN™** :
Fast switching characteristics





– To drive components perfectly

– Minimize non-ideal features on the PCB
– Allow fast switching operation on devices & circuits

Simple layout steps to maximize GaN performance

Step 1: Prepare the schematics and identify the components of each critical loop

- Isolated gate driver circuit for single GaN transistor
- Isolated gate driver circuit for paralleled GaN transistors
- Half-bridge Bootstrap gate driver circuit

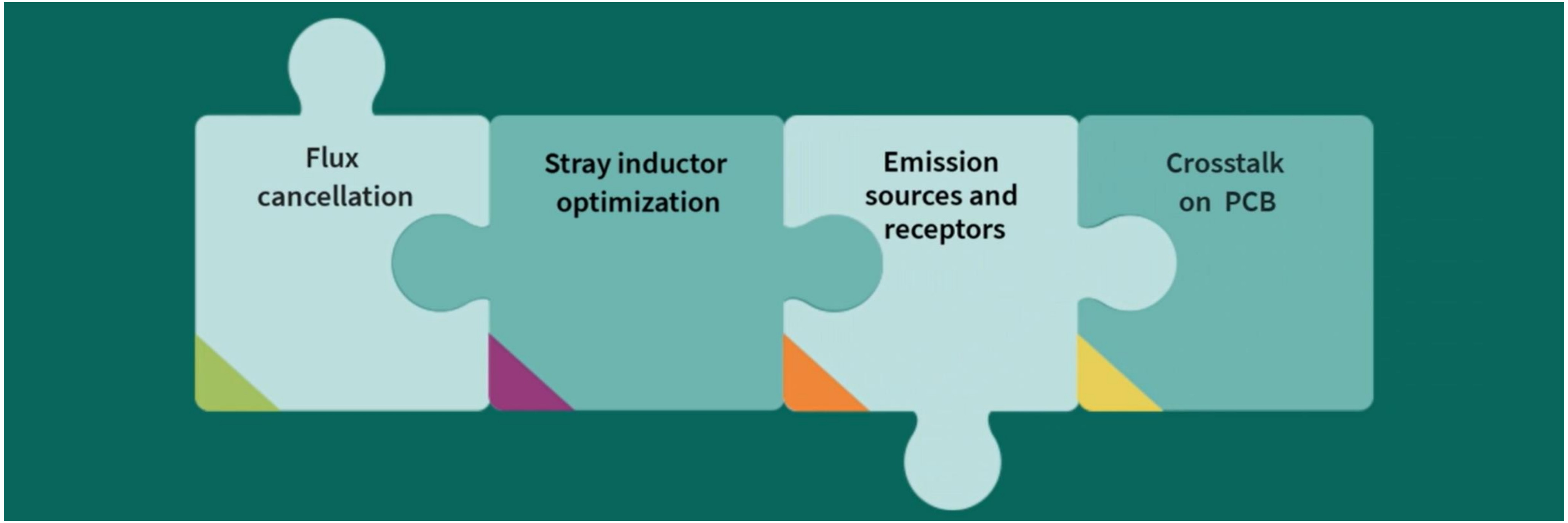
Step 2: Place the components according to the design priority and current direction

- Put components as near to each other as possible
- According to the current direction, set the component in sequence
- If there is a conflict for minimizing all the loops, refer to the priorities previously listed

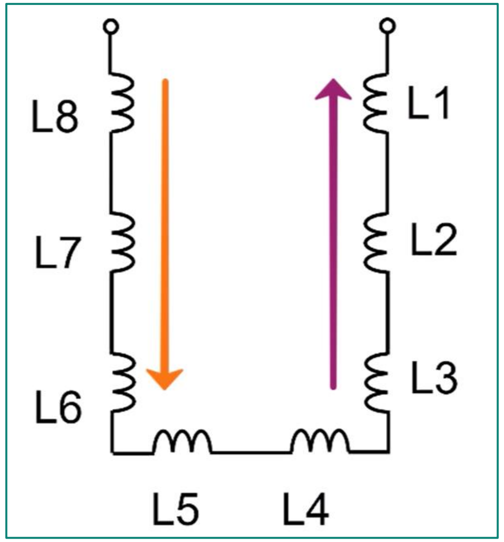
Step 3: Connect components to achieve low parasitics with flux cancellation techniques

Step 4: Verify the switching performance by performing double pulse tests

How to optimize the layout



The importance of minimizing the power loop stray inductance

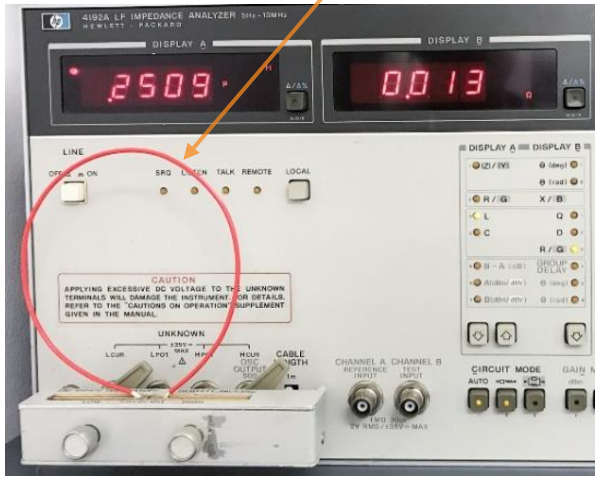


- When high di/dt current flows through the circuit, it leads to generation of a voltage spike across the stray inductor, thus unwanted devices stress and power losses
- This phenomenon occurs regardless of whether it is in the emission source or receptor loops

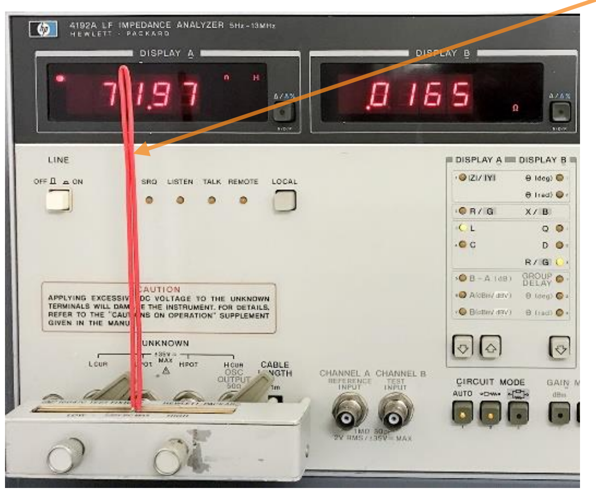
Let's see how to minimize this stray inductance

The relationship between loop geometry and inductance

- Below shows a loop of wire 100 mm diameter on the left
- And the same loop formed into a 150 mm side-by-side stripline on the right



This loop measures 250 nH



The same wire formed into a stripline measures only 72 nH, a **3.5X reduction**

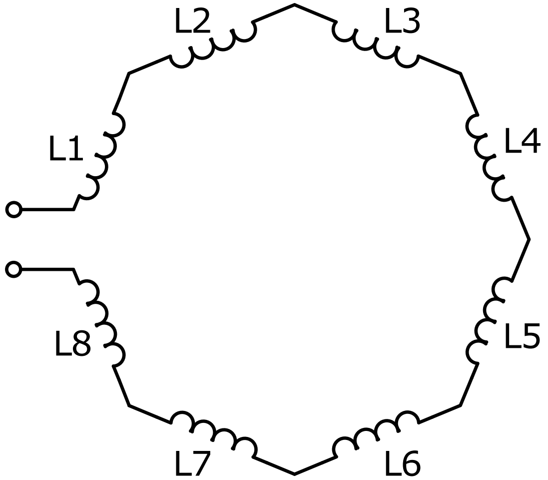
(Both measurements @ 1 MHz)

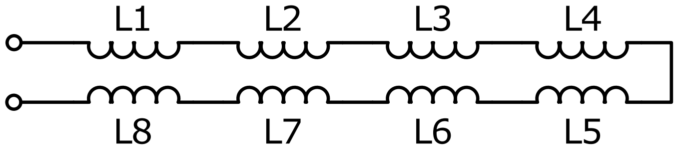
There are two ways to think about this:

- The loop area explains the difference
- Mutual inductance makes the difference
- These are related concepts and **both are correct**

The relationship between loop area and mutual inductance

– Think of both the loop and stripline as being comprised of discrete inductors





– Very little mutual inductance between these elements in the large loop, so the total inductance is essentially the sum of the individual elements

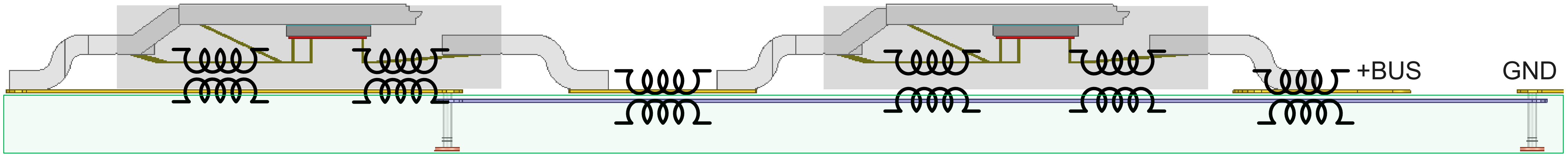
– The stripline has small area but high mutual inductance, and the mutual inductance subtracts from the sum of individual elements (negative sign because the direction of current is opposite)

$$L_{Loop} \approx \sum_{n=1}^{n=8} L_n$$

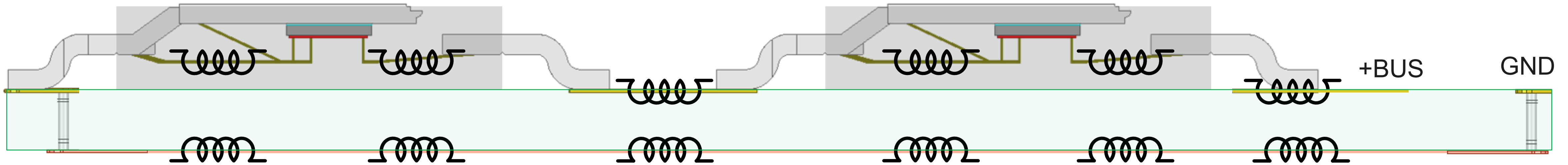
$$L_{Loop} \approx \left(\sum_{n=1}^{n=8} L_n\right) - M_{L1-L8} - M_{L2-L7} - M_{L3-L6} - M_{L4-L5}$$

Application of this concept to the PCB layout of a half-bridge topology

– In both the HB PCB layouts below, the loop begins at +BUS and ends at GND. The individual inductive elements represent the wire bonds in the transistor package, the leadframe, copper segments on the PCB and so on.



1. In the power loop above, the narrow spacing between layers maximizes the mutual inductance, thus minimizing the overall power-loop inductance

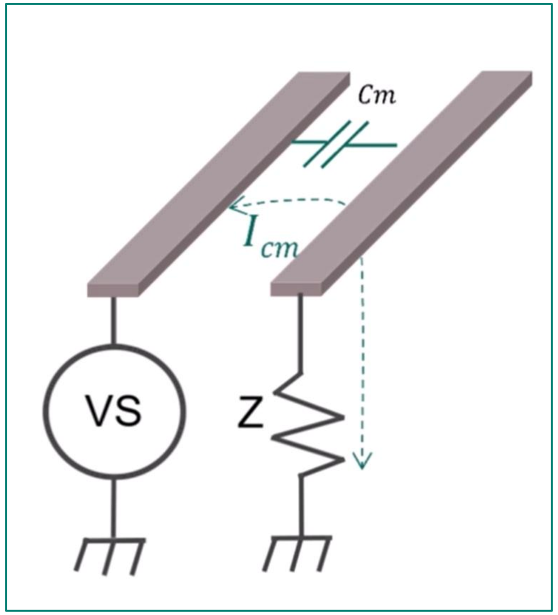


2. In this second example, the increased layer spacing reduces the mutual inductance results in a higher overall total power loop inductance

Emission sources, receptors and crosstalk

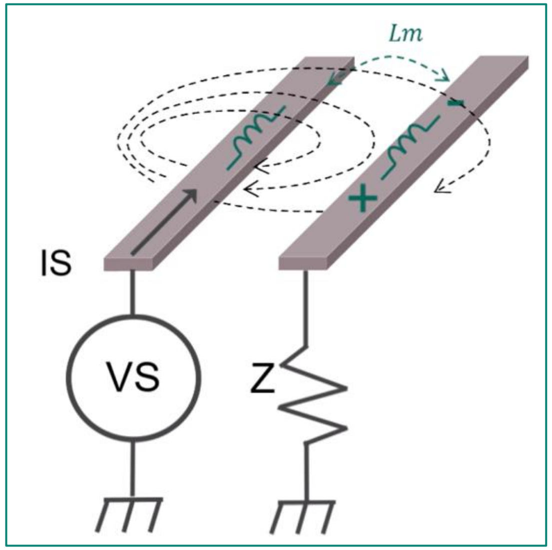
Capacitive crosstalk
(Electric coupling)

dv/dt



Inductive crosstalk
(Magnetic coupling)

di/dt

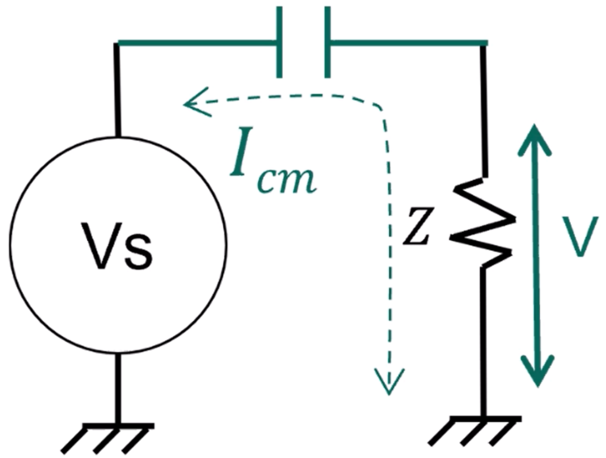


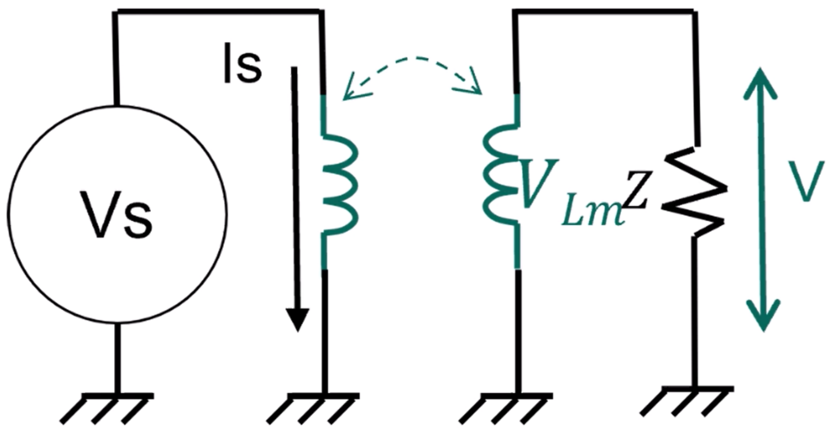
- For high dv/dt, we can use capacitive crosstalk with high-frequency energy and dv/dt will couple to another loop via mutual capacitance.
- The I_{cm} (induced current) in the receptor loop will be the mutual capacitance multiplied by dv/dt

- For high di/dt, we can use inductive crosstalk with high-frequency current energy and di/dt will couple to the receptor via mutual inductance.
- The V_{Lm} (induced voltage) will be mutual inductance multiplied by di/dt

How to reduce coupling?

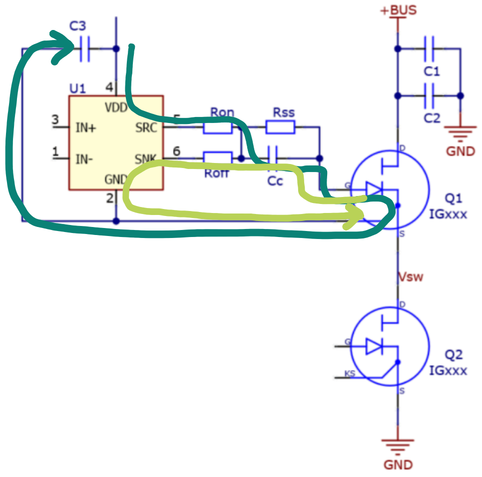
- In PCB design, to reduce the coupling between two loops needs to reduce magnetic lines and try to minimize the impedance of the receptor loop.
- That’s why the methods to cancel the flux and reduce stray inductance in loops are useful.

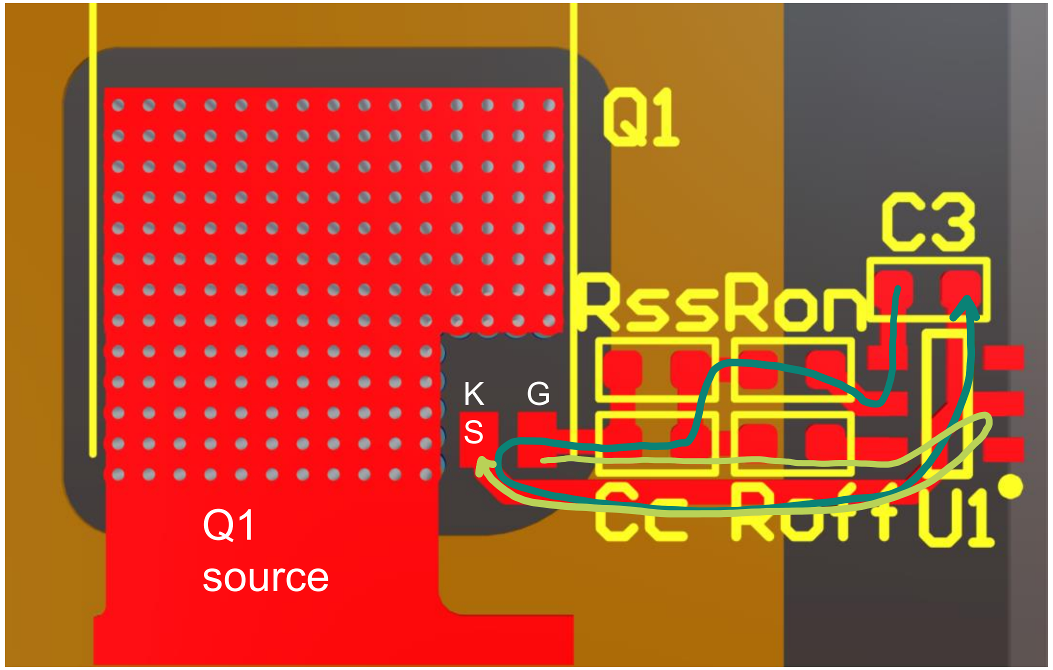




Basic rules for an optimal PCB design

– Review the turn-ON and turn-OFF current loops

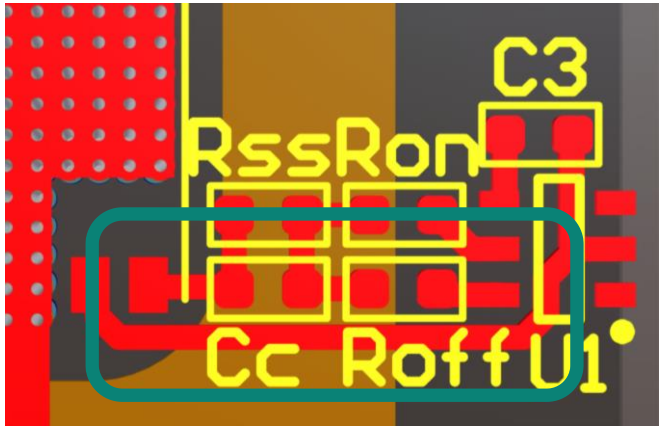




– Is this a good layout?

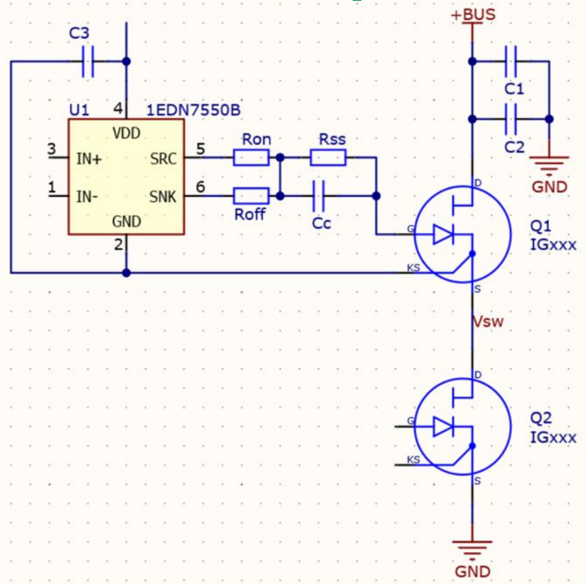
Is this a good layout?

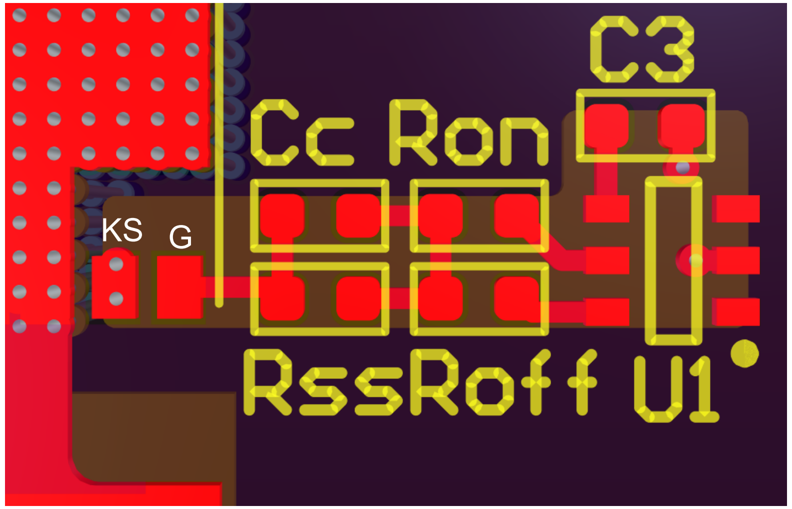
– It is close proximity to the transistor ☑
– Short, direct paths ☑
– Return common as close as it can be…
  (on the same layer→ rather long loop)
– But – is there a better alternative?

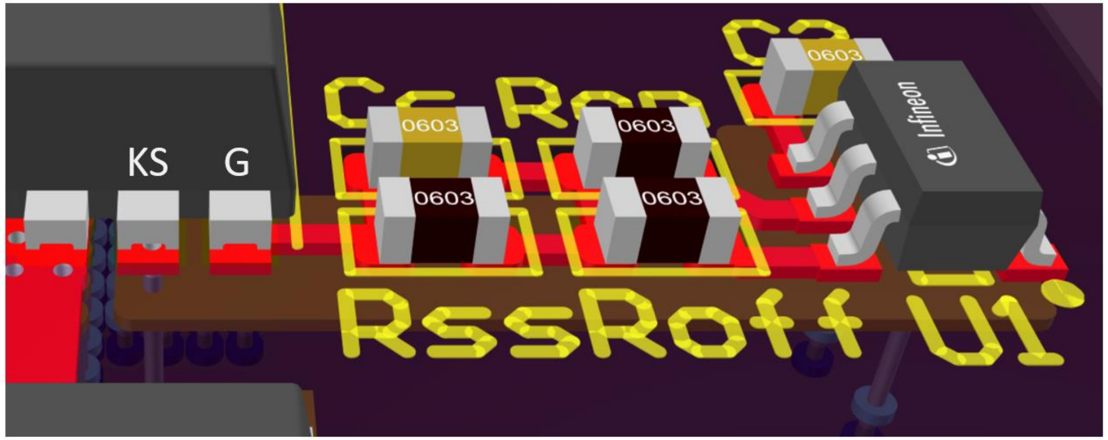


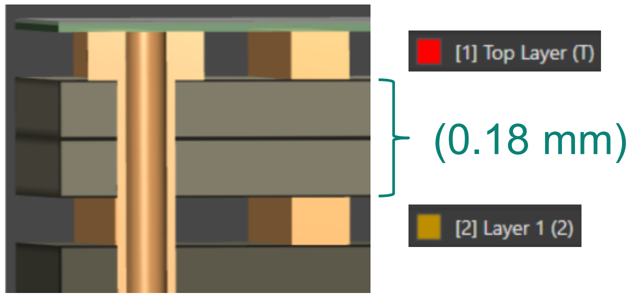
– Easy layout change **reduces the loop area**
  – This will substantially reduce loop inductance
  – But – it requires the second-layer in the PCB stack up

Gate-drive loop(s) need return-path directly below the circuit







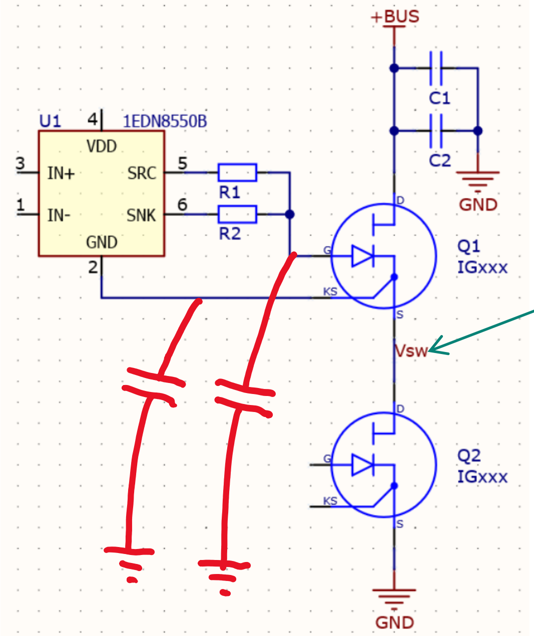


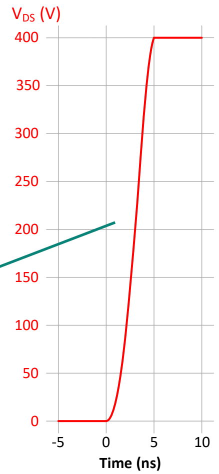
Loop dimensions ≈ **0.2** x 9.8 mm → **loop area reduced 13.5x**

The second possible problem with this layout: The high-side gate-drive circuit is directly over a ground-plane

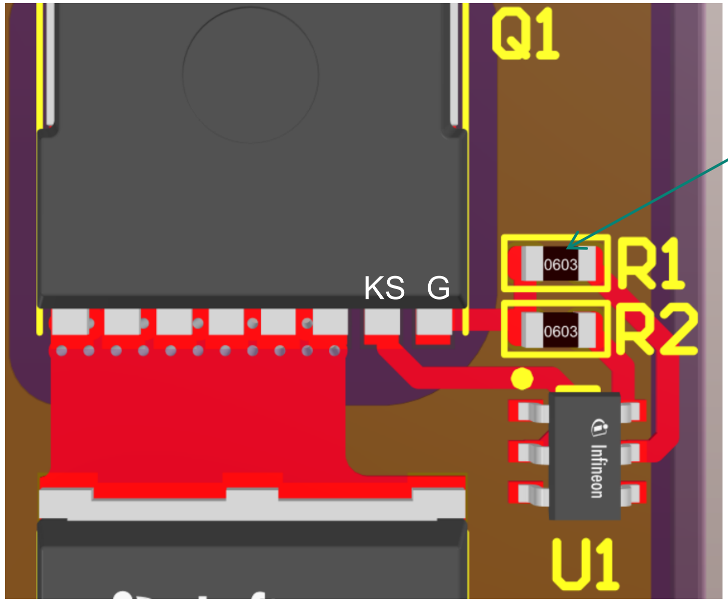
High side gate-drive circuit over ground/power plane

Sometimes high-side gate-drive circuit has to cross-over ground-plane…





100 V/ns



≈ 1 pF for 0603 to GND

The resulting current injected into the gate-drive circuit can have severe consequences
C may be very small, but **dv/dt** may be very large: 1 pF x 100 V/ns = 100 mA

Never place unshielded high side gate-drive circuit over ground/power plane

Thermal management guidelines for GaN transistors

Importance of device thermal management

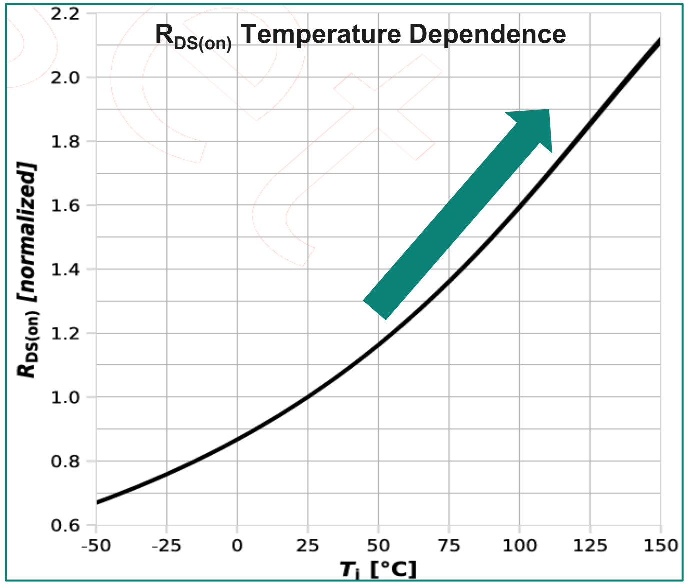
– A good thermal design from both device-level and system-level is critical. Two electrical parameters dependent on temperature:

1- $R_{DS(on)}$ and conduction loss

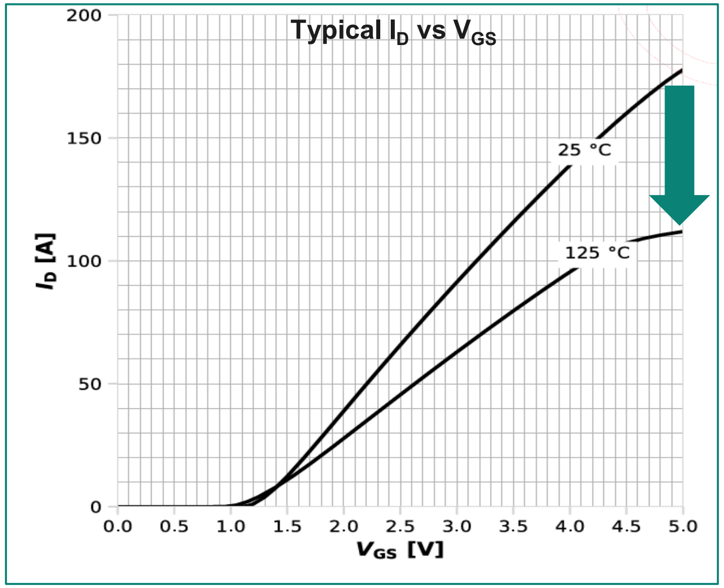
2- Transconductance (g_m) and switching loss

1. $R_{DS(on)}$ and conduction loss

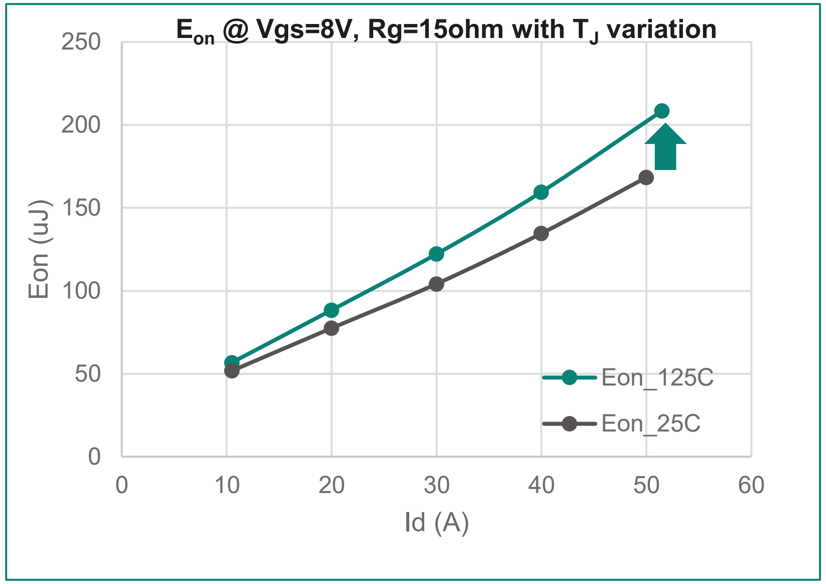
2. Transconductance and switching loss



$R_{DS(on)}$ vs T_J for
CoolGaN™ Transistor 650 V G5



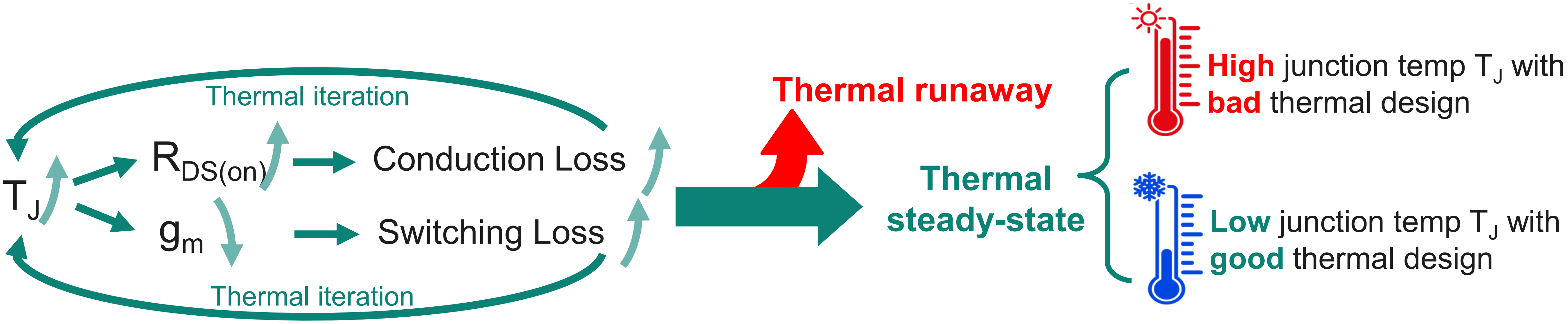
Transconductance g_m vs T_J for
CoolGaN™ Transistor 650 V G5



E_{on} with T_J variation for
CoolGaN™ Transistor 650 V G5

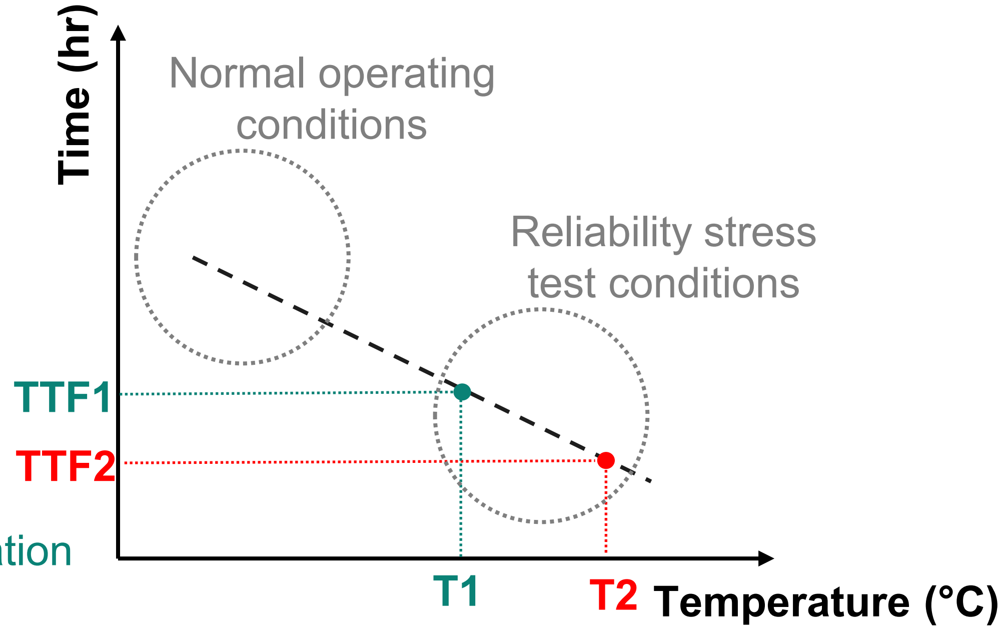
Need to properly manage T_J to minimize losses

Reasons to keep device cool



Reasons to keep device cool:

1. **Prevents thermal runaway at maximum/worst operating conditions**
2. **Reduce overall loss and improve system efficiency**
3. **Improve system reliability**



Time to failure with temperature acceleration

GaN reduces power losses

	GaN characteristics	System impact
Hard-switching mode	Zero reverse recovery loss Low capacitive E_{oss}/E_{qoss} loss Excellent transconductance	Switching-on loss ↓
ZVS soft-switching mode	Fast switching speed →	Switching-off loss ↓
	Low energy-related $C_{oss(ER)}$ →	Inductive energy to achieve ZVS, less reactive power loss ↓
	Low time-related $C_{oss(TR)}$ →	Deadtime ↓
	Low gate charge Q_g →	Gate driver loss ↓

Due to its excellent electrical performance, GaN enhances both soft-switching and hard-switching applications

Packaging and thermal solutions in high power density

The growth of :

- Cloud-based services
- Internet services
- Artificial Intelligence
- Cryptocurrency

……has driven strong demand for data centers and increased processing power and this trends creates need for highly efficient and compact server power supplies.

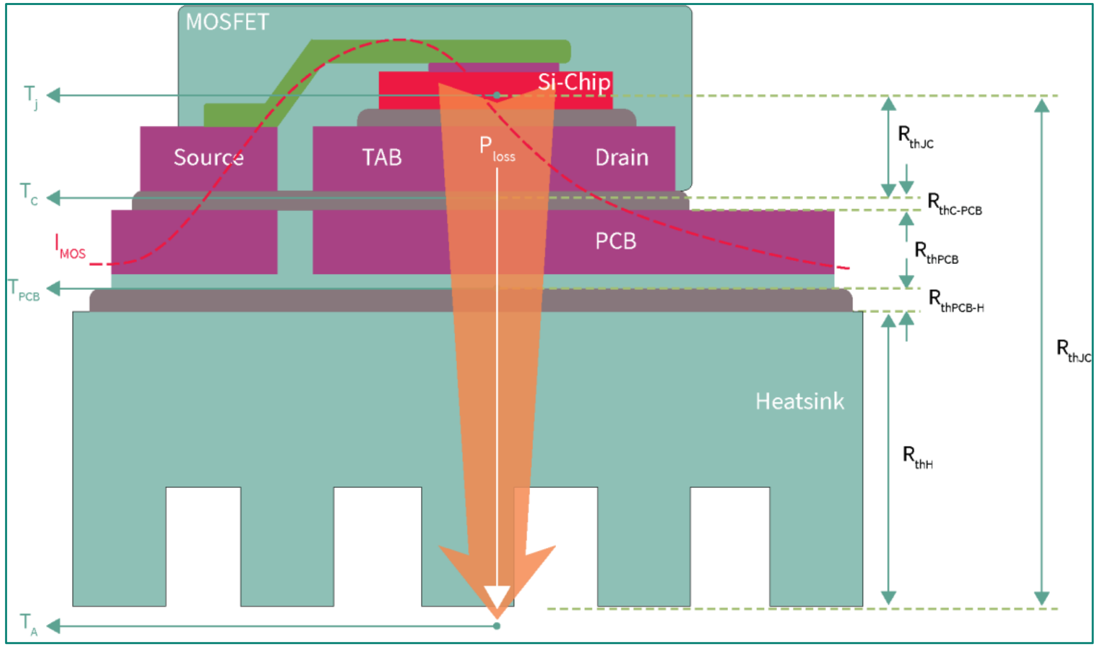
Key contributors to achieve high power density:

1. **Increased efficiency:**
   - enabled by new topologies and technologies
   - e.g. transition from the conventional silicon (Si) classic boost PFC to the GaN/SiC totem-pole PFC

2. **Improved packages and thermal solutions**
   - dissipate the power away from the device junction to heat sinks and ambient.
   - this becomes more challenging in smaller SMD packages that are the main enabler for high-density converters

3. **Optimized system design and switching frequency**
   - reduces size and improve thermal performance
   - this leads to an increased switching frequency, driving the transition from conventional to new packages and thermal solutions

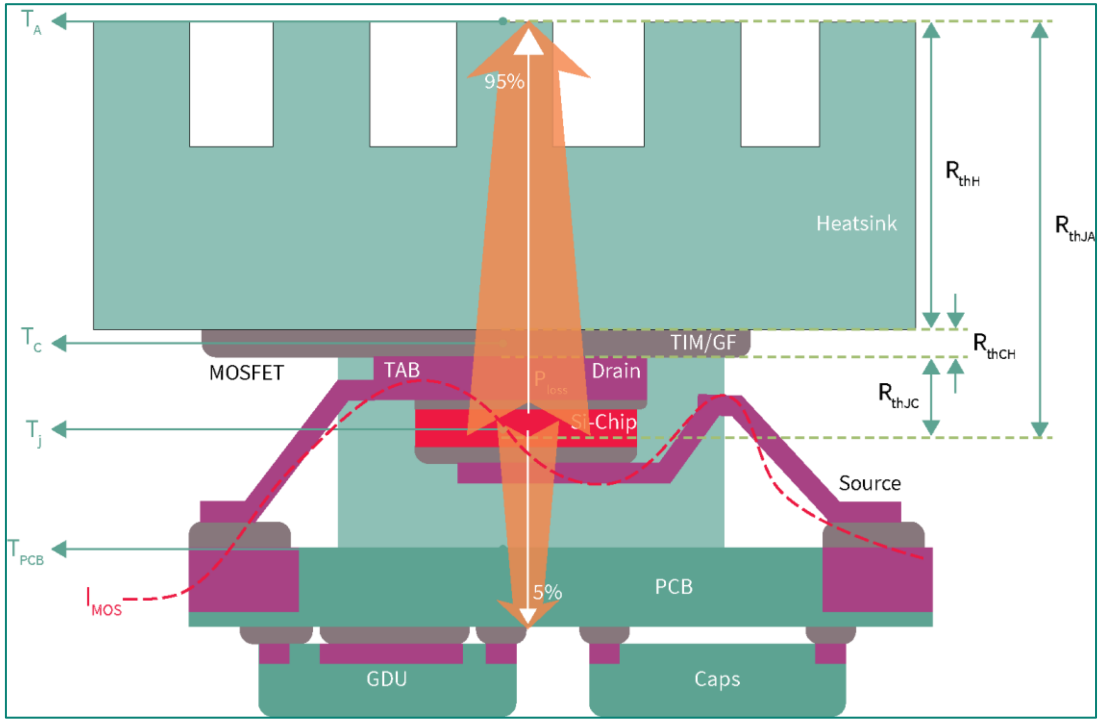
Bottom side cooling (BSC)



- For BSC, the main heat flux is directed from the device heatsink (exposed pad) on the bottom of the package through the PCB to an external heatsink mounted on the opposite side of the PCB.
- Therefore, thermal vias below the package and through the PCB are needed for heat transfer when using an FR4-based PCB.
- On the backside of the PCB, the external heatsink is mounted on the area with the thermal vias.
- The heatsink and the PCB are electrically separated via a thermal interface material (TIM).
- Quite often, a foil with a thickness in the range of 100-500 µm is used as TIM, which has, in the best case, a good thermal admittance λ.
- This leads ideally to a low thermal impedance Zthja for the overall system

BSC enables efficient heat dissipation through thermal vias, and a TIM-isolated external heatsink, reducing thermal impedance, enabling higher power handling

Top side cooling (TSC)



- In TSC packages, the device heatsink on top of the package is interfaced directly to the external heatsink through the TIM (thermal interface material).
- In this case, there is no heat passing through the PCB and thermal vias, therefore eliminating their thermal impedance from the total thermal impedance.
- Results in:
  - enhanced thermal conductivity
  - higher package maximum power dissipation
- Advantage:
  - free PCB area on the opposite PCB side: that can be used to place other devices such as gate drivers and passive components
  - space for signal routing directly below the package body.

TSC improves thermal performance by avoiding heat flow through the PCB and frees up PCB space for additional components and routing

Value proposition of GaN in high switching frequency topologies

GaN application in high switching frequency topologies

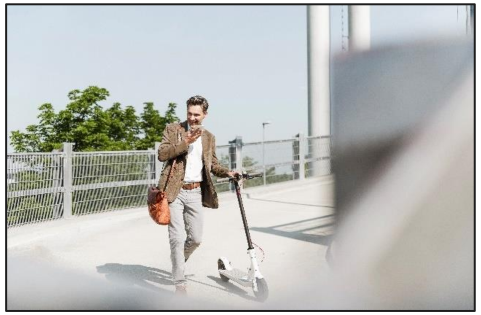
Resonant LLC & TCM PFC

- Server & data center PSU
- Telecom rectifiers
- Industrial AC-DC or DC-DC converters

Cyclo-converter

- On-board chargers in EVs
- Solar microinverters

Hybrid Flyback



- USB PD adapter
- E-bike
- Power tool chargers
- Lightning
- Smart home and IoT devices

Dual Active Bridge

- 10 kW OBC
- Energy storage systems

GaN in Resonant LLC – Value proposition

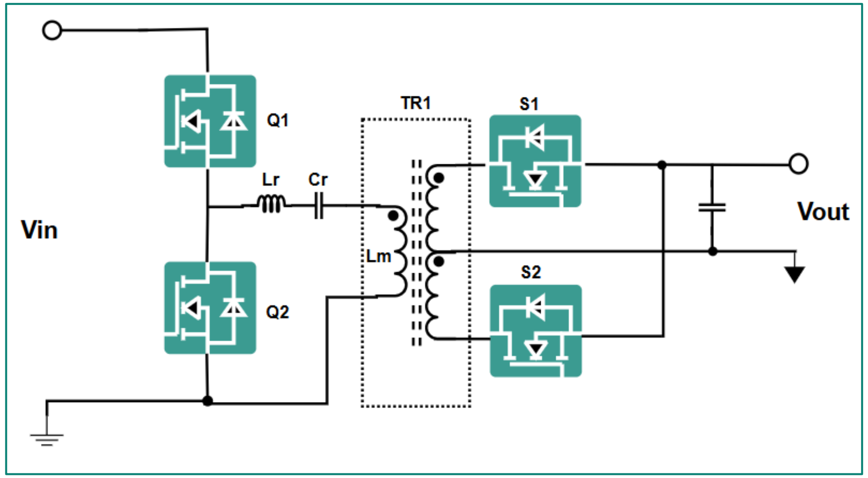


Figure: Principle schematics of a HB LLC

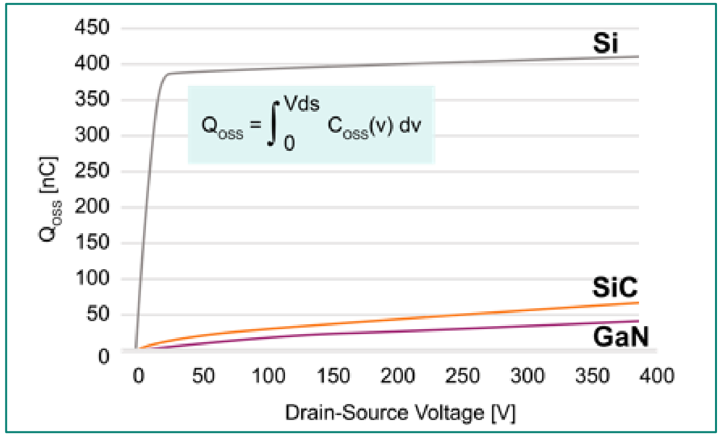


Figure: Q_{OSS} vs. V_{DS} and $R_{DS(ON)}$ *Q_{OSS} comparison

- **High efficiency:** High efficiency at high frequency due to the soft-switching of both primary side and secondary side devices
- **Superior FOM**: CoolGaN™ devices easily address this requirement of a higher switching frequency due to their **superior FoM and lowest switching losses** among Si, SiC, and GaN devices
- Especially in soft-switching LLC converters, CoolGaN™ has the **lowest output capacitor charge (Q_{oss}),** which plays a vital role in reaching ZVS (zero voltage switching) more easily
- **Minimizes dead-time setting:** Eliminates unnecessary dead-time conduction losses on both primary and secondary side

Ideal for use in server and telecom PSU, industrial & medical SMPS, battery charging and consumer application

GaN in TCM PFC - Value proposition

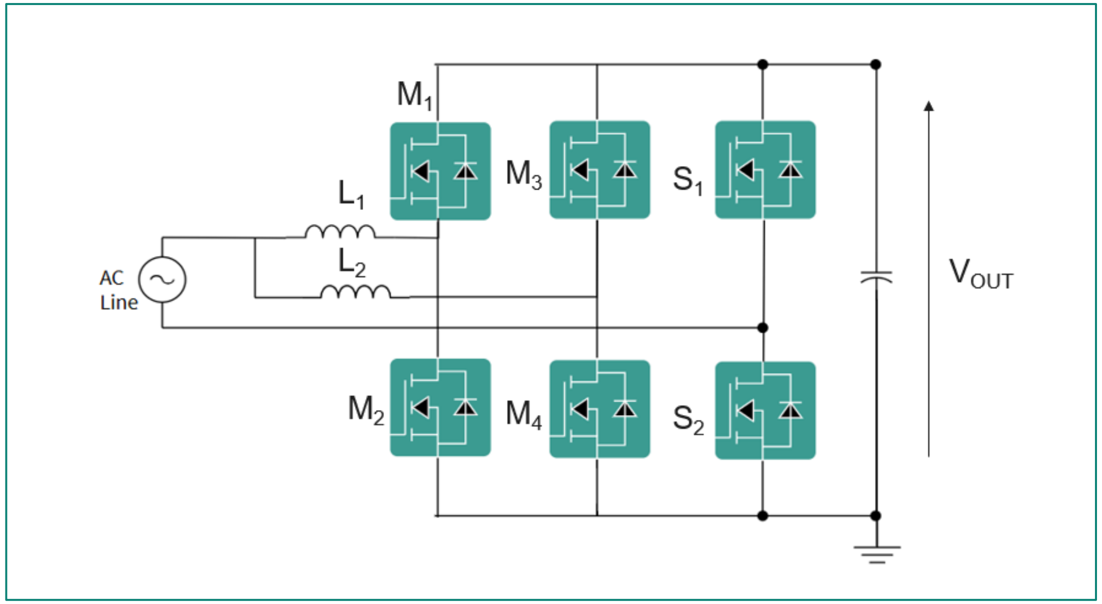


Figure: Schematics of 2-phases interleaved TCM Totem Pole PFC

- **High efficiency**: Reduced switching losses due to soft switching improves overall system efficiency, particularly at light and medium loads
- **Compact design:** Smaller magnetics and components result in lighter, space-saving power supplies
- **Thermal management:** Soft switching operation inherently reduces power losses, thus reducing the size and cost of heatsink and improving reliability

Ideal for use in server and telecom PSU, industrial & medical SMPS, battery charging and consumer application

GaN in Cyclo-converter - Value proposition

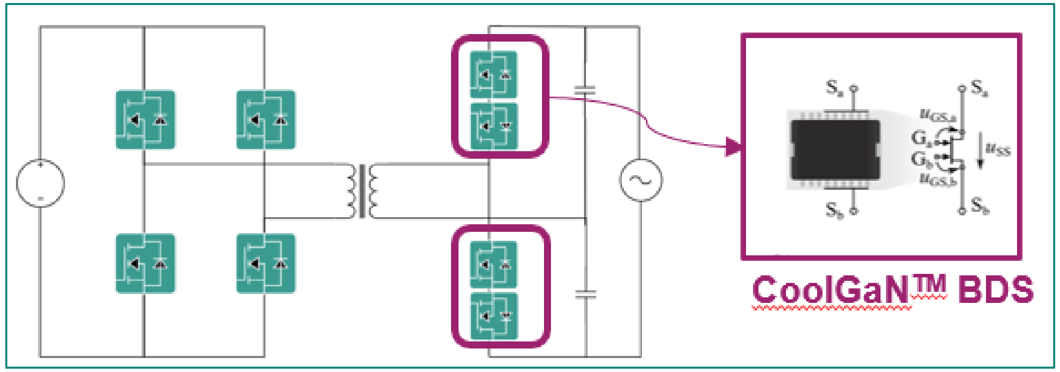


Figure : Cycloconverter microinverter basic topology

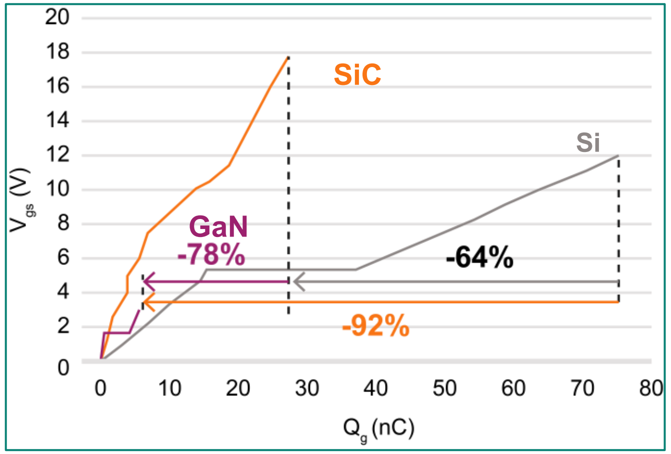


Figure : Gate charge profile comparison of GaN vs. Si vs. SiC

- **Higher efficiency:** Higher efficiency reduced losses and heat dissipation, allow for **higher power and more integration**
- **Lower switching loss:** GaN has the **lowest Q_{gd} and total Q_g** , to enable fastest switching time and lowest switching loss
- **Compact design**: GaN compared to Si and SiC is that it's a lateral device, while Si and SiC are vertical structures, this enable monolithic integration in GaN devices, such as a true normally-off monolithic bidirectional switch, which can **replace the two back-to-back switches** of the cyclo-converter
- **Cost effective**: This offers **cost-effective high-performance** solution, **smaller PCB** area and **BOM reduction**

Ideal for use in on-board chargers in electric vehicles and solar microinverters

GaN in Hybrid Flyback - Value proposition

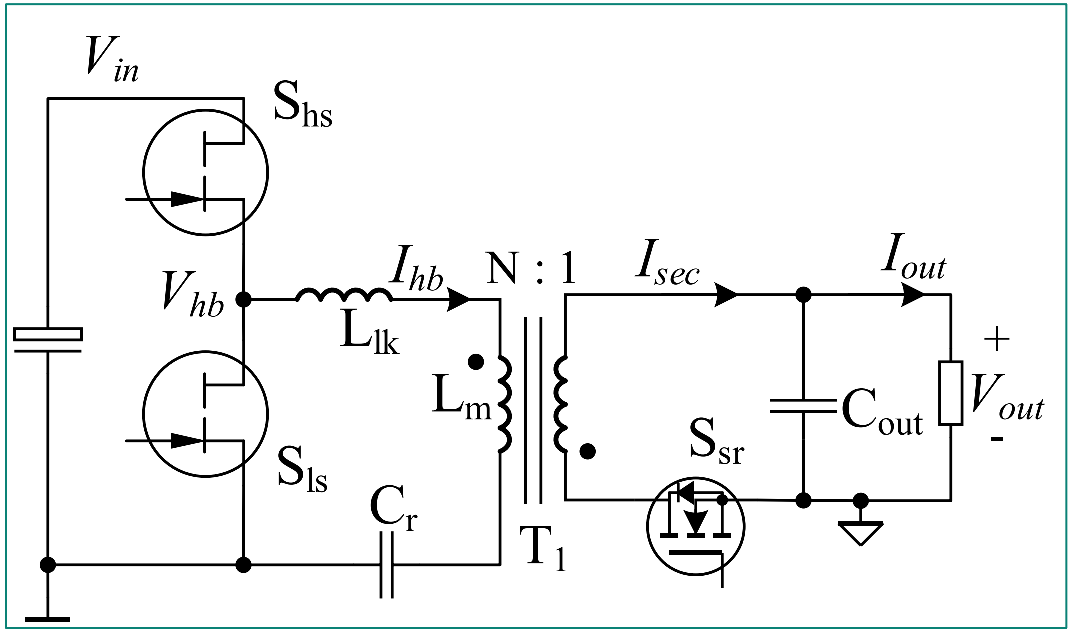


Figure : Hybrid Flyback topology

- **High efficiency:** High switching frequency is desired to **achieve small size** and **efficient operation**
- **Compact and cost-effective:** It can help to reduce the size of the magnetic components which are one of the major contributors for the size of the power supply
- **Enhanced EMI performance: EMI filter components could be reduced** when higher switching frequencies are used
- **Superior FOM:** GaN devices compare to other technologies like Silicon offer the **best FOM** (figure of merit) $R_{DS(on)}$ x C_{oss}

Ideal for use in USB-PD & fast chargers, LED lightening drivers, E-bikes, power tool chargers and smart home & IoT devices

GaN in Dual Active Bridge (DAB) - Value proposition

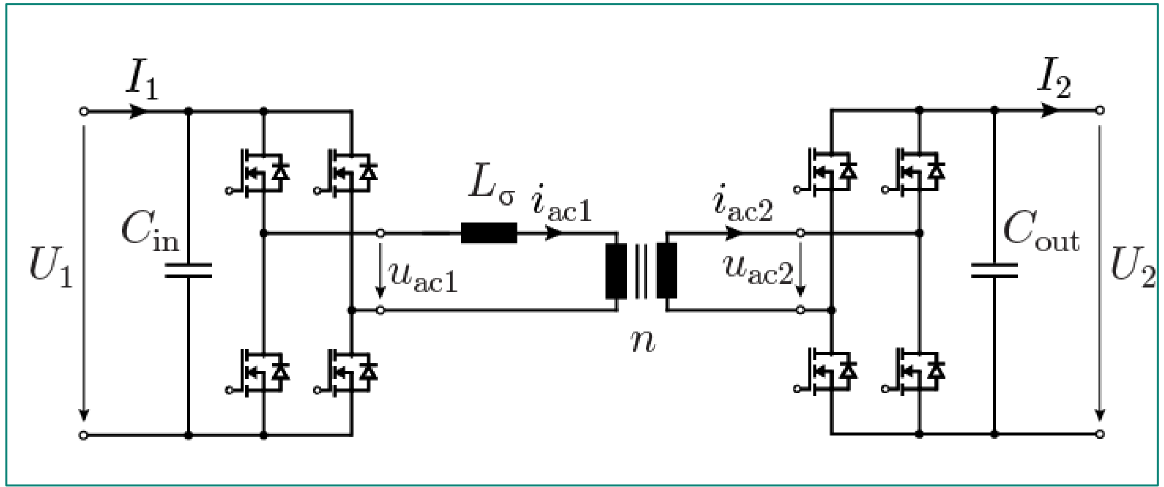


Figure : Dual Active Bridge (DAB) topology

- **High efficiency with soft-switching:** GaN is highly suitable for high-frequency soft-switching applications, with a low Q_{oss}, linear C_{oss}, and very low soft-switching (turn-off) losses

- **High power density:** High-switching frequency enablement with GaN, not only can the DAB be built in a very efficient way for wide voltage range operation, but it can also be done in a very compact manner, increasing power density

- **Bidirectional power flow:** Supports seamless energy transfer in both directions

Ideal for use in on-board chargers and energy storage systems

Key takeaways

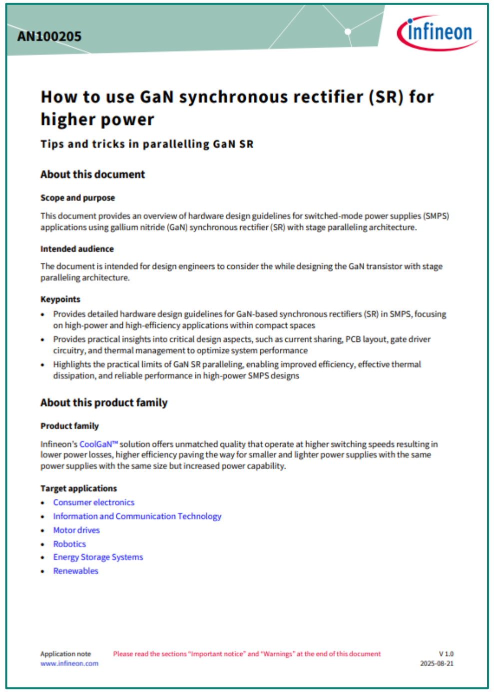
Key takeaways

- **Infineon leads** in all power semiconductor technologies (Si, SiC, GaN), offering unmatched material expertise, system integration, and reliability
- **GaN market is growing** rapidly with a projected 47% CAGR, expected to $8 bn cumulative market potential over the next 5 years
- Infineon provides **gate driving solutions** compatible with both GIT and SG GaN types using the EiceDRIVER™ family of ICs
- **Optimized PCB layout** techniques are critical to optimize GaN performance, and minimize switching losses
- **Thermal management** is essential for reliability and efficiency; Infineon supports both top-side and bottom-side cooling for improved heat dissipation
- **GaN enables high-frequency soft-switching topologies** like LLC, TCM PFC, and DAB, offering compact, efficient power supply designs
- Overall, **CoolGaN™ technology enables** compact, high-density, and cost-effective power solutions across a wide voltage and power range

Related White Papers and App Notes (Links Embedded)

Considerations and guidelines for using high-voltage CoolGaN™ switches in power systems

Bernhard Zojer, Infineon Technologies Austria AG



AN100205

How to use GaN synchronous rectifier (SR) for higher power

Tips and tricks in parallelling GaN SR

About this document

Scope and purpose

This document provides an overview of hardware design guidelines for switched-mode power supplies (SMPS) applications using gallium nitride (GaN) synchronous rectifier (SR) with stage paralleling architecture.

Intended audience

The document is intended for design engineers to consider the while designing the GaN transistor with stage paralleling architecture.

Keypoints

- Provides detailed hardware design guidelines for GaN-based synchronous rectifiers (SR) in SMPS, focusing on high-power and high-efficiency applications within compact spaces
- Provides practical insights into critical design aspects, such as current sharing, PCB layout, gate driver circuitry, and thermal management to optimize system performance
- Highlights the practical limits of GaN SR paralleling, enabling improved efficiency, effective thermal dissipation, and reliable performance in high-power SMPS designs

About this product family

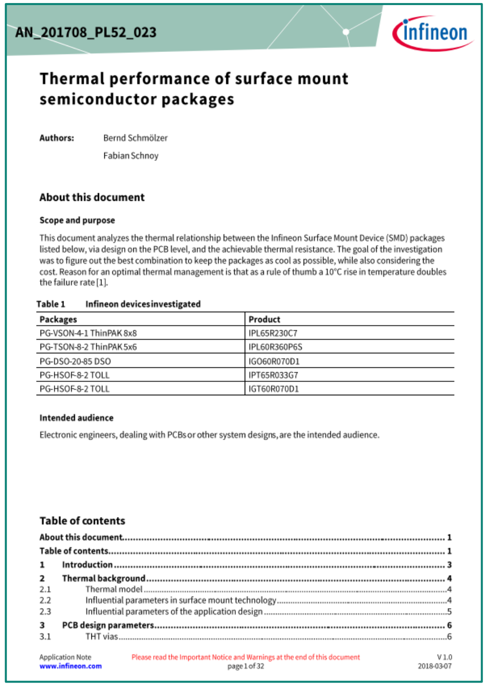
Product family

Infineon's CoolGaN™ solution offers unmatched quality that operate at higher switching speeds resulting in lower power losses, higher efficiency paving the way for smaller and lighter power supplies with the same power supplies with the same size but increased power capability.

Target applications

- Consumer electronics
- Information and Communication Technology
- Motor drives
- Robotics
- Energy Storage Systems
- Renewables

Application note www.infineon.com Please read the sections "Important notice" and "Warnings" at the end of this document V 1.0 2025-08-21



AN_201708_PL52_023

Thermal performance of surface mount semiconductor packages

Authors: Bernd Schmölzer, Fabian Schnoy

About this document

Scope and purpose

This document analyzes the thermal relationship between the Infineon Surface Mount Device (SMD) packages listed below, via design on the PCB level, and the achievable thermal resistance. The goal of the investigation was to figure out the best combination to keep the packages as cool as possible, while also considering the cost. Reason for an optimal thermal management is that as a rule of thumb a 10°C rise in temperature doubles the failure rate [1].

Table 1 Infineon devices investigated

Packages	Product
PG-VSON-4-1 ThinPAK 8x8	IPL65R230C7
PG-TSON-8-2 ThinPAK 5x6	IPL60R360P6S
PG-DSO-20-85 DSO	IGO60R070D1
PG-HSOF-8-2 TOLL	IPT65R033G7
PG-HSOF-8-2 TOLL	IGT60R070D1

Intended audience

Electronic engineers, dealing with PCBs or other system designs, are the intended audience.

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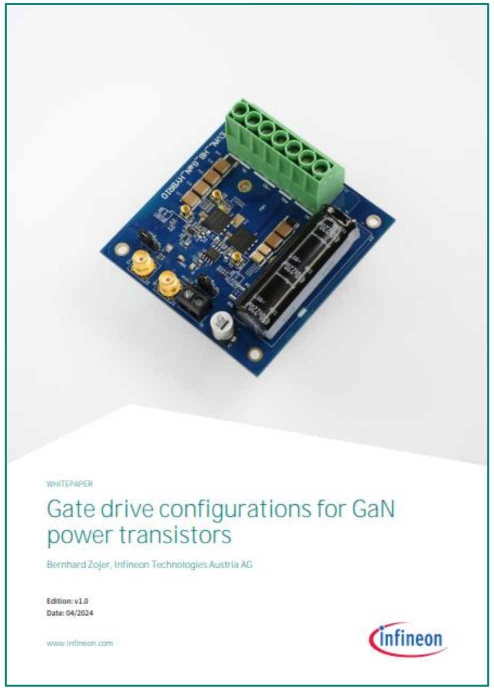
Application Note www.infineon.com Please read the Important Notice and Warnings at the end of this document V 1.0 page 1 of 32 2018-03-07



WHITEPAPER

Gate drive configurations for GaN power transistors

Bernhard Zojer, Infineon Technologies Austria AG

Edition: v1.0

Date: 04/2024

www.infineon.com

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